

## Article

# Implementation of High-Speed Compact Level-Up Shifter for Nano-Scale Applications

Muppidi Venkata Sudhakar <sup>1</sup> and Ovidiu Petru Stan <sup>2,\*</sup><sup>1</sup> Department of Electronics and Communication Engineering, Lakireddy Bali Reddy College of Engineering, Mylavaram 521230, India; venkatasudhakarm@lbrce.ac.in<sup>2</sup> Faculty of Automation and Computer Science, Technical University of Cluj Napoca, 400114 Cluj-Napoca, Romania

\* Correspondence: ovidiu.stan@aut.utcluj.ro

**Abstract:** The objective of this study is to present a level shifter architecture that utilizes a pair of inverters and a Wilson current mirror to reduce power consumption while improving voltage shifting capabilities. We introduce novel components such as super-cut-off pull-down and stacked pull-up networks to effectively minimize leakage power. Our design leverages multi-threshold CMOS (MTCMOS) technology, incorporating sleep transistors to boost operational speed, decrease power consumption, and reduce the physical footprint. The proposed circuit is engineered to step up voltage levels, ranging from a mere 0.4 V to a substantial 1.2 V. Through extensive optimization of performance parameters, including power efficiency, delay, and area utilization, we have tailored this design to cater specifically to the demands of nano-scale applications. Key results from our research reveal that the average active power consumption for “level-up” shifts is impressively low at 48.5 nW, with an average latency of a mere 1.58 ns for 1 MHz transmission frequencies. Post-layout modeling demonstrates that our suggested design occupies a compact area of just 9.97  $\mu\text{m}^2$ . These findings were meticulously modeled using Cadence Virtuoso with 45 nm processes. Furthermore, our research highlights the substantial advancements achieved when compared to previous methods. The proposed design boasts a threefold increase in operational speed and delivers significant savings in both area and power consumption. These outcomes have far-reaching implications for emerging technologies and applications in the field.

**Keywords:** level shifter; leakage; MTCMOS; super-cut-off pull-down; stacked pull-up networks



**Citation:** Sudhakar, M.V.; Stan, O.P. Implementation of High-Speed Compact Level-Up Shifter for Nano-Scale Applications. *Electronics* **2023**, *12*, 5015. <https://doi.org/10.3390/electronics12245015>

Academic Editors: Nabil Yassine, Abdallah Tammam and Khaled Hayatleh

Received: 8 November 2023

Revised: 9 December 2023

Accepted: 12 December 2023

Published: 15 December 2023



**Copyright:** © 2023 by the authors. Licensee MDPI, Basel, Switzerland. This article is an open access article distributed under the terms and conditions of the Creative Commons Attribution (CC BY) license (<https://creativecommons.org/licenses/by/4.0/>).

## 1. Introduction and Literature Survey

Level shifters are commonly employed in a wide variety of applications for System-on-Chips (SoCs) in order to enable communication between different voltage domains. Sensors on SoCs operate at voltage levels different from those used by the core circuitry. Level shifters allow communication between sensor outputs and the core logic, simplifying data transmission. Different forms of memory, such as double-data rate (DDR) and flash memory, may operate at different voltage levels within SoCs. Level shifters facilitate the interface of memory components with the rest of the semiconductor. Level shifters are required in SoCs used in mobile devices and other applications focused on display technology. These level shifters allow for seamless interaction between SoCs and display technologies such as liquid crystal display (LCD) and organic light-emitting diodes (OLEDs), which may have different voltage needs. Level shifters are critical components in SoCs that handle mixed signals, which are integrated circuits with both analogue and digital components that must communicate with one another. It is possible that different components of portable or battery-powered equipment may require independent voltage levels. Level shifters are essential in these devices because they maximize the use of available power resources. Interfacing with sensors and peripherals running at multiple voltage levels

is a common requirement in SoC architectures designed for specific domains such as automotive, medical, or industrial applications. SoCs require the inclusion of level shifters to efficiently interface with the various radio frequency (RF) components in order to support the smooth integration of communication devices such as wireless transceivers. Level shifters are critical in enabling the integration of many voltage domains on a single chip, allowing for uninterrupted communication between system components. A level shifter is a crucial component in the development of inter-integrated circuit (I2C) communication protocols, as it helps ensure proper signal compatibility between devices with different voltage levels. I2C is a popular serial communication protocol used for connecting various integrated circuits within electronic systems.

The required larger chip area associated with the usage of a level shifter is a restriction found in some SoC systems. SoCs are semiconductor devices that include various components inside a singular integrated circuit; these components comprise central processing units (CPUs), graphics processing units (GPUs), memory units, communication interfacing units, and several other functional blocks. The use of a larger area by a single component, such as a level shifter, may impose limitations on the integration of other essential components or diminish the overall functioning of the chip. The optimization of the level shifter circuit is essential for designers to save power consumption while simultaneously meeting performance specifications. Level shifters' operational characteristics can vary depending on a number of factors, including the temperature at which they operate and the surrounding environmental conditions. The presence of extreme temperatures, humidity, and other environmental factors may potentially harm the circuit's stability and reliability.

Because of the low power needs of SoC applications, the semi-conductor industries often operate at voltages ranging from 0.1 V to 5 V. As integrated circuits become more complicated and demand more power, effective power supply solutions such as stacking and multiple VDD become more important. Modern SoC design has significant issues in obtaining the correct power consumption and latency. The need for efficient power delivery and low-latency solutions is growing, particularly as chip layouts become more complex. When each block within the system operates with a separate electrical supply, then a level shifter (LS) is required/essential to connect the output of one block to the input of the next block.

Addressing these challenges [1] not only increases the performance of SoCs but also offers potential for a wide range of applications, from mobile devices to high-performance computing. Enhancing power delivery efficiency [2] and decreasing latency [3,4] not only yield advantages for the semiconductor sector but also bear significance for the ongoing development of digital technology and energy conservation.

In a prior study [5], a high-speed LS circuit was developed through the utilization of complementary metal-oxide semiconductor (CMOS) and carbon-nano-tube field-effect-transistor (CNFET) technology. The utilization of the high-voltage threshold (HVT) and low-voltage threshold (LVT) stages was observed. The circuit demonstrated notable improvements in power and efficiency by employing a reduction in the number of transistors to 5, while also achieving a decrease in transmission delay to 4.95 ns. Wang et al. developed a LS [6] that was meant to have minimal space requirements and low leakage current. This approach employs a multi-layer pull-up and pull-down system to mitigate energy dissipation. The total area of this architecture was  $5.614 \mu\text{m}^2$ , and it was fabricated on 55 nm multi-threshold CMOS (MTCMOS) technology. When the input voltage was converted from 0.3 V to an output of 1.2 V, the power consumption was measured to be just 21.62 pW, and the time delay or latency was found to be 24.06 ns.

In [7], this model describes a system with a single translator that can translate impulses of different amplitudes. The circuit receives a pulse-shaped signal with a voltage of 3.3 V as input. Depending on the specific configuration, the circuit generates one of three impulses with voltages of 1.2 V, 1.8 V, or 2.5 V as output. Heng introduced a model [8] that illustrates the design and implementation of the MTCMOS approach for developing a level converter with a wide range of capabilities. An integrated mixed-threshold current reflection circuit

is used in the circuit to effectively reduce the occurrence of oscillation issues that were seen in earlier designs. The level converter exhibits the ability to convert a signal with an initial voltage of 1.2 V. The delay of this level converter is measured to be 17.86 ns, while its power consumption remains constant at 73.95 pW. Furthermore, numerous alternative low-voltage LS designs have been presented in the literature [9–11] as potential solutions for the implementation of energy-efficient pull-down and pull-up systems [12–14].

In reference [15], two conventional LS architectures are discussed: the current mirroring (CM) and the differential cascading voltage switching (DCVS) models. However, this approach is accompanied by significant power consumption when dealing with high-voltage input signals, hence making it less suitable for low-power devices. The authors in reference [16] present an LS that effectively converts a lower input voltage to high output voltage. This architecture design incorporates the MTCMOS method and the super-cut-off mechanism in order to mitigate power dissipation resulting from leakage. It also incorporates a performance-preserving positive feedback system. The level shifter exhibits a transmission delay of 70.77 ns and is capable of converting a voltage range of 0.3 V to 1.2 V at an input frequency of 1 MHz. The device operates with a consistent power consumption of 27.82 pW and occupies a compact footprint of just 7.79  $\mu\text{m}^2$ . According to the study referenced in [17], CM and DCVS are identified as the predominant types of LS. The utilization of CM configuration facilitates expedited conversion. Nonetheless, because leakage current through transistors at “high” input signal voltages results in significant static power consumption, it might not be appropriate for ultra-low power systems.

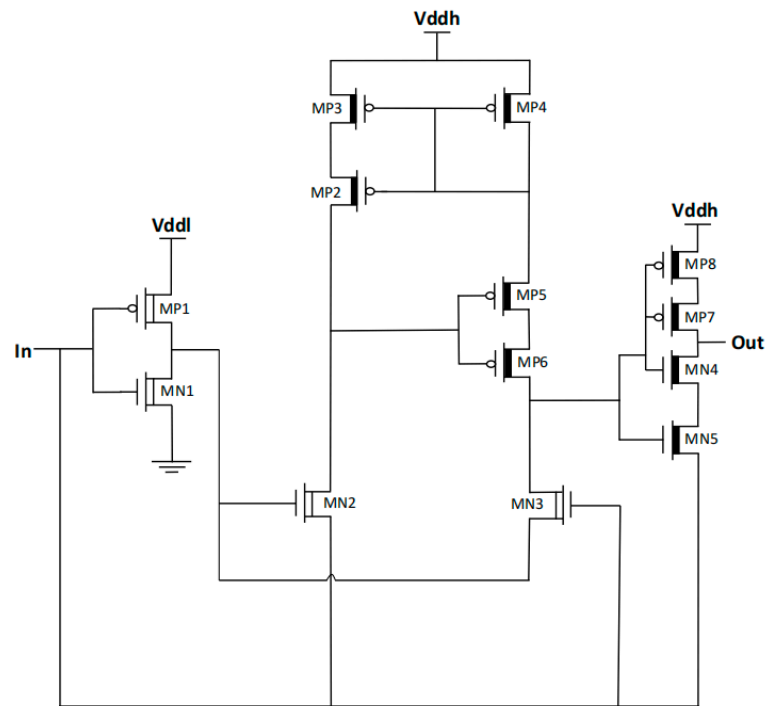
The utilization of efficient and energy-saving techniques [18–21] based on 180 nm technology and subsequent advancements has facilitated the improvement of chip area. Although they possess significant advantages in terms of space and energy, they may not be well suited for applications that require low latency. Our solution to this problem involved the use of a LS in conjunction with MTCMOS, super-cut-off mechanisms, and transistor stacking. Furthermore, we integrate inverters at both the input and output stages in conjunction with the super-cut-off mechanism. The implementation of this approach guarantees the achievement of low latency and efficient voltage switching.

## 2. Methods

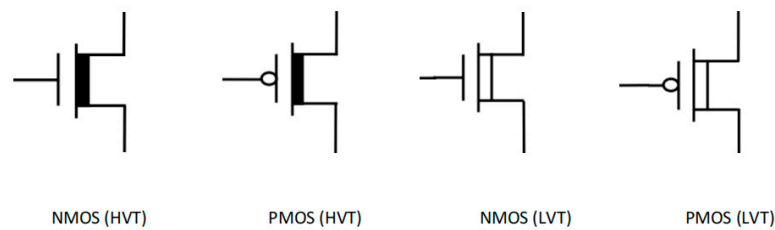
As shown in Figure 1, the proposed method employs MTCMOS technology, which employs transistors with two distinct threshold voltages (HVT and LVT), each with a length of 45 nm and a width of 120 nm. The input signal is fed into the input inverter (MP1 and MN1); we added a second inverter (MN5, MN4, MP7, and MP8) at the output. To translate the output voltage from low to high, we employed current mirror circuits. This design optimizes the LS's structure, using various methods such as MTCMOS (as seen in Figure 2), transistor stacking, and a super-cut-off mechanism. MTCMOS is an enhanced CMOS technology that reduces delays and maximizes energy savings by utilizing transistors with multiple threshold voltage levels. It achieves high switching speed and area optimization through the strategic use of sleeper transistors with optimized gate length, width, size, and body bias. Sleep transistors, typically high-threshold PMOS or NMOS, are employed to cut power to specific sections of a device. MTCMOS devices are known for their reduced power consumption during idle states and lower latency [22,23]. The circuit was developed with possible changes in the size and quantity of HVT and LVT transistors along with a super cut-off mechanism.

In typical CMOS technology [24], a single-threshold design restricts transistors to supplying electricity to circuitry that operates at a specific voltage. However, MTCMOS introduces multiple threshold devices like HVT and LVT. This allows both high- and low-voltage circuitry to be powered. In our proposed circuit, we use MTCMOS transistors, which include both HVT and LVT variants, offering flexibility to accommodate a range of voltage requirements. The decision was made to include MTCMOS technology in our design to simultaneously achieve a reduced physical size and enhanced power efficiency. In order to provide more precision, it was determined that the implementation of LVT would

be used for the transistors (MN1, MP1, MN2, MN3) whose gates were linked to either the input (In) or output of an input inverter (MP1 and MN1). The purpose of this action was to save space on the design. To mitigate power dissipation resulting from leakage, we opted to use HVT for the remaining components of the level shifter. Despite the fact that LVT-based transistors leak more current than HVT-based transistors, the implementation of the super-cut-off mechanism effectively reduces the amount of leakage when MN2 or MN5 is turned off.



**Figure 1.** Level-up shifter.



**Figure 2.** MTCMOS.

“Transistor stacking” is a straightforward technique that involves connecting multiple transistors in series. This configuration significantly reduces power leakage compared to using a single device. The reduction in leakage current when series transistors are turned off is known as the stack effect or self-reverse bias effect [25,26]. In our proposed circuit, we employed this method to minimize power lost due to leakage. It consists of two systems: the stacked pull-up (MP2, MP3, MP7, and MP8) and the super-cut-off pull-down (MN2, MN3, and MN5). In the proposed circuit, the source of MN1 is only connected to the ground, while the source of MN2, MN3, and MN5 is connected to the input signal of the level shifter; this enables the MN2, MN3, and MN5 transistors to enter super cut-off, minimizing power consumption. This approach was chosen to achieve high-speed performance while maintaining low standby electrical current. The proposed approach involves replacing the traditional pull-up transistor with a configuration of stacking pull-up transistors (MP2 and MP3) in the current-mirror circuit. However, the stacking pull-up

transistors (MP7 and MP8) and the super-cut-off transistors (MN5) are part of the output inverter's design to reduce current loss due to leakages. The sourcing nodes of MN2 and MN5 are electrically linked to the input signal. To identify the super-cut-off transistor state, we verified that the gate-to-source voltage ( $V_{gs}$ ) was substantially below the threshold voltage ( $V_{th}$ ). The transistor was essentially turned off in this condition, and leakage current is minimized. To reduce  $V_{gs}$  below the threshold voltage, the transistor source nodes (MN2 and MN5) were linked to the input signal. When the rising flip of the input signal "In" was completed, the  $V_{gs}$  of MN2 and MN5 were equal to  $-400$  mV.

As a consequence of this modification, the transistors MN2 and MN5 were effectively driven into the super-cut-off state upon deactivation, resulting in a substantial reduction in the current dissipated by leakage. The activation of both MN1 and MN3 occurred upon the attainment of a high state in the LS input signal. Subsequently, the voltage levels at both the output of the input inverter and the input of the output inverter were reduced. The MN2, MN3, and MN5 transistors simultaneously switch to super-cut-off mode at the same time.

Subsequently, the transistors MP7 and MP8 elevate the amplitude of the output signal (Out) until it reaches a high state. When the input voltage (In) of the level shifter is in a low state, the output of the input inverter is raised to low supply voltage (VDDL) by the MP1 component. During the same time frame, MN1 and MN3 experience disconnection. As a result of this, the MN5 component is responsible for making the level shifter's output almost identical to the input signal (In).

The system may be divided into subsystems and supplied with suitable voltages based on their performance requirements. It achieves high switching speed and area optimization through the strategic use of sleeper transistors with optimized gate length, width, size, and body bias. Sleep transistors, typically high-threshold PMOS or NMOS, are employed to cut power to specific sections of a device. The multi-VDD design methodology utilizes several supply voltage levels to energize different circuit blocks or subsystems inside a SoC. This technique involves dividing the design into distinct voltage domains, wherein each domain operates at an appropriate power supply voltage level based on its specific timing needs. Subsystems with low power consumption are operated using a VDDL, resulting in a decrease in speed performance. In contrast, subsystems that require high-speed operation are supplied with VDDH, leading to a decline in energy efficiency.

Figure 3 illustrates a conceptual representation of a Voltage LS (VLS) with several voltage supply levels (VDDH/VDDL). By using VLSs, which are buffering circuits facilitating the connection between voltage domains by converting high-voltage signals to low-voltage signals or vice versa, this approach achieves an optimal balance between power consumption and higher-speed functioning. The multi-VDD technique aims to reduce energy utilization in a level shifter by applying VDDL to non-essential blocks and VDDH to critical blocks. Nevertheless, when the low-voltage module establishes a connection with the high-voltage module, it produces a driving signal characterized by a lower voltage. The static current flow in the high-voltage domain is seen to grow as a result of the low voltage module's inability to drive it. In order to address this issue, level shifters are strategically positioned between the domains of low and high voltage in order to ensure the smooth functioning of the system. Level shifters play a crucial role in ensuring the accurate timing of signal transitions and effectively driving subsequent circuit blocks.

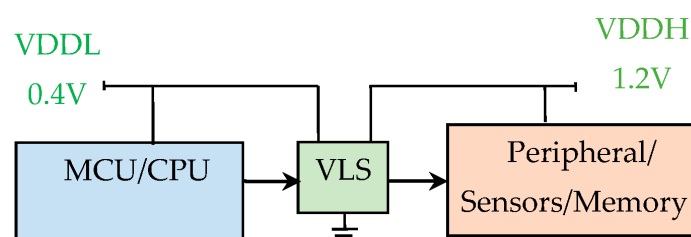
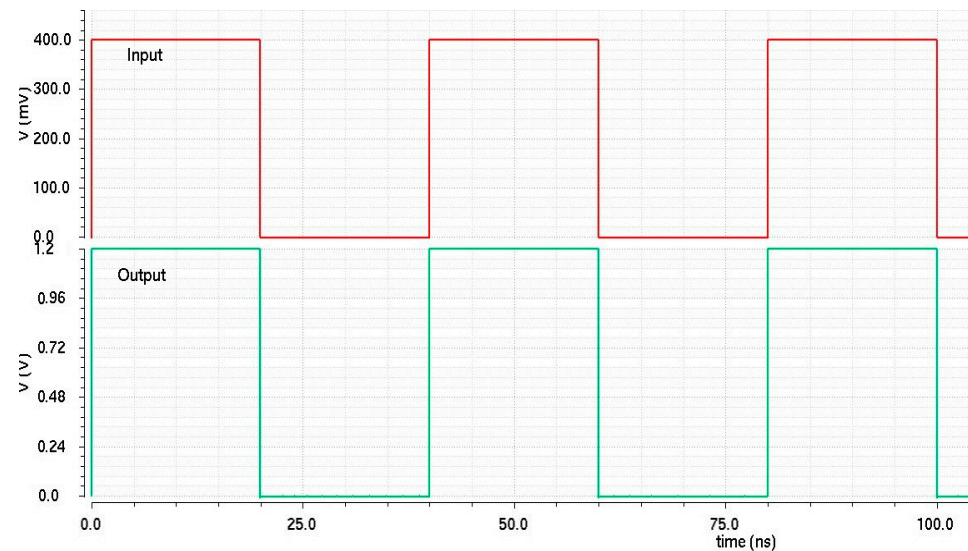


Figure 3. VLS up-conversion for nano-scale applications.



### 3. Results

The level shifter input and output waveform are shown in Figure 4. The circuit operates with an input voltage of 0.4 V and produces an output voltage of 1.2 V at a frequency of 1 MHz. Notably, both the input and output signals remained stable throughout the measurement duration. The propagation delay of a circuit is calculated as the interval of time between the application of an input and the subsequent switching of the output (measured at the point where the input–output transition reaches 50%).



**Figure 4.** Input (red) and output (green) waveform.

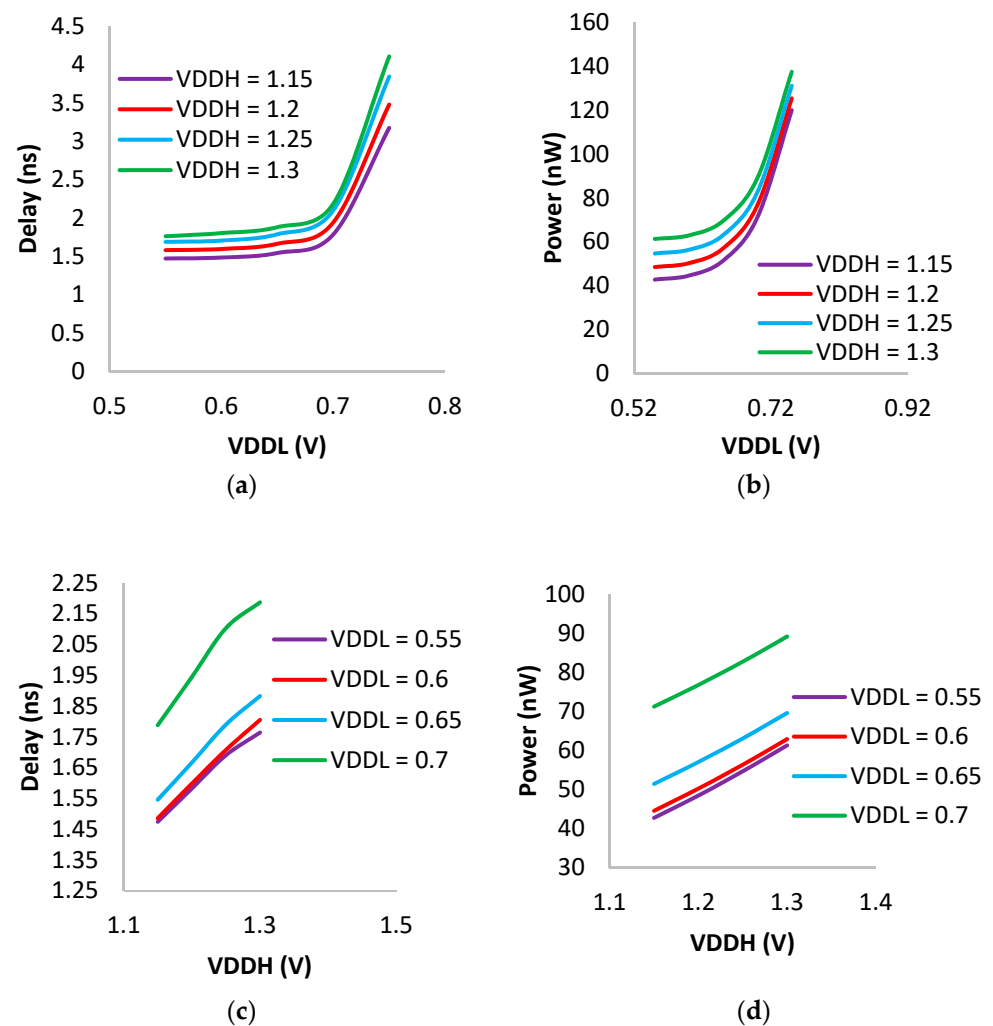
Power consumption, propagation delay, and area are the three important aspects of the chip design. To obtain the best design parameters for the level shifter, the proposed model's behavior under multi-VDD (Figure 5) and temperature changes (Figure 6) was studied. The circuit was optimized to deliver the best performance under the following parameters: VDDH of 1.2 V, VDDL of 0.65 V, and a room temperature of 27 °C.

The delay is calculated under different conditions to observe the behavior of the circuit. In Figure 5a, delay is assessed under various conditions by altering VDDL values while keeping VDDH constant. We can observe that delay remains constant initially and gradually increases in all scenarios. Although lower VDDL values may appear to be advantageous (delay is almost constant) at first, these advantages are dependent on their use within a specified operational range. Deviating from this range might result in compromised or poor performance. The circuit is designed to operate at a typical VDDL value of 0.65 V. Small variations in VDDL can have a pronounced impact on the effective  $V_{th}$  of transistors, influencing delay exponentially.

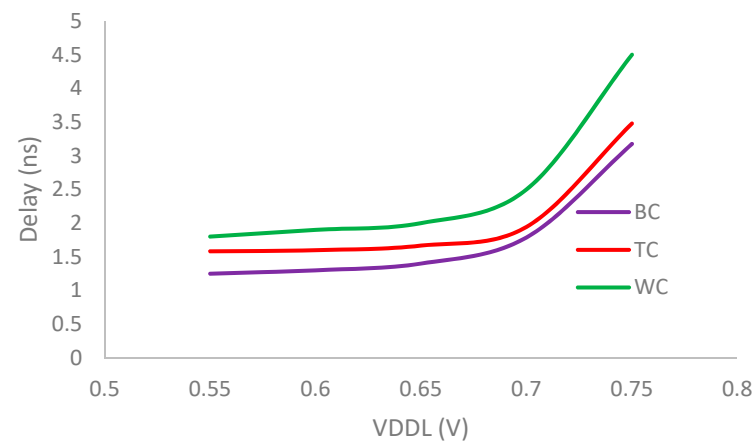
In Figure 5b, power consumption is evaluated by adjusting VDDL values while maintaining a constant VDDH. The findings demonstrate an exponential increase in power as VDDL is raised. Additionally, power consumption escalates with higher VDDH levels. The power consumption of level shifters is also affected by the existence of capacitive loads inside the circuit. The rise in VDDL has the potential to induce alterations in capacitive loads, hence influencing power consumption and contributing to the observed upward trajectory. Dynamic power is primarily caused by supply voltages and the discharging and charging of load capacitance. The power consumption has a positive correlation with the magnitude of the load [27].

The parasitic capacitances associated with the gate capacitance of the transistors contribute to the delay. The capacitive loading on the input and output nodes impacts the time it takes for the voltages to change during a logic level transition. Parasitic ca-

capacitances associated with transistor switching contribute to dynamic power loss during signal transitions.



**Figure 5.** Influence of VDDL and VDDH variations on delay and power consumption: (a) delay versus VDDL; (b) correlation between power consumption and VDDL; (c) relationship between delay and VDDH; (d) power behavior according to VDDH.



**Figure 6.** Delay in the case of various PVT corners.

Similarly, as shown in Figure 5c,d, delay and power are evaluated by adjusting VDDH at a constant VDDL. As depicted in Figure 5c, the delay demonstrates a consistent linear increase with each increment in VDDH.

A linear relationship between the increase in VDDH and the resulting increase in latency of a level shifter suggests that the level shifter circuit exhibits a direct correlation between propagation delay (latency) and VDDH. An increase in VDDH can lead to changes in the effective resistances and capacitances, resulting in a linear impact on the delay.

The power output of a level shifter exhibits a linear response to changes in VDDH while VDDL remains constant, as shown in Figure 5d. In a multi-VDD design, different voltage domains exist within the circuit. As VDDH increases, the voltage across the high-voltage transistors also increases. Since power is proportional to voltage, the power dissipation in the high-voltage domain increases linearly with VDDH.

The power consumption in circuits has a quadratic dependence on the supply voltage. The dynamic power dissipation is proportional to the square of the voltage. Therefore, even a moderate increase in VDDL can result in a more substantial increase in power consumption compared to an equivalent increase in VDDH.

The behavior of power concerning VDDH closely mirrors that of delay, demonstrating a linear rise that further escalates with increased VDDL; when the power output of a level shifter demonstrates a linear response solely to changes in VDDH while VDDL remains constant, it indicates the existence of a linear relationship between VDDH and power consumption.

Figure 6 shows a depiction of the propagation delay of the proposed LS for different process voltage–temperature (PVT) corners. The typical case (TC) scenario contains typical NMOS and PMOS devices at a temperature of 27 °C and a typical voltage of 1.2 V (VDDH). The worst-case scenario (WC) corner employs both slow NMOS and fast PMOS devices. A 10% increase in high voltage (VDDH = 1.32 V) and −40 °C temperature is also considered. Finally, the best-case (BC) scenario is a mix of fast NMOS and slow PMOS transistors operating at 125 °C with a 10% drop in high voltage (VDDH = 1.08 V). At a typical voltage of VDDL of 0.65 V, the delay in the cases of BC, TC, and WC is 1.4, 1.58, and 2 ns, respectively.

The impact of temperature on delay and power is evident. In Figure 7a, one can observe how delay changes with varying temperature values. It shows a slight decrease in delay with increasing temperature up to room temperature, after which it begins to rise. The temperature-induced increase in delay in a level shifter is a result of multiple inter-related factors, including changes in threshold voltage, carrier mobility, and parasitic capacitances. These factors collectively contribute to the degradation of the level shifter's performance as the temperature rises, leading to a longer delay in signal propagation.

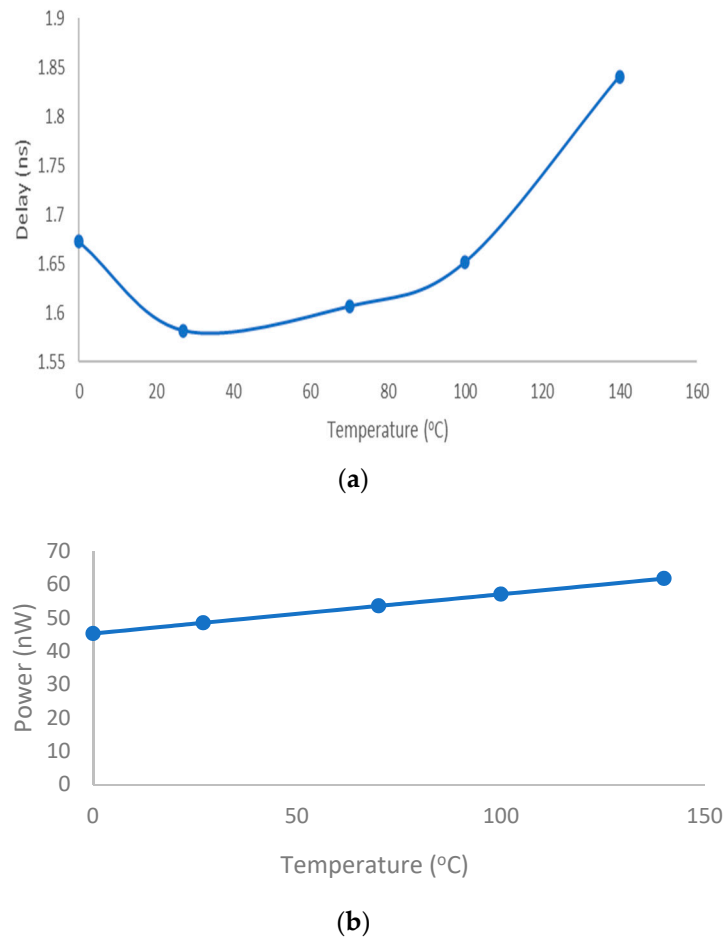
The measurement conditions in Figure 6 are a VDDL of 0.5 V and VDDH of 1.2 V. Figure 7b illustrates power consumption under different temperature conditions, where power increases slightly with rising temperatures. For optimal results, it is advisable to operate under low-temperature conditions, particularly room temperature.

Figure 8 shows the layout created for our proposed design using the Cadence tool with 45 nm technology. The circuit's area depends on various factors, including wire routing, metal widths, poly width, spacing of metal–poly connectors, the number of connections, and wire size. All these parameters influence the circuit's area. Despite having fewer transistors, an improper arrangement of the above parameters can lead to increased circuit area. Therefore, effective layout construction is crucial to maintain an optimized circuit.

A comparison of different previous works with the current model is given in Table 1. In terms of latency, our suggested architecture outperforms existing alternatives, achieving a remarkably low latency of approximately 1.58 ns, which is superior to any previous model. The proposed design also boasts a compact layout, occupying only 9.97  $\mu\text{m}^2$ . Even though this circuit uses less power than some earlier designs, its power-delay product reduction capabilities set it apart as the best in its class. The magnitude of leakage current when a transistor is in the super-cut-off state can be extremely low. In this state, the transistor is designed to be as close to fully turned off as possible, and the leakage current is minimized.



Stacking is used in pull-up and pull-down networks to lower total power consumption; the average power with and without stacking is 48.5 and 50.44 nW, respectively. We noticed an overall improvement in power consumption with the use of stacking in the circuit; the power consumption decreased by 4% when compared to the lack of stacking.



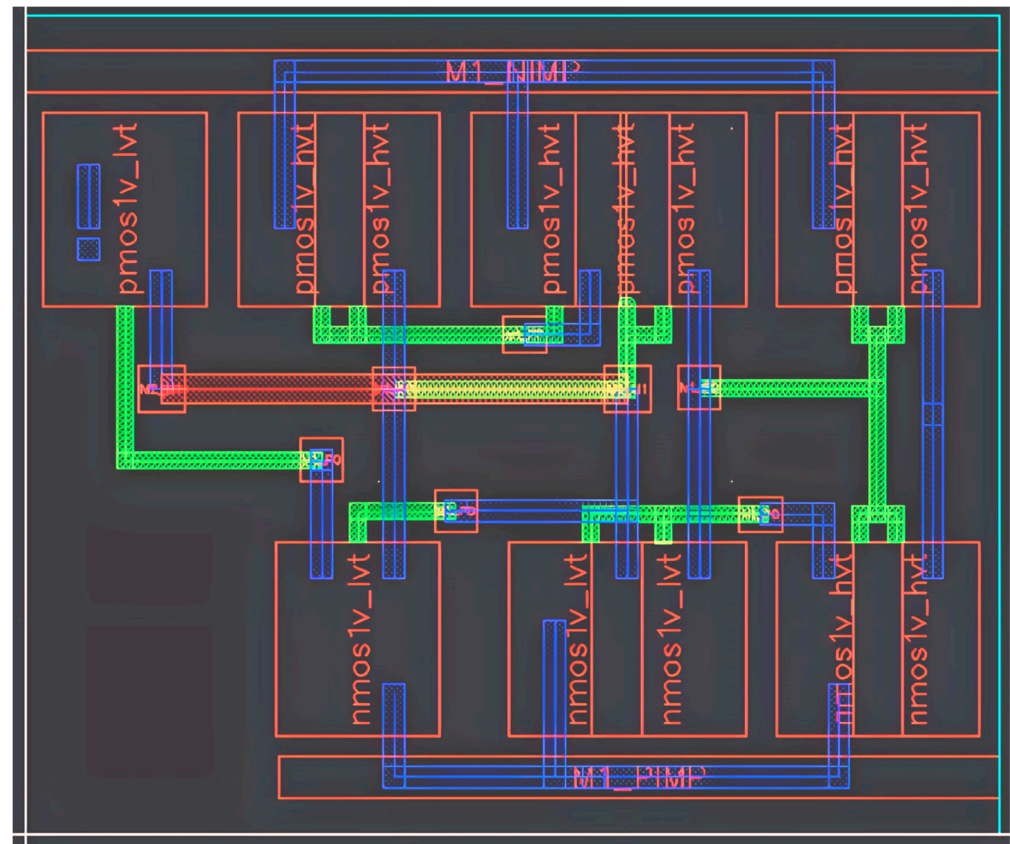
**Figure 7.** Influence of temperature variations on delay and power consumption: (a) delay versus temperature; (b) temperature effects on power.

**Table 1.** Comparison with previous work.

Parameter	Ref. [5]	Ref. [20]	Ref. [21]	Ref. [6]	Ref. [18]	This Work
Results	Pre-layout	Pre-layout	Pre-layout	Measured	Post-layout	Pre-layout
Tech (nm)	45	180	45	55	180	45
Delay (ns)	4.95	10	16.4	24.06	23.69	1.58
P.Static (W)	0.28n	70p	412p	21.62p	0.3n	1.2n
P.Avg. (nW)	4.4	2600	-	8.86	123.1	48.5
PDP	27.7	26,000	-	213.7	2916	76.73
VDDL (V)	0.25	0.4	0.2	0.3	0.6	0.65
VDDH (V)	1	1.8	1.2	1.2	1.8	1.2
Area ( $\mu\text{m}^2$ )	3.46	99.875	0.173	5.614	63	9.97

The main advantage of using a proposed VLS is that it facilitates communication and data exchange between different voltage domains. By allowing different parts of a system to operate at their optimal voltage levels, a VLS can contribute to energy efficiency. It enables the use of lower voltage levels in specific sections of the circuit, reducing overall power consumption. VLSs provide flexibility in system design and scalability. As new

components are added to a system, they can be designed to operate at their preferred voltage levels, and VLSs ensure compatibility with the existing system architecture.



**Figure 8.** Layout of the proposed design.

To further optimize the performance of the proposed circuit, consider implementing any of the subsequent alternatives: The dimensions of the level shifter circuit may have an effect on both the overall chip area and cost. The size of the transistors in the level shifter must be precisely optimized. By altering the widths and lengths of the transistors, one can achieve the desired delay while using less area. It is advised that the input-side inverter be replaced with a pass transistor to minimize the total circuit size. To enable efficient communication and smooth compatibility, the level shifter must adhere to voltage standards and signaling protocols that are compatible with the other components or devices with which it desires to communicate. Choose a conventional cell collection with higher cell density and smaller cell footprints. The use of enhanced-design standard cells in the level shifter circuit may result in overall space reductions. The use of proper placement strategies has the ability to reduce chip area by effectively reducing wire length and mitigating the influence of parasitic capacitance.

#### 4. Conclusions

Our research has successfully developed a compact level shifter based on a Wilson current mirror with minimal leakage current, utilizing MTCMOS, transistor stacking, and super-cut-off CMOS techniques. The level shifter excels in transforming low input voltages to a higher level (from 0.4 V to 1.2 V) with an impressive propagation delay of 1.5821 ns, accompanied by an average power consumption of 48.5 nW and a compact area of approximately  $9.9736 \mu\text{m}^2$ .

This work has notable implications for low-power computing designs, particularly in applications demanding ultra-low delay performance. It represents a significant step

forward in the field of level shifters, surpassing existing alternatives in terms of performance and efficiency.

Looking ahead, there are opportunities for further research, such as exploring the integration of our design in specific low-power applications and investigating optimizations for even more power-efficient solutions. Our research serves as a foundation for future advancements in ultra-low-power computing and opens the door to a range of innovative applications that require efficient level-shifting solutions.

**Author Contributions:** Conceptualization, M.V.S.; methodology, M.V.S. software, M.V.S.; validation, M.V.S.; formal analysis, M.V.S.; investigation, M.V.S.; resources, M.V.S.; data curation, M.V.S.; writing—original draft preparation, M.V.S.; writing—review and editing, M.V.S. and O.P.S.; visualization, O.P.S.; supervision, O.P.S.; project administration, O.P.S.; funding acquisition, O.P.S. All authors have read and agreed to the published version of the manuscript.

**Funding:** This research was partially supported by the project 38 PFE in the frame of the program PDI-PFE-CDI 2021.

**Data Availability Statement:** The data that support the findings of this study are available upon reasonable request from the authors.

**Conflicts of Interest:** The authors declare no conflict of interest.

## References

- Rivera-Barrera, J.P.; Muñoz-Galeano, N.; Sarmiento-Maldonado, H.O. SoC Estimation for Lithium-ion Batteries: Review and Future Challenges. *Electronics* **2017**, *6*, 102. [\[CrossRef\]](#)
- Shihab, M.M.; Agrawal, V. Energy Efficient Power Distribution on Many-Core SoC. In Proceedings of the 32nd International Conference on VLSI Design and 18th International Conference on Embedded Systems (VLSID), Delhi, India, 5–9 January 2019; pp. 488–493.
- Guha, K.; Saha, D.; Chakrabarti, A. Self Aware SoC Security to Counteract Delay Inducing Hardware Trojans at Runtime. In Proceedings of the 30th International Conference on VLSI Design and 16th International Conference on Embedded Systems (VLSID), Hyderabad, India, 7–11 January 2017; pp. 417–422.
- Sheng, D.; Lai, H.-F.; Chan, S.-M.; Hong, M.-R. A High Resolution On-Chip Delay Sensor with Low Supply-Voltage Sensitivity for High-Performance Electronic Systems. *Sensors* **2015**, *15*, 4408–4424. [\[CrossRef\]](#) [\[PubMed\]](#)
- Vidhyadharan, A.S.; Satheesh, A.; Pragna, K.; Vidhyadharan, S. High-Speed and Area-Efficient CMOS and CNFET-Based Level-Shifters. *Circuits Syst. Signal-Process.* **2022**, *41*, 4649–4670. [\[CrossRef\]](#)
- Wang, P.; Wang, X.; You, H.; Yin, J.; Zhan, Y.; Qiao, S.; Zhou, Y. Ultra-low leakage and small-area level shifter based on super-cut-off mechanism. *AEUE-Int. J. Electron. Commun.* **2022**, *146*, 154085. [\[CrossRef\]](#)
- Karimi, M.; Ali, M.; Hassan, A.; Sawan, M.; Gosselin, B. A Reconfigurable Single-supply Multiple-level Down-shifter for System-on-Chip Applications. In Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS), Daegu, Republic of Korea, 22–28 May 2021; pp. 1–5. [\[CrossRef\]](#)
- You, H. An Energy efficient level shifter for ultra low voltage digital LSIs. *IEEE Trans. Circuit Syst. II* **2020**, *67*, 3357–3361. [\[CrossRef\]](#)
- Late, E.; Ytterdal, T.; Aunet, S. An energy efficient level shifter capable of logic conversion from sub-15 Mv to 1.2 V. *IEEE Trans. Circuits Syst. II Express Briefs* **2020**, *67*, 2687–2691. [\[CrossRef\]](#)
- Garcia, J.G.; Montiel-Nelson, J.A.; Nooshabadi, S. High Performance CMOS Level up Conversion for Systems with Low-Voltage Power Supply. In Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS), Sapporo, Japan, 26–29 May 2019; pp. 1–5.
- Cai, Q.; Ji, Y.; Ma, C.; Li, X.; Zhou, T.; Zhao, J.; Li, Y. An Ultra-Low-Voltage Energy-Efficient Dynamic Fully-Regenerative Latch-Based Level-Shifter Circuit with Tunnel-FET & FinFET Devices. In Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS), Daegu, Republic of Korea, 22–28 May 2021; pp. 1–5.
- Sobhan Bhuiyan, M.A.; Hossain, M.R.; Minhad, K.N.; Haque, F.; Hemel, M.S.K.; Md Dawi, O.; Ibne Reaz, M.B.; Ooi, K.J.A. CMOS Low-Dropout Voltage Regulator Design Trends: An Overview. *Electronics* **2022**, *11*, 193. [\[CrossRef\]](#)
- Lai, L.F.; Ramiah, H.; Tan, Y.C.; Lai, N.S.; Lim, C.C.; Chen, Y.; Mak, P.I.; Martins, R.P. Design Trends and Perspectives of Digital Low Dropout Voltage Regulators for Low Voltage Mobile Applications: A Review. *IEEE Access* **2023**, *11*, 85237–85258. [\[CrossRef\]](#)
- Wang, C.; Ji, Y.; Ma, C.; Cai, Q.; Qi, L.; Li, Y. An Ultra-Low-Voltage Level Shifter with Embedded Re-Configurable Logic and Time-Borrowing Latch Technique. *IEEE Access* **2021**, *9*, 79904–79910. [\[CrossRef\]](#)
- Yin, J.; Yuan, J.; You, H.; Peng, W.; Qiao, S. A fast and low-power level shifter for multisupply voltage designs. *IEICE Electron. Express* **2020**, *17*, 20200243. [\[CrossRef\]](#)
- You, H.; Yuan, J.; Tang, W.; Yu, Y.; Qiao, S.; Hei, Y. An ultra low leakage energy efficient level shifter with wide conversion range. *IEICE Electron. Express* **2019**, *16*, 20190507. [\[CrossRef\]](#)

17. Mukherjee, B.; Ghosal, A. An Area Efficient Sub-threshold Voltage Level Shifter using a Modified Wilson Current Mirror for Low Power Applications. *IETE J. Res.* **2022**, *68*, 559–565. [[CrossRef](#)]
18. Kabirpour, S.; Jalali, M. A Low-Power and High-Speed Voltage Level Shifter Based on a Regulated Cross-Coupled Pull-Up Network. *IEEE Trans. Circuits Syst. II Express Briefs* **2019**, *6*, 909–913. [[CrossRef](#)]
19. Maroof, N.; Sohail, M.; Shin, H. A fast and energy-efficient two-stage Level shifter using the controlled Wilson Current Mirror. *Automatika* **2018**, *58*, 473–478. [[CrossRef](#)]
20. Rezaei, N.; Mirhassani, M. An efficient high speed and low power voltage-level shifter. *Int. J. Electron. Commun.* **2021**, *138*, 153857. [[CrossRef](#)]
21. Rajendran, S.; Chakrapani, A. A 16 ns, 28 fJ Wide-Range Subthreshold Level Converter Using Low-Voltage Current Mirror. *Circuits Syst. Signal Process.* **2021**, *40*, 1479–1495. [[CrossRef](#)]
22. Saxena, S.; Akashe, S. High performance CMOS current comparator using MTCMOS technique design. In Proceedings of the Innovative Applications of Computational Intelligence on Power, Energy and Controls with Their Impact on Humanity (CIPECH), Ghaziabad, India, 28–29 November 2014; pp. 345–349.
23. Gour, S.; Soni, G.K. Reduction of Power and Delay in Shift Register using MTCMOS Technique. In Proceedings of the 4th International Conference on Trends in Electronics and Informatics (ICOEI) (48184), Tirunelveli, India, 15–17 June 2020; pp. 202–206.
24. Naeini, M.M.; Dass, S.B.; Ooi, C.Y. The Design and Implementation of a Low-Power Gating Scan Element in 32/28 nm CMOS Technology. *J. Low Power Electron. Appl.* **2017**, *7*, 7. [[CrossRef](#)]
25. Oliveira, A.C.; Cordova, D.; Klimach, H.; Bampi, S. A 0.12–0.4 V, Versatile 3-Transistor CMOS Voltage Reference for Ultra-Low Power Systems. *IEEE Trans. Circuits Syst. I Regul. Pap.* **2018**, *65*, 3790–3799. [[CrossRef](#)]
26. Rodovalho, L.H.; Ramos Rodrigues, C.; Aiello, O. Self-Biased and Supply-Voltage Scalable Inverter-Based Operational Transconductance Amplifier with Improved Composite Transistors. *Electronics* **2021**, *10*, 935. [[CrossRef](#)]
27. Boshetty, P.; Gurram, U.; Panati, S.R.; Beyyani, D.D. Designing a level shifter to enhance the performance suitable for low power applications. In Proceedings of the 2017 International Conference on Electrical, Electronics, Communication, Computer, and Optimization Techniques (ICECCOT), Mysuru, India, 8–9 September 2017; pp. 1–7.

**Disclaimer/Publisher’s Note:** The statements, opinions and data contained in all publications are solely those of the individual author(s) and contributor(s) and not of MDPI and/or the editor(s). MDPI and/or the editor(s) disclaim responsibility for any injury to people or property resulting from any ideas, methods, instructions or products referred to in the content.