

Article

A Basic Design Tool for Grid-Connected AC–DC Converters Using Silicon Carbide MOSFETs

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Abstract: The design and optimization of power converters is a key factor in the growth and development of the power electronics field. However, the process of designing a power converter is not straightforward, and engineers often rely on experience and intuition, sometimes requiring time-consuming computer simulations. This paper presents a tool for the basic design of grid-connected AC–DC converters. The design tool takes specifications and operating conditions for two-level and three-level NPC converter topologies and derives a draft design. The tool calculates the input filter’s electrical parameters, the converter’s losses, the temperature rise of the power semiconductor devices, and the ripple current and voltage of the DC-link capacitor. In order to validate the proposed design tool, four AC–DC converters using SiC MOSFETs were designed. Based on the design results, simulation models and prototypes were fabricated to verify the performance and confirm that the proposed design tool can be used in the basic design process of converters.

Keywords: AC–DC converter; grid-connected; automated design



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1. Introduction

As the field of power electronics continues to evolve, the design and optimization of power converters is a key factor in the efficient conversion and utilization of energy. Power converters in various forms, such as AC–DC converters and DC–DC converters, play an important role in power management, motor control, and more in a variety of applications such as renewable energy systems, electric vehicles, industrial automation, and home appliances. The ability to design these power converters precisely and efficiently is crucial for meeting the energy efficiency, reliability, and sustainability requirements of the ever-evolving energy industry [1].

However, the process of designing a power converter is far from simple. There are complex tradeoffs between design features such as the power circuit structure, control scheme, and switching frequency and performance metrics such as efficiency, voltage ripple, and current ripple. Engineers designing power converters often rely on experience and intuition, and in some cases, complex computer simulations, to achieve optimal results. Even experienced professionals can find it difficult to design with new converter topologies, control schemes, etc., and it can take a lot of trial and error to learn how to do it, especially for newcomers to the field [2,3].

To solve this problem, studies have been conducted on procedures and methods for designing various types of power converters. References [4–6] present step-by-step procedures for designing power converters with specific converter topologies or introduce tools that can assist in the design. These works are mainly aimed at finding the optimal design point to achieve the targeted performance metrics when the basic design of the power converter is already completed. However, this approach can be difficult for someone not already familiar with the design of this type of converter. Recently, methods using artificial intelligence (AI) have been studied to automate and reduce the reliance on experts

in the converter and controller design phase [7–10]. These methods are well suited for use in the optimization design phase for specific target systems. However, AI-based design methods have the disadvantage of requiring simulations under various specifications and operating conditions to collect data, and the selection of appropriate training methods and the training process may require a considerable amount of resources. Alternatively, basic power converter design tools are available, often provided by power semiconductor manufacturers [11,12]. However, the applicable converter topologies are limited, and device selection is also limited by the only components manufactured by the design tool vendor.

To address these issues, this paper introduces a general converter design tool for power converter design. The research project “Development of High Efficiency Power Converter based on Multidisciplinary Design and Optimization Platform”, funded by the Korea Institute of Energy Technology and Planning (KETEP), aims to build and operate an open web-based design tool for various power conversion systems based on wide-band-gap (WBG) semiconductors [13]. The design tool proposed in this paper is intended to be used in the basic design phase and is intended to quickly check feasibility or to quickly see how a particular performance varies as a function of parameter variation. The intention is to save the user of the design tool the effort of calculating formulas or building simulation models by hand. The tool is a synthesis of state-of-the-art research and practical engineering expertise and aims to simplify and popularize the process of power converter design and optimization. It provides engineers and researchers with an intuitive and user-friendly interface, allowing them to efficiently explore different design outcomes with a large number of degrees of freedom. It enables them to optimize the design parameters and ultimately deliver a high-performance solution for their specific needs. These design tools can help accelerate the development of power conversion systems, foster innovation, and enable the rapid adoption of new technologies. Furthermore, they have the potential to popularize power conversion design knowledge. The popularization of this knowledge can play an important role in the development of new technologies and paving the way for a more sustainable and efficient future in power electronics.

This paper introduces a general power conversion design tool for grid-connected AC–DC converters as part of the general converter design tool. The design tool developed requires the ability to allow the user to select different types of components available on the market during the design process. For this purpose, it is difficult to use data that must be obtained through complex experiments, and it is possible to use only the level of information disclosed in the datasheets provided by the manufacturers of the devices. The proposed design tool also aims to have simple formulas and design procedures so that they can be used in a lightweight web-based design tool.

The proposed design tool primarily tackles the complexity inherent in power converter design. While traditional design methods heavily rely on complex computer simulations, the proposed tool simplifies this aspect, allowing for faster, more rapid, and more accessible design iterations. By making the design process more accessible and less dependent on deep expertise, the proposed tool helps to popularize power converter design knowledge, which is crucial for promoting innovation in the field.

In the next section, the procedure for the basic system design of an AC–DC converter is presented, and the formulas used in each design step are derived. Based on the proposed design procedure, the design of converters of various specifications was carried out, and simulation models and prototypes were produced based on the designed parameters to verify the results of the design tool.

2. Design Procedures

This paper presents a design tool for grid-connected three-phase AC–DC converters using SiC MOSFETs among various types of power conversion devices. The design tool aims to facilitate the drafting of designs by engineers with little experience in converter design. Figure 1 shows the design procedure. Viewing the converter as an electrical circuit composed of lumped elements, the basic specifications, such as the input and

output voltages, capacity, and converter topology, are first selected. Limits are set on the efficiency, voltage and current ripple, and temperature rise of the semiconductors, and the switching devices are selected. The input parameters include operating conditions such as the switching frequency and power factor, along with the previously selected items. Based on the input parameters, the tool calculates the ripple of the input current, the voltage and current ripple of the DC-link, derives the electrical parameters of the input filter and the DC-link capacitor, and calculates the converter loss and temperature rise to check whether the limit conditions are met.

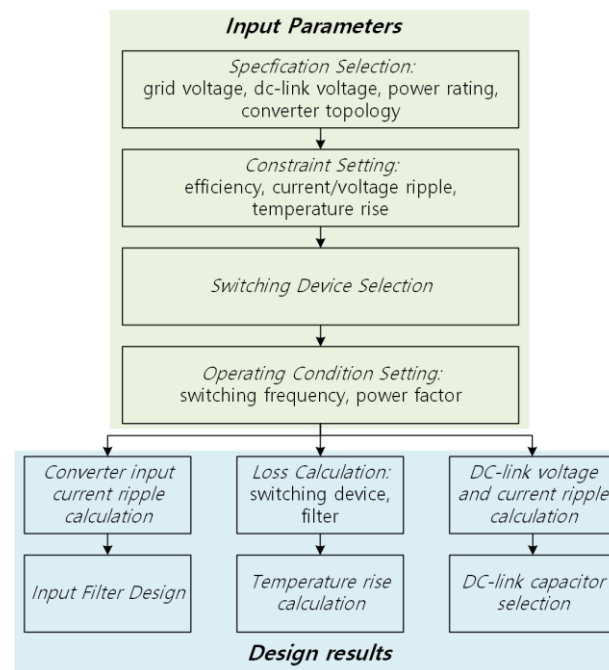


Figure 1. Grid-connected AC–DC converter design procedure.

However, this tool is intended for use in the basic design phase of a converter. In order for the web-based design tool to display design results quickly, the design procedure is based on simple formulas, and a certain amount of error is allowed. To develop a real product-level converter, more detailed design steps are required. The component-level design of passive devices, such as inductors used in converters, component placement and mechanical structure design for power density optimization, and the electromagnetic field analysis and heat distribution analysis, which require finite element analysis, are not covered in this paper. The process and formulas used in the design tool are as follows.

2.1. Input Filter Design Procedure

In a grid-connected AC–DC converter, the purpose of the input filter is to reduce current harmonics at the input side caused by voltage harmonics generated by PWM switching. As an input filter circuit, a simple inductor or an LCL filter consisting of two inductors and one capacitor is commonly used. The design tool in this paper exploits an LCL filter that has high harmonic rejection performance per unit inductance. Figure 2 shows the structure of the AC–DC converter and the LCL filter discussed in this paper. L_c and L_g represent the converter-side and grid-side inductors, respectively, and the filter capacitor, C_f , is connected in series with the damping resistor, R_d . The power stack is represented by a three-phase, two-level (2L) voltage-type inverter structure, which assumes the use of a three-phase, two-level or three-level (3L)-NPC converter in this paper.

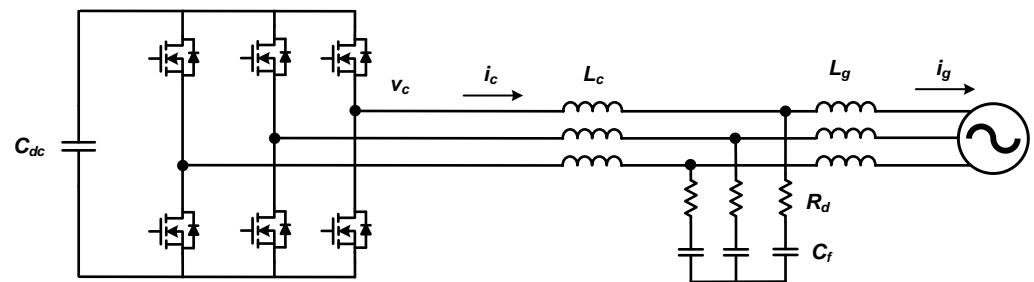


Figure 2. Grid-connected AC–DC converter structure with LCL filter.

Ignoring the effect of damping resistors in the converter structure of Figure 2, the relationship between voltage harmonics and current harmonics can be expressed as follows.

$$\frac{i_g(s)}{v_c(s)} = \frac{1}{s^3 L_c L_g C_f + s(L_c + L_g)}, \quad (1)$$

where i_g is the grid-side current and v_c is the output voltage at the converter side. The order-specific harmonics of the output voltage due to the switching of the converter can be calculated analytically [14]. With the limits of the target harmonic currents for each order, the input filter can be designed using the relationship in (1).

Tables 1–3 show the current harmonic limits by order of the current harmonic regulations IEEE-519 [15] and IEEE-1547 [16], which are widely used in designing grid-connected AC–DC converters. Studies on designing input filters have used the relationship in (1) to select input filter parameters that ensure that the voltage harmonics caused by the PWM of the converter do not exceed the current harmonic limits of each regulation [17,18].

Table 1. Current harmonic limits according to the IEEE 519 standard [15].

Maximum Harmonic Current Distortion in Percent of I_L						
Individual Harmonic Order (Odd Harmonics) ^{a,b}						
I_{sc}/I_L	$3 \leq h < 11$	$11 \leq h < 17$	$17 \leq h < 23$	$23 \leq h < 35$	$35 \leq h \leq 50$	TDD
$< 20^c$	4.0	2.0	1.5	0.6	0.3	5.0
$20 < 50$	7.0	3.5	2.5	1.0	0.5	8.0
$50 < 100$	10.0	4.5	4.0	1.5	0.7	12.0
$100 < 1000$	12.0	5.5	5.0	2.0	1.0	15.0
> 1000	15.0	7.0	6.0	2.5	1.4	20.0

^a Even harmonics are limited to 25% of the odd harmonic limits above. ^b Current distortions that result in a dc offset, e.g., half-wave converters, are not allowed. ^c All power generation equipment is limited to these values of current distortion, regardless of the actual I_{sc}/I_L , where I_{sc} = maximum short-circuit current at PCC. I_L = maximum demand load current (fundamental frequency component) at PCC. TDD = total demand distortion (RSS), harmonic current distortion in % of maximum demand load current (15 or 30 min demand). PCC = point of common coupling.

Table 2. Odd harmonic current distortion limit in percent of rated current (I_{rated}) ^a according to IEEE 1547 [16].

Individual Odd Harmonic Order, h	h < 11	$11 \leq h < 17$	$17 \leq h < 23$	$23 \leq h < 35$	$35 \leq h < 50$	Total Rated Current Distortion (TRD)
Percent (%)	4.0	2.0	1.5	0.6	0.3	5.0

^a I_{rated} = the DER unit rated current capacity (transformed to the RPA when a transformer exists between the DER unit and the RPA).

Table 3. Even harmonic current distortion limit in percent of rated current (I_{rated})^a according to IEEE 1547 [16].

Individual Even Harmonic Order, h	$h = 2$	$h = 4$	$h = 6$	$8 \leq h < 50$
Percent (%)	1.0	2.0	3.0	Associated range specified in Table 2

^a I_{rated} = the DER unit rated current capacity (transformed to the RPA when a transformer exists between the DER unit and the RPA).

However, this approach may not be appropriate for converters using SiC MOSFETs. As shown by the relationship in (1), harmonics in the grid current are caused by harmonics in the output voltage due to the PWM operation of the converter. The output voltage harmonics can be roughly divided into two classes according to their order: higher-order harmonics around multiples of the PWM switching frequency and lower-order harmonics corresponding to multiples of the fundamental wave, such as the 5th, 7th, 11th, etc. The higher-order voltage harmonics can be calculated analytically according to the PWM method by obtaining the magnitude of the harmonic voltage of each order, and filter parameters can be designed accordingly to limit the harmonic current of that order to a target value or less.

However, higher-order harmonics often account for a smaller proportion of the total current harmonic component generated by a grid-tied converter than lower-order harmonics. This is because higher-order harmonics have higher frequencies and are more easily attenuated by the input filters. This is especially true for converters using SiC MOSFETs, which often have switching frequencies of tens of kHz or more. Furthermore, popular grid input current harmonic regulations, IEEE 519 [15] and IEEE 1547 [16], limit the harmonic frequency to no more than the 50th order of the fundamental wave. For converters using SiC MOSFETs, most have switching frequencies above 20 kHz, so the higher-order harmonics associated with the switching frequency are well beyond the 50th order when referenced to the typical grid frequency of 60 Hz, which is outside the harmonic regulation criteria.

When using input filters to satisfy grid current harmonics regulations, it is then necessary to design them with low-order current harmonics in mind, but it is difficult to accurately calculate the magnitude of the voltage harmonics that cause low-order current harmonics.

Low-order output voltage harmonics are due to the non-ideal output characteristics of the converter, such as dead time and a voltage drop across switching elements, and are difficult to obtain analytically. In addition, for converters using SiC MOSFETs with fast switching frequencies, harmonic current controllers can be used to significantly suppress low-order harmonics [17]. In practice, harmonic current controllers are often used, which can lead to overly large filter designs if their effects are not considered. However, the harmonic control performance of the controller is also difficult to accurately estimate at the filter design stage.

In this paper, an input filter design method based on limiting the maximum value of the ripple of the converter-side current below a certain value is used, rather than limiting the grid current harmonics below a certain value according to the regulations of [15,16], etc. The design procedure of the input filter is shown in Figure 3, and the detailed design process is as follows.

1. Select system specifications and operating conditions:
Select the grid voltage, grid frequency, converter type (2L or 3L-NPC), switching frequency, DC-link voltage, and rated current.
2. Calculate ripple current and select converter side inductance:
Set the converter-side ripple current limit. Select the limit value of the peak-to-peak amplitude of the current ripple relative to the rated current and calculate the converter-side inductor value that satisfies the ripple current according to the operating conditions. The peak-to-peak amplitude of the ripple current generated by the

converter is determined by the operating conditions, and the instantaneous phase angle and can be expressed as (2) [18].

$$i_{pp} = \frac{V_{dc} T_s}{2L_c} r(m, \theta), \quad (2)$$

where V_{dc} is the DC-link voltage, T_s is the switching period, and $r(m, \theta)$ is a function of the voltage modulation index (m) and the output voltage phase angle (θ). The magnitude of the instantaneous current ripple depends on the phase angle, but the proposed method calculates the magnitude of the current ripple based on the output voltage at a phase angle of 90° . In general, the power factor of a grid-connected converter is close to unity, so the output voltage and current are almost in-phase, and the magnitude of the current flowing in the converter is maximized around 90 degrees. Therefore, when considering the maximum current flowing through the converter due to current ripple, it is appropriate to base the design on the value when the phase angle is 90° . The converter-side inductance (L_c) value that satisfies the magnitude of the ripple current can be selected by using (2).

3. Select capacitance and grid-side inductance:

The larger the capacitor of the LCL filter, the better it can absorb the converter's ripple current and reduce the harmonics of the grid-side current. However, the capacitor in the input filter introduces reactive power at the grid side and changes the grid side power factor. Typically, the reactive power flowing into the capacitor is limited to 2–5% of the apparent power in the design of the input filter [19]. The proposed design tool takes the reactive power value of the capacitor as input and selects the capacitor divisor of the corresponding filter. The formula for selecting the capacitance value is shown in (3).

$$C_f = \frac{S}{3\omega V_{ph}^2} R, \quad (3)$$

where S is the apparent power of the converter, ω is the frequency of the grid, V_{ph} is the phase voltage of the grid, and R is the ratio of the reactive power to the apparent power. In studies dealing with LCL filter design, the values of the grid-side inductance and the converter-side inductance are often chosen to be equal. This is because, when the resonant frequency of the LCL filter is first determined, equalizing the two inductance values results in the smallest magnitude of the total inductance [20], i.e., the harmonics of the grid current can be reduced the most with the same inductance value. However, in this paper, the filter is designed based on the ripple current on the converter side, not the current harmonics delivered to the grid. In the case of converters using SiC MOSFETs, the low-order harmonics that contribute most to the grid current harmonics can be significantly suppressed by current controllers, so the proposed method focuses more on the converter-side inductor in the total inductance used in the input filter. In this paper, the grid-side inductance is selected as one-third of the converter-side inductance.

4. Check the resonant frequency of the input filter:

The resonant frequency (f_{res}) of the input filter should be less than one-half of the sampling frequency (f_s) according to the Nyquist sampling theory, and it should be higher than the bandwidth (f_b) of the current controller to avoid affecting the current control behavior [21].

$$f_b < f_{res} < \frac{1}{2} f_s \quad (4)$$

Finally, check whether the parameters of the input filter selected satisfies (4), and if not, adjust the capacitance value so that the resonant frequency satisfy the limitation of (4).

5. Select damping resistor:

The LCL filter theoretically has zero impedance at its resonant frequency. The damping resistor is used to provide impedance at this time to suppress the oscillation of the current at the resonant frequency. For this purpose, the value of the damping resistor is designed to be similar to the impedance of the capacitor connected in series at the resonant frequency [22], and in this paper, it is selected as one-third of the impedance of the capacitor at the resonant frequency.

$$R_d = \frac{1}{3} \frac{1}{2\pi f_{res} C_f} \quad (5)$$

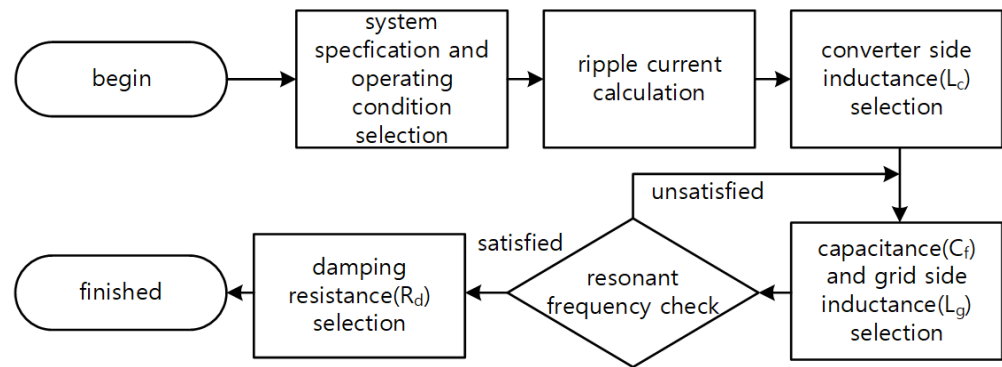


Figure 3. Input filter design procedure.

2.2. Calculating Losses and Temperature Rise

The losses of the converter covered in this paper are composed of the losses of the power semiconductor and the losses of the input filter. The losses are calculated based on the given converter specifications and operating conditions, and the junction temperature is estimated using the thermal resistance information of the heat sink where the power semiconductor is installed.

The losses of the power semiconductor can be divided into conduction losses and switching losses. The conduction losses of SiC MOSFETs and diodes are calculated using the R_{ds} , R_d , and V_{f0} information in the datasheet, as shown in (6) and (7), respectively, and the switching losses of SiC MOSFETs are calculated using the datasheet loss data, as expressed in (8).

$$P_{cond} = R_{ds} I_{rms}^2 \quad (6)$$

$$P_{cond,diode} = V_{f0} I_{avg} + R_d I_{rms}^2 \quad (7)$$

$$P_{on/off} = f_{sw} \frac{s(\theta)}{2\pi} \frac{V_{dc}}{V_{test}} E_{on/off}(I_{avg}), \quad (8)$$

where R_{ds} is the equivalent resistance when the SiC MOSFET is turned on and R_d and V_{f0} are the equivalent resistance and threshold voltage when the diode is turned on, respectively. I_{rms} is the rms value of the current flowing in each power semiconductor device, f_{sw} is the switching frequency, $s(\theta)$ is duration when the current is flowing in that semiconductor device, I_{avg} is the average current in the current flowing section, V_{dc} is the DC-link voltage, V_{test} is the test voltage indicated in the switching loss data in the datasheet, and $E_{on/off}$ is the loss function extracted from the on and off switching loss data in the datasheet. The gate resistance is inputted by the user and reflected in the determination of R_{ds} and $E_{on/off}$.

Equation (8) uses the average current in the conducting section to calculate the switching losses under the assumption that the current flowing in the device at the time of switching is proportional to the switching losses. In practice, the two are not exactly proportional. In general, for SiC MOSFETs, there is a slight exponential increase in switching

losses as the current flowing through the device at the time of switching increases. As a result, the switching losses calculated from the average current tend to be smaller than the actual switching losses at higher load currents, leading to calculation errors. However, since the design tool presented in this paper is intended to be used in the basic design phase for feasibility checks, this level of error can be justified. Overcurrent and overvoltage due to parasitic components like stray inductance also affect the switching loss [23]. However, the parasitic component cannot be anticipated during the basic design phase, so it is not reflected.

Figure 4 shows the leg structure of the two-level and three-level converters covered in this design tool, and the output voltage command and output current of the converter are shown in (9) and (10).

$$v_{out} = V \cos(\omega t), \quad (9)$$

$$i_{out} = I \cos(\omega t - \varphi), \quad (10)$$

where V and I represent the magnitude of the output voltage command and output current, respectively, ω is the frequency of the grid, and φ is the load angle. In order to calculate the loss of each power semiconductor device, the operating region can be divided into four according to sign of output voltage command and output current. Figure 5 shows the four operating areas with the state of the output voltage command and current. Table 4 summarizes the current-carrying devices and devices where switching losses occur in each operating area for 2L and 3L-NPC converters. Using Figure 5 and Table 4, it is possible to calculate the rms value of the current flowing through each power semiconductor element, the average current in the section where the current flows, and substitute the values into (6)–(8) to calculate the loss for each element in each converter, as shown in Tables 5 and 6.

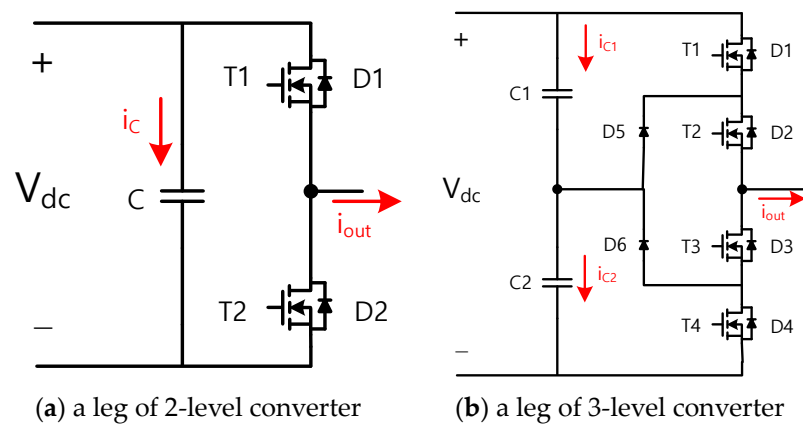


Figure 4. Leg configuration of AC–DC converters.

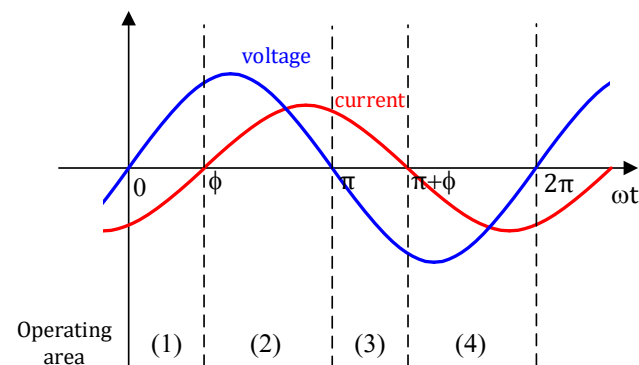


Figure 5. Operating area classification.

Table 4. Switch operation according to operating area.

Operating Area		(1)	(2)	(3)	(4)
2L	conduction path	T1 or T2			
	switching loss	T2	T1		T2
3L-NPC		T1, T2	T1, T2	D5, T2	T3, T4
	conduction path	or	or	or	or
	switching loss	T3, D6	D5, T2	T3, T4	T3, D6
		T3	T1	T2	T4

Table 5. Power semiconductor loss for 2L converter.

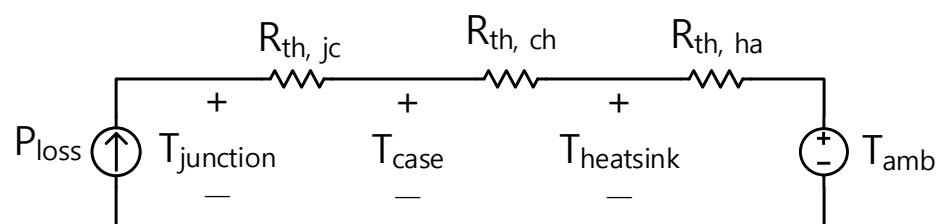
conduction loss	T1, T2	$\frac{R_{ds} I^2}{4}$
switching loss	T1, T2	$f_{sw} \frac{1}{2} \frac{V_{dc}}{V_{test}} E_{on/off} \left(\frac{2I}{\pi} \right)$

Table 6. Power semiconductor loss for 3L-NPC converter.

conduction loss	T1, T4	$\frac{R_{ds} M I^2}{3\pi} (1 + \cos^2 \varphi), M = \frac{V}{0.5 \times V_{dc}}$
	T2, T3	$\frac{R_{ds} I^2}{4}$
	D5, D6	$\frac{I}{12\pi} \left[V_{f0} \{12 + 3M((2\phi - \pi)\cos\phi - 2\sin\phi)\} + R_{ds} I \{3\pi - 4M(\cos^2 \phi)\} \right]$
switching loss	T1, T4	$f_{sw} \frac{\pi - \phi}{2\pi} \frac{V_{dc}}{V_{test}} E_{on/off} \left(\frac{I}{\pi - \phi} (\cos\phi + 1) \right)$
	T2, T3	$f_{sw} \frac{\phi}{2\pi} \frac{V_{dc}}{V_{test}} E_{on/off} \left(\frac{I}{\phi} (1 - \cos\phi) \right)$

The calculated losses of the power semiconductor are used to calculate the junction temperature rise of the power semiconductor. Figure 6 shows the heat transfer circuit model used to calculate the temperature rise in this paper. The losses generated by the power semiconductor are denoted as P_{loss} , and the thermal resistance from the junction of the power semiconductor to the case, the thermal resistance from the case to the heat sink, and the thermal resistance from the heat sink to the atmosphere are denoted as $R_{th,jc}$, $R_{th,ch}$, and $R_{th,ha}$, respectively. $T_{junction}$, T_{case} , $T_{heatsink}$, and T_{amb} represent the junction, case, heatsink, and ambient temperatures, respectively. The heat capacity of each part is not considered, but only steady-state losses and thermal resistance are considered to calculate the junction temperature. $R_{th,jc}$ and $R_{th,ch}$ use the datasheet values of the semiconductor device, and $R_{th,ha}$ of the heat sink can be entered to be used to calculate the temperature rise, as shown in (11).

$$\Delta T_{junction} = P_{loss} \times (R_{th,jc} + R_{th,ch} + R_{th,ha}) \quad (11)$$

**Figure 6.** Heat transfer circuit.

More precisely, thermal resistance could be expressed as a function of temperature [24]. However, as shown in [24], for accurate modeling, the parameters should be obtained through testing for each component used in the converter, which is difficult to achieve with

a basic design tool for various different types of components. The thermal resistance in this paper uses nominal values from the datasheet.

Most of the losses in the input filter come from the inductor. The loss of the inductor is determined by the design conditions, such as the core and winding used in the inductor, and the operating conditions, such as the magnitude and frequency of the voltage and current applied to the inductor. The conduction losses of an inductor are calculated using the resistance calculated from the cross-sectional area and length of the inductor windings, and the effective value of the current flowing in the inductor and the iron losses are calculated using the Steinmetz equation shown in (12) [25].

$$P_{core} = k f^{\alpha} B^{\beta} \quad (12)$$

The coefficients required for the Steinmetz equation were obtained from the core's datasheet information and added together by calculating the losses at the fundamental and switching frequencies. The flux density (B) was calculated using the magnitude of the fundamental wave current and the maximum ripple current magnitude, calculated using (2).

2.3. DC-Link Voltage, Current Ripple Calculations

The design tool in this paper derives the minimum DC-link capacitance values required during the converter design process. With the given system specifications and operating conditions, the DC-link capacitor currents of the 2L and 3L-NPC converters (i_C of the 2L converter and i_{C1}/i_{C2} of the 3L-NPC converter in Figure 4) can be calculated analytically, as shown in (13) and (14), respectively [26,27]. Table 7 shows the detailed formulas for the parameters used in (14).

$$I_{C,rms} = I_{rms} \sqrt{2m \left\{ \frac{\sqrt{3}}{4\pi} + \cos^2 \varphi \left(\frac{\sqrt{3}}{\pi} - \frac{9}{16} m \right) \right\}}, \quad m = \frac{V}{0.5 \times V_{dc}} \quad (13)$$

$$I_{C,rms} = I \sqrt{\frac{\sqrt{3}}{4\pi} \{ (Am_a + B) \cos 2\varphi + (Cm_a + D) \}}, \quad m_a = \frac{\sqrt{3}V}{V_{dc}} \quad (14)$$

Table 7. Expressions of A, B, C, and D in (14).

m_a	β	A	B	C	D
$0 \leq m_a \leq \frac{1}{2}$	-	$\frac{2}{3}$	1	0	0
$\frac{1}{2} < m_a \leq \frac{\sqrt{3}}{3}$	$\arcsin\left(\frac{1}{2m_a}\right) - \frac{\pi}{3}$	$\frac{\pi}{3} - 2\sin\left(\frac{\pi}{6} - \beta\right) - \frac{2}{3}\cos 3\beta$	$1 - 2\sin\left(\frac{\pi}{6} - \beta\right)$	$\sin\left(\frac{\pi}{3} - 2\beta\right)$	$\frac{\pi}{6} - \beta$
$\frac{\sqrt{3}}{3} < m_a \leq 1$	$\frac{\pi}{3} - \arcsin\left(\frac{1}{2m_a}\right)$	$\frac{\pi}{3} - 2\sin\left(\frac{\pi}{6} + \beta\right) - \frac{2}{3}\cos 3\beta$	$1 - 2\sin\left(\frac{\pi}{6} + \beta\right)$	$\sin\left(\frac{\pi}{3} + 2\beta\right)$	$\frac{\pi}{6} - \beta$

Taking the limit value of the voltage ripple as the input, the minimum value of the DC-link capacitor that satisfies the limit value can be selected as follows [26].

$$C_{dc,min} = \frac{I_{C,rms}}{V_{ripple} \times 2\pi f_{sw}} \quad (15)$$

The tool selects the minimum value of the DC-link capacitor through equation (15) and derives the minimum value of the ripple current rating of the capacitor through (13) or (14).

3. Design Examples

Many cases of grid-connected AC–DC converters were designed using the converter design tool introduced in this paper. Table 8 shows the specifications and operating

conditions of the design cases. All of them are 10 kVA-class grid-connected AC–DC converters and use 2L and 3L-NPC NPC converter topologies. The grid to which they are connected is assumed to be typical three-phase 380 V 60 Hz converters. The current ripple ratio indicates the magnitude of the ripple current relative to the rated current. Cases 1 and 2 and cases 3 and 4 have identical specifications except for the current ripple specification, resulting in designs with different input filters.

Table 8. Specification and operating conditions for design cases.

	Case 1	Case 2	Case 3	Case 4
topology	2L	2L	3L-NPC	3L-NPC
capacity [kVA]	10	10	10	10
power factor	0.99	0.99	0.99	0.99
input voltage/ dc-link voltage [V]	380/740	380/740	380/740	380/740
power semiconductor	C3M0032120K	C3M0032120K	C3M0060065K, E3D30065D	C3M0060065K, E3D30065D
switching frequency [kHz]	50	50	50	50
current ripple ratio [%]	22	33	10	20
voltage ripple ratio [%]	1	1	1	1

Table 9 shows the minimum values of the input filter and DC-link capacitance derived from the design tool. In (2), the current ripple magnitude of the 2L converter is generally larger compared to the 3L-NPC converter, resulting in a larger inductance despite the higher current ripple limit of the 2L converter. The minimum value of the DC-link capacitor resulting from the design is less than 10 μF , so in practice, the converter design should be based on selecting a capacitor that meets the current ripple rating. In such a design, the capacitance of the actual capacitor used is considerably larger than the minimum capacitance derived from the design tool, so that the voltage ripple caused by the current ripple is negligible.

Table 9. Input filter design results.

	Case 1	Case 2	Case 3	Case 4
converter side inductance (L_c) [μH]	387	258	194	97
grid side inductance (L_g) [μH]	129	86	65	32
filter capacitance (C_f) [μF]	6.1	6.1	6.1	6.1
damping resistance (R_d) [Ω]	1.3	1	2	1.3
minimum dc-link capacitance [μF]/[A]	7.9/9.2	7.9/9.2	6.2/7.3	6.2/7.3

4. Simulation and Experimental Results

Based on the results of the design tool introduced in this paper, simulation models and prototypes were produced and compared with the design values. For the four cases of circuits in Tables 8 and 9, simulation models were created using PSIM (version 9.0), and prototypes were fabricated and compared with the experimental results. Figure 7 is a photo of the experimental set of one of the fabricated prototypes. The current ripple of the fabricated converter was measured using an oscilloscope, and the efficiency was measured using a power meter. The temperature rise was measured by attaching an NTC to the heatsink where the power semiconductor was installed.

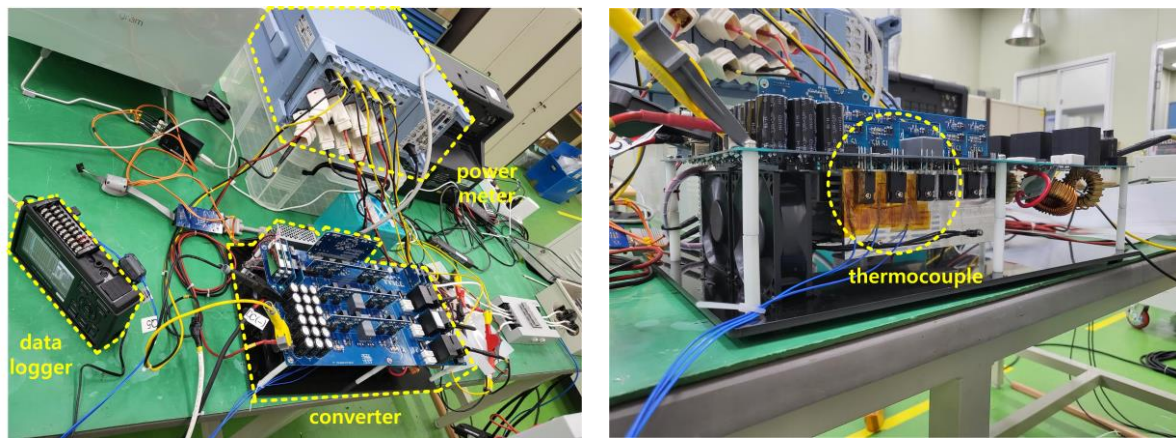


Figure 7. Experimental setup with prototype converter.

Figure 8 shows the waveforms of the fabricated simulation and the prototype. They represent the input line voltage, converter current, and grid current, respectively. It can be seen that the experimental waveforms have similar characteristics to the simulation results and behave appropriately. Both the experimental and simulation results show that the ripple of the converter-side current varies with the circuit topology and the parameters of the input filters, but the harmonics of the grid-side current are not significantly different in all four cases. It can be seen that the low-order harmonics, which have a significant impact on the grid-side current quality, are sufficiently suppressed by the current controller.

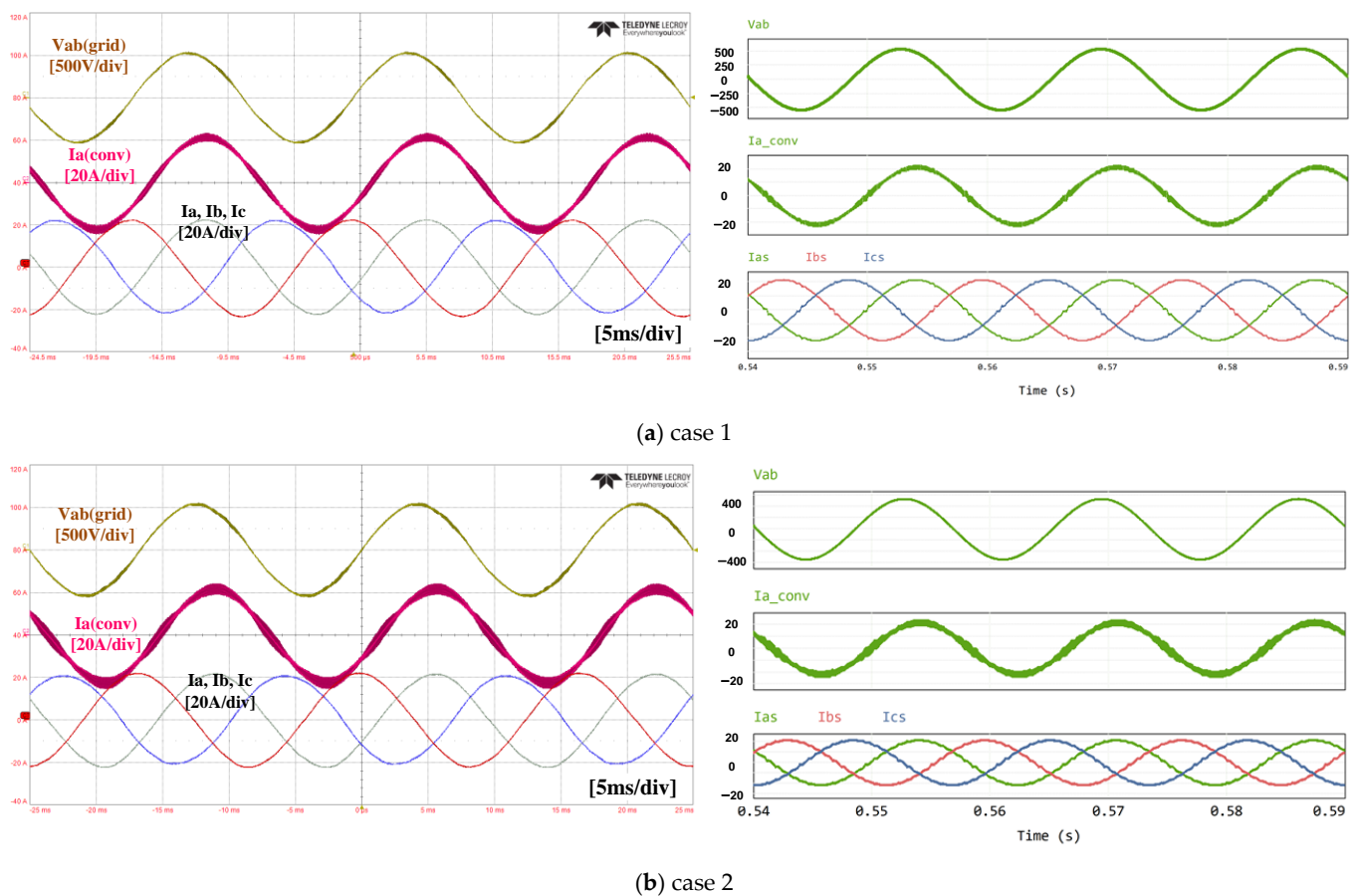


Figure 8. Cont.

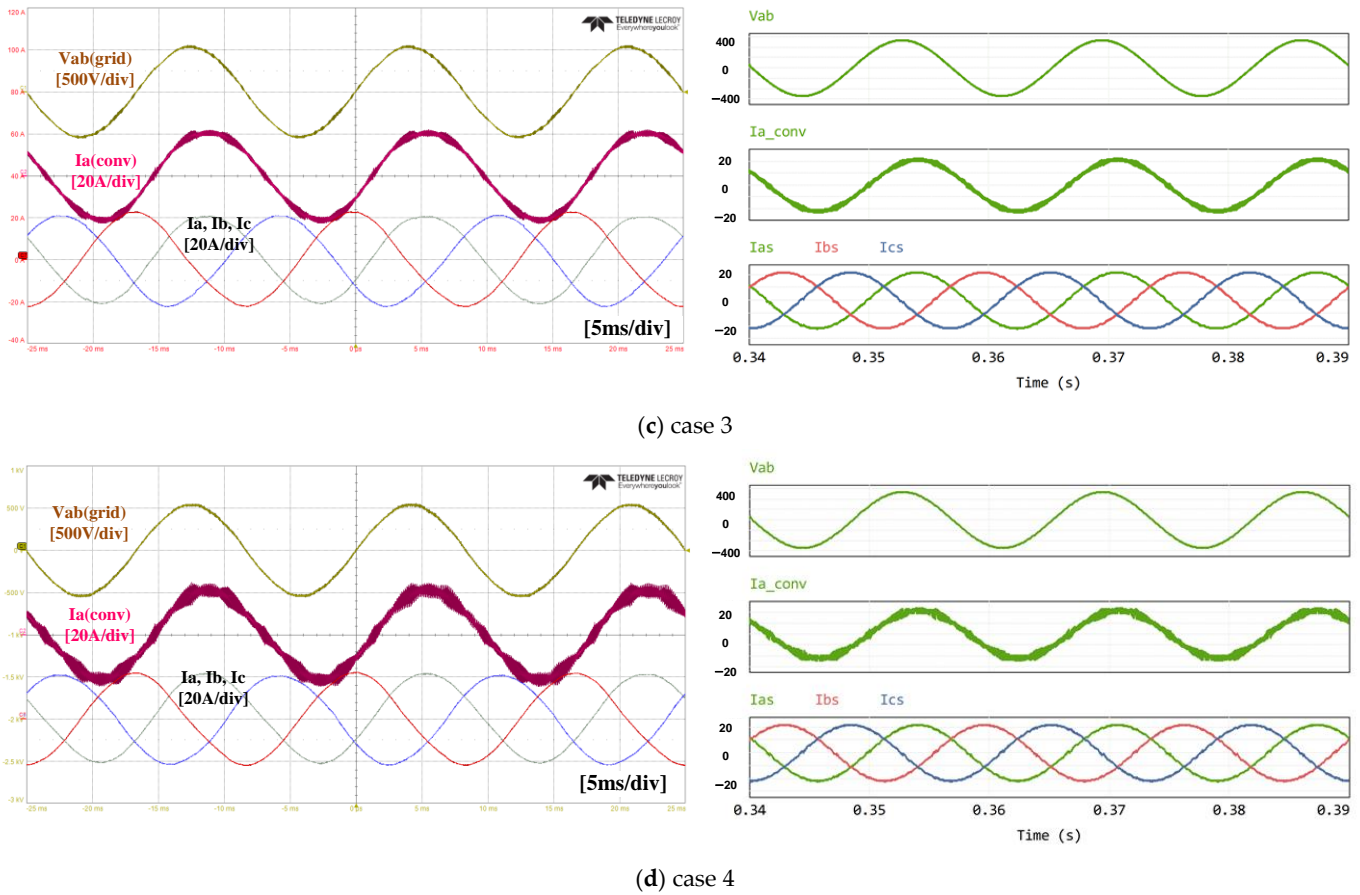


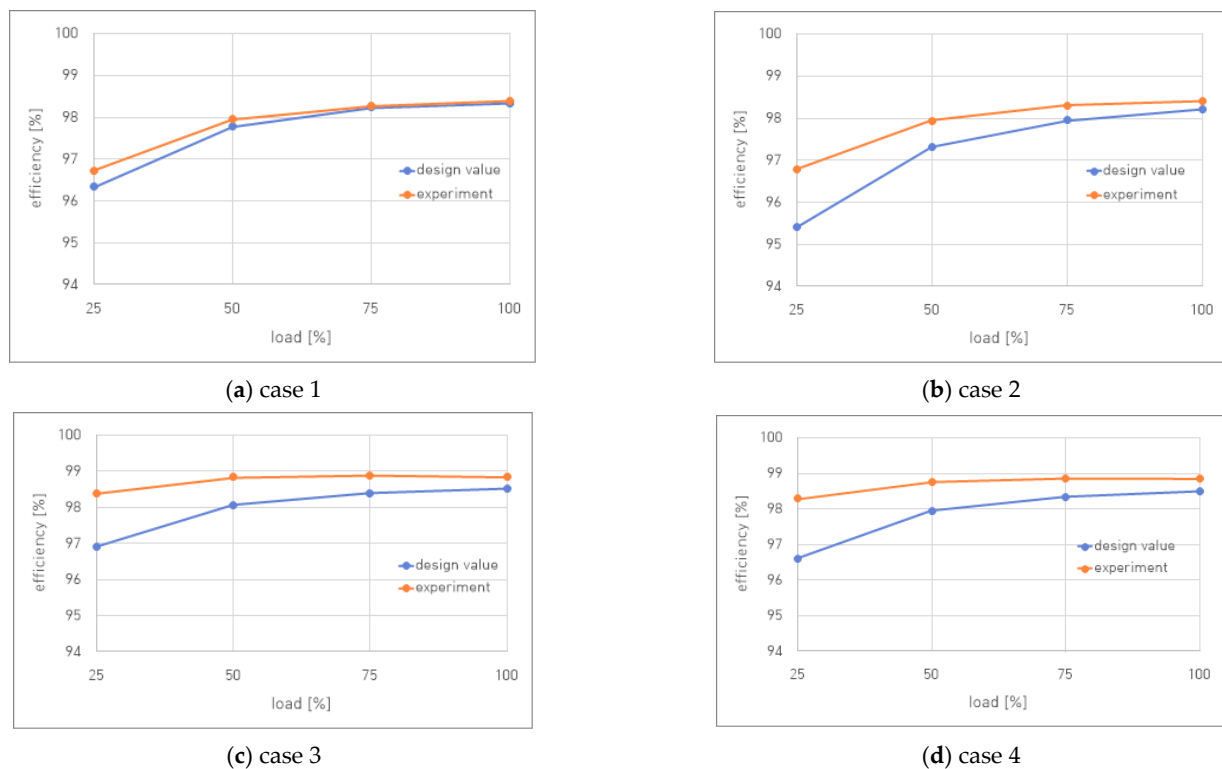
Figure 8. Experimental and simulation waveforms.

Table 10 shows the design values and experimental results of the current ripple, temperature rise, and THD of the grid current. For these metrics, only results at a rated load are compared, as their maximum values are considered during the design phase. The current ripple is similar to the design value for the 2L converter, while the 3L-NPC converter shows more deviation from the design value. In the 3L-NPC converter, the parasitic inductance along the switching path is larger due to the increase in the number of power semiconductor devices and the complexity of the busbar structure of the PCB, and the voltage spikes generated during switching have the effect of making the current ripple larger. The THD of the grid-side current is not considered in the design tool introduced in this paper, but the measured current THD is shown to confirm that the input filter, considering only the converter-side ripple current, can keep the current THD low enough if a sufficiently good PR controller is used under a fast switching frequency. The temperature rise was calculated by measuring the temperature of the heatsink near where the power semiconductor is attached, as shown in Figure 7. In the model in Figure 6, the power semiconductor losses were calculated as P_{loss} and compared to $T_{heatsink}$'s calculations and measurements. The heatsink model was calculated with a simple concentrated integer thermal resistance, and the temperature of three heatsinks near the power semiconductor was measured and averaged. For the 2L converter, the temperature rise difference between the design and experimental results is smaller, but for the 3L-NPC converter, the deviation is relatively larger. In the case of the 2L converter, the number of semiconductor devices and the size of the heat sink are smaller, so the heat transfer structure is simpler and more in line with the simple model in Figure 6, but in the case of the 3L-NPC converter, the placement structure of the power semiconductor devices and the heatsink is relatively more complex, which is estimated to cause a slight deviation from the model.

Table 10. Current ripple, THD, and temperature rise of design value and experimental results.

		Case 1	Case 2	Case 3	Case 4
current ripple [A]	design value	4.8	7.2	2.2	4.3
	experimental results	4.0	7.1	2.8	5.6
THD [%]	experimental results	2.44	2.4	2.7	2.3
temperature rise [K]	design value	14.2	14.2	12.7	12.7
	experimental results	13.7	14.2	8.5	10.7

Figure 9 shows the calculated efficiency of the design tool and the measured efficiency from the experiment. The losses in the power semiconductor and the losses in the input filter were used to calculate the efficiency. Overall, the deviation between the measured and calculated efficiency at low loads is large, and the error decreases as the load factor increases. At light loads, the iron losses in the input filter account for a large portion of the total losses, and it is assumed that the iron losses calculated through (12) are different from the actual losses incurred, leading to the error. The flux density is used as an input variable to calculate the iron loss in Equation (12). In the proposed design tool, the flux density is derived based on the maximum value of the current ripple calculated in (2). However, in practice, the magnitude of the current ripple varies with the phase angle [28]. In the phase section where the current ripple is reduced, the flux density is also reduced, resulting in smaller iron losses. As a result, the calculated value of iron loss is larger than the actual value. Further improvements in flux density variation according to phase angle may be needed to increase the precision of the iron loss calculation. However, as a tool used in the basic design phase of a converter, it can be considered to have a reasonable calculation error. It is also appropriate that the calculation error is reduced under heavy loads, as efficiency at higher load factors is generally considered more important.

**Figure 9.** Efficiencies vs. loads of design value and experimental results.

5. Conclusions

This paper presents a design tool for designing three-phase grid-connected AC–DC converters. The basic design procedures for drafting the system design of a 2L or 3L-NPC converter were introduced, and the theory and formulas used in each design procedure were presented. The introduced design tools view the converter as an electrical circuit composed of lumped elements and set basic specifications, such as the input and output voltages, capacitance, converter topology, and limit conditions, such as the efficiency, voltage and current ripple, and temperature rise, and select switching elements. Based on the input parameters, the ripple of the input current, DC-link voltage, and current ripple are calculated to derive the electrical parameters of the input filter and DC-link capacitor, and the converter losses and temperature rise are calculated to verify that the limit conditions are met.

The input filter uses the LCL filter structure, which is widely used in grid-connected converters. To limit the converter-side ripple current, the converter-side inductor value is determined first, and the grid-side inductor value is set accordingly. The capacitor value is determined according to the user-entered reactive power magnitude limit, and the damping resistor value is set to make the impedance of the input filter at the resonant frequency large enough.

Then, to calculate the efficiency, the converter losses are calculated. There are two main types of losses discussed in this paper: power semiconductor losses and input filter losses. The power semiconductor losses are calculated using the device's datasheet information. The rms and average current flowing in each device are calculated and applied to the datasheet information of the power semiconductor device to calculate the conduction and switching losses. The temperature rise is calculated using the thermal resistance information of the semiconductor device, the heatsink, and the previously calculated losses of the semiconductor device. The losses of the input filter are calculated by calculating the copper and iron losses of the inductor.

The current ripple in the DC stage is calculated analytically using the given system specifications and operating conditions. The calculated current ripple is used to find the minimum value of the DC-link capacitor that satisfies the voltage ripple given as a limit.

Using the introduced design tool, the converter design for various conditions is carried out and validated through a simulation and experiment. For four 10kVA-class converters, the design tool was used to derive the parameters of the input filter and the minimum value of the DC-link capacitor, and simulation models and prototypes were built based on the derived values and compared with the results of the design tool. The experimental results showed that the temperature rise and current ripple magnitude were similar to the results of the design tool. The measured efficiency showed some deviation from the calculated value in the light-load region, but overall, the trend of efficiency change with load factor was similar in the design value and the experimental result, and the difference in the absolute values was small, showing that it is suitable as a basic design tool.

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References

1. Mohan, N.; Undeland, T.M.; Robbins, W.P. *Power Electronics: Converters, Applications, and Design*; Wiley: Hoboken, NJ, USA, 2003.
2. Rashid, M.H. *Power Electronics: Circuits, Devices, and Applications*; Pearson: London, UK, 2011.
3. Erickson, R.W.; Maksimović, D. *Fundamentals of Power Electronics*; Springer: Berlin/Heidelberg, Germany, 2007.
4. Toshon, T.A.; Faruque, M.O. A design optimisation tool to minimise volume and failure rate of the modular multilevel converter and the thyristor-controlled rectifier. *J. Mar. Eng. Technol.* **2023**, *22*, 189–198. [\[CrossRef\]](#)
5. Saha, J.; Hazarika, D.; Gorla, N.B.Y.; Panda, S.K. Machine-Learning-Aided Optimization Framework for Design of Medium-Voltage Grid-Connected Solid-State Transformers. *IEEE J. Emerg. Sel. Top. Power Electron.* **2021**, *9*, 6886–6900. [\[CrossRef\]](#)
6. Soeiro, T.B.; Mühlethaler, J.; Linnér, J.; Ranstad, P.; Kolar, J.W. Automated Design of a High-Power High-Frequency LCC Resonant Converter for Electrostatic Precipitators. *IEEE Trans. Ind. Electron.* **2013**, *60*, 4805–4819. [\[CrossRef\]](#)
7. Liu, X.; Qiu, L.; Fang, Y.; Wang, K.; Li, Y.; Rodríguez, J. Finite Control-Set Learning Predictive Control for Power Converters. *IEEE Trans. Ind. Electron.* **2023**. [\[CrossRef\]](#)
8. Liu, X.; Qiu, L.; Fang, Y.; Wang, K.; Li, Y.; Rodríguez, J. Predictive Control of Voltage Source Inverter: An Online Reinforcement Learning Solution. *IEEE Trans. Ind. Electron.* **2023**. [\[CrossRef\]](#)
9. Li, X.; Zhang, X.; Lin, F.; Blaabjerg, F. Artificial-Intelligence-Based Design for Circuit Parameters of Power Converters. *IEEE Trans. Ind. Electron.* **2022**, *69*, 11144–11155. [\[CrossRef\]](#)
10. Dragičević, T.; Wheeler, P.; Blaabjerg, F. Artificial Intelligence Aided Automated Design for Reliability of Power Electronic Systems. *IEEE Trans. Power Electron.* **2019**, *34*, 7161–7171. [\[CrossRef\]](#)
11. WEBENCH Circuit Designer. Available online: <https://www.ti.com/tool/WEBENCH-CIRCUIT-DESIGNER> (accessed on 13 October 2023).
12. SMPS Designer. Available online: <https://infineon.powersim.com/> (accessed on 13 October 2023).
13. The General Converter Design Tool. Available online: <https://wbg.koema.or.kr> (accessed on 13 October 2023).
14. Holmes, D.G.; Lipo, T.A. *Pulse Width Modulation for Power Converters: Principles and Practice*; IEEE Press: Piscataway, NJ, USA, 2003.
15. *IEEE Standard 519-2014*; IEEE Recommended Practices and Requirements for Harmonic Control in Electrical Power Systems, (Revision of IEEE Standard 519-1992). IEEE: New York, NY, USA, 2014; pp. 1–29. [\[CrossRef\]](#)
16. *IEEE Standard 1547-2018*; IEEE Standard for Interconnection and Interoperability of Distributed Energy Resources with Associated Electric Power Systems Interfaces, (Revision of IEEE Std 1547-2003). IEEE: New York, NY, USA, 2018. [\[CrossRef\]](#)
17. Lascu, C.; Asiminoaei, L.; Boldea, I.; Blaabjerg, F. Frequency Response Analysis of Current Controllers for Selective Harmonic Compensation in Active Power Filters. *IEEE Trans. Ind. Electron.* **2009**, *56*, 337–347. [\[CrossRef\]](#)
18. Grandi, G.; Loncarski, J.; Dordevic, O. Analysis and Comparison of Peak-to-Peak Current Ripple in Two-Level and Multilevel PWM Inverters. *IEEE Trans. Ind. Electron.* **2015**, *62*, 2721–2730. [\[CrossRef\]](#)
19. Jiao, Y.; Lee, F.C. LCL Filter Design and Inductor Current Ripple Analysis for a Three-Level NPC Grid Interface Converter. *IEEE Trans. Power Electron.* **2015**, *30*, 4659–4668. [\[CrossRef\]](#)
20. Jalili, K.; Bernet, S. Design of LCL filters of active-front-end two level voltage-source converters. *IEEE Trans. Ind. Electron.* **2009**, *56*, 1674–1689. [\[CrossRef\]](#)
21. Jayalath, S.; Hanif, M. Generalized LCL-Filter Design Algorithm for Grid-Connected Voltage-Source Inverter. *IEEE Trans. Ind. Electron.* **2017**, *64*, 1905–1915. [\[CrossRef\]](#)
22. Liserre, M.; Blaabjerg, F.; Hansen, S. Design and control of an LCL-filter-based three-phase active rectifier. *IEEE Trans. Ind. Appl.* **2005**, *41*, 1281–1291. [\[CrossRef\]](#)
23. Górecki, P. Electrothermal Averaged Model of a Diode-IGBT Switch for a Fast Analysis of DC-DC Converters. *IEEE Trans. Power Electron.* **2022**, *37*, 13003–13013. [\[CrossRef\]](#)
24. Górecki, P.; Górecki, K. Measurements and computations of internal temperatures of the IGBT and the diode situated in the common case. *Electronics* **2021**, *10*, 210. [\[CrossRef\]](#)
25. KVenkatachalam; Sullivan, C.R.; Abdallah, T.; Tacca, H. Accurate prediction of ferrite core loss with nonsinusoidal waveforms using only Steinmetz parameters. In Proceedings of the Computers in Power Electronics, Mayaguez, PR, USA, 3–4 June 2002; pp. 36–41.
26. Karanayil, B.; Agelidis, V.G.; Pou, J. Performance Evaluation of Three-Phase Grid-Connected Photovoltaic Inverters Using Electrolytic or Polypropylene Film Capacitors. *IEEE Trans. Sustain. Energy* **2014**, *5*, 1297–1306. [\[CrossRef\]](#)
27. Zhao, Z.; Diao, F.; Wu, Y.; Wang, Z.; Zhao, Y. DC-Link Capacitor Current Modeling and Analysis for Three-Level Voltage Source Inverters. In Proceedings of the IEEE Applied Power Electronics Conference and Exposition (APEC), Phoenix, AZ, USA, 14–17 June 2021.
28. Jiang, D.; Wang, F. Current-Ripple Prediction for Three-Phase PWM Converters. *IEEE Trans. Ind. Appl.* **2014**, *50*, 531–538. [\[CrossRef\]](#)

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