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The Development of a Compact Pulsed Power Supply with Semiconductor Series Connection

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Abstract: In this study, high-voltage switching was performed by connecting semiconductors in series. By employing Snubber circuits and voltage divider resistors for each semiconductor, the destruction of the semiconductors was prevented. Additionally, a pulse transformer was installed between the function generator and the photocoupler to isolate the gate circuit, preventing electrical discharges in the circuit and enabling operation at an output voltage of 10 kV and an operating frequency of 200 Hz. The temperature of the semiconductors increased with the increase in operating frequency, which was counteracted by connecting charging resistors and capacitors to limit the current to the semiconductors. As a result, operation at 430 Hz became possible. Furthermore, a saturable inductor (SI) was connected to enable continuous operation. The SI delays the rise of the current and creates a phase difference, thereby reducing the power consumption of the conductor and mitigating the temperature rise, enabling continuous operation at 300 Hz. Moreover, by increasing the number of semiconductor series stages to six, an output voltage of 20 kV was confirmed in tests. By using two semiconductor series circuits, the pulsed power supply that can be changed to any pulse width was also created. As a result, output voltages with arbitrary pulse widths from 5 μs to 30 μs were confirmed.

Keywords: power semiconductor; serialization; saturable inductors

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1. Introduction

Pulsed power technology has made remarkable progress in recent years and has been applied to a wide range of fields, including exhaust gas treatment [1–3], concrete crushing [4–6], plasma etching [7–9], and laser oscillation [10–12]. It has been actively applied to biological fields [13–17]. In these applications, a high electric field is generated and applied to the target. However, the target materials, such as seawater [18–20], sewage [21–23], or liquid fertilizer [24,25], are often the cases involving low-impedance loads, making the inactivation of bacteria by a high electric field a challenging task.

Pulse power is mainly generated by a magnetic pulse compression impulse power supply [26–35]. The advantage of this method is that using a transformer allows for lower-rated voltages of the required semiconductors, making it easier to ensure semiconductor reliability. However, the use of magnetic materials for the transformer and the SI requires

an increased power supply capacity and a large current flow when applying high voltage to a low-impedance load, resulting in a larger and heavier power supply [36].

Therefore, to address this issue, we employed series-connected power semiconductors without the need for large magnetic materials. Currently, research is underway on series connection and switching beyond the rated voltage of a single discrete semiconductor [36–49]. One of the specific challenges with the series connection of semiconductors is the occurrence of voltage differences between them, which can lead to voltages surpassing the rating of a single semiconductor, resulting in its destruction. Additionally, the power consumption of the semiconductors increases, leading to temperature rises. To address these issues, conventional research has focused on methods such as active clamping [50] and active gate control [39], which introduce collector voltage adjustment functions, including overvoltage protection, to the gate driver.

The active clamp method adopts a dependent drive configuration, where the lowest stage among multiple connected semiconductors serves as the master stage, while the higher stages are considered dependent stages. The external trigger supplied to the switch is only provided to the lowest master stage, eliminating the need for supplying both the external trigger and gate power to the dependent stages. In this method, when performing low-voltage switching with multiple IGBTs connected in series, the voltage divider voltage of the master stage decreases before conduction, resulting in a reduction of the transient current compared to high-voltage switching. As a result, it becomes more challenging for the dependent stages to conduct. To prevent semiconductor breakdown in this low-voltage region, an active clamp circuit is employed. The circuit is configured with a Zener diode and a diode as clamp elements between the gate and collector. When an overvoltage exceeding the clamping voltage specified by the Zener diode is applied to the IGBT, the Zener diode conducts, allowing current to flow in the direction of the collector and Zener diode. This action lowers the voltage between the emitter and collector to the clamp voltage, effectively preventing semiconductor breakdown. However, the significant switching losses pose a challenge as they cause an increase in the temperature of the semiconductor.

The active gate control method is designed to mitigate the turn-off losses that are problematic in the active clamp method. The gate signal circuit consists of an on/off signal generation circuit, a signal switching circuit, a clamp signal generation circuit, and a gate voltage generation circuit. When a turn-off signal is input and the gate voltage reaches the threshold, the collector voltage starts to rise. As the collector voltage exceeds the DC voltage of the IGBT alone, the current decreases. The collector voltage continues to rise while the current decreases. When both the collector voltage and current locus exceed the set value, the collector voltage is clamped because the saturation current value of the IGBT is higher than the instantaneous collector current value. If the cutoff current is small, the collector voltage can be clamped at a relatively low gate voltage, resulting in a low clamping voltage. Even when the breakdown current is higher, it is possible to prevent overvoltage from being applied to the IC by turning the gate completely on when the breakdown current reaches the limit value of the semiconductor's withstand voltage. This feature excels in suppressing the increase in loss during the turn-off phase. However, compared to the active clamp method, the active gate control method requires integrating the control circuit into each semiconductor, which increases the number of components and makes the circuit more complex.

In this study, we aimed to equalize the voltage distribution across each semiconductor by connecting a Snubber circuit to each one. The Snubber circuit is a simple circuit composed of resistors, capacitors, and diodes. It can absorb the transient high voltage generated during the turn-off phase, effectively protecting the semiconductors. However, similar to the active clamp method, there is a notable increase in semiconductor temperature due to switching losses. To address this issue, we introduced the use of a saturable inductor (SI), which introduces a delay in the current rise, creating a phase difference to suppress power consumption during the turn-on phase and reduce temperature rise. This approach, combining Snubber circuits and SI, offers the potential to minimize temperature rise com-

pared to the active clamp method while providing the advantage of a simpler circuit setup compared to the active gate control method.

There are two methodologies to improve the performance of semiconductor series circuits performed in this study. The first one is the method of adjusting the gate resistance of each stage to equalize the turn-off voltage. Compared to the method using active gate control or the method using active clamp circuits, this method has the advantage of reducing the number of elements around the gate and matching the timing of the voltages with a simple method. The second one is the use of SI as a method to suppress the temperature rise of semiconductors and increase the operating frequency. By connecting a saturable inductor and a semiconductor switch in series, a phase difference between the voltage and current of the semiconductor can be made, thereby reducing losses.

The reduction of switching losses with SI, serial connection of semiconductor devices, and jitter adjustment methods are all well-established technologies. However, the key distinguishing feature lies in their comprehensive integration, allowing for easy variation of pulse width and output voltage. Another noteworthy aspect is that the components are readily available in the market, making it easy to create this system without the need for gate adjustments or programming.

The SI used in this method is much smaller than those typically used in conventional magnetic pulse compression impulse power supplies. This resolves the issues of large size and heavy weight associated with traditional pulsed power supplies. Furthermore, the series connection of semiconductors enables switching beyond the rating of a single unit. However, the pulse width cannot be adjusted and varies with the load. To address this limitation, a circuit was developed using two instances of this three-stage circuit, allowing for arbitrary control of the pulse width of the output voltage. A pulse width change test was conducted to validate this capability. Additionally, tests were performed to increase the number of semiconductor stages in order to enhance the output voltage.

2. Materials and Methods

In this study, a circuit was developed to enable switching of semiconductors beyond their individual ratings by connecting them in series. Figure 1 depicts the circuit diagram. The circuit consists of a gate signal circuit, a semiconductor, a Snubber circuit, and a voltage divider resistor. The semiconductor utilized was an IGBT (IXYT30N450HV, IXYS CORPORATION, Milpitas, CA, USA). It possesses a voltage rating of 4.5 kV, making it the highest voltage rating among discrete power semiconductor devices available on the market through distributors like Mouser. Additionally, among power semiconductor devices with a 4.5 kV voltage rating, this IGBT is particularly compact and easy to mount on a substrate, making it the preferred choice for this application. To increase the output voltage, three of these stages are connected in series.

The operating principle is as follows: A voltage from the DC input power supply is applied to the semiconductors. When the gate signal is transmitted from the function generator to the gate through the photocoupler, the semiconductor turns on, allowing current to flow and voltage to be applied to the load resistance.

The gate signal comprises a photocoupler (TLP250, Toshiba Corporation, Tokyo, Japan), a current limiting resistor (Rc = 220 Ω), a gate resistor (R_G = 3.3 Ω), and a DC-DC converter (MGJ6D122005WMC-R7, Murata Manufacturing Co., Ltd., Kyoto, Japan). The gate signal is transmitted from the function generator to the IGBTs via a photocoupler. The gates of the semiconductors require individual signal application. While the use of pulse transformers is conceivable, there is a risk of inadvertent turn-on phase due to the noise generated when switching high voltages. To address this, the gate signals of each semiconductor device are insulated using photocouplers. Additionally, on the secondary side of these photocouplers, an isolated power source is used to ensure that the semiconductor device gates are not electrically connected to the signal generation section.

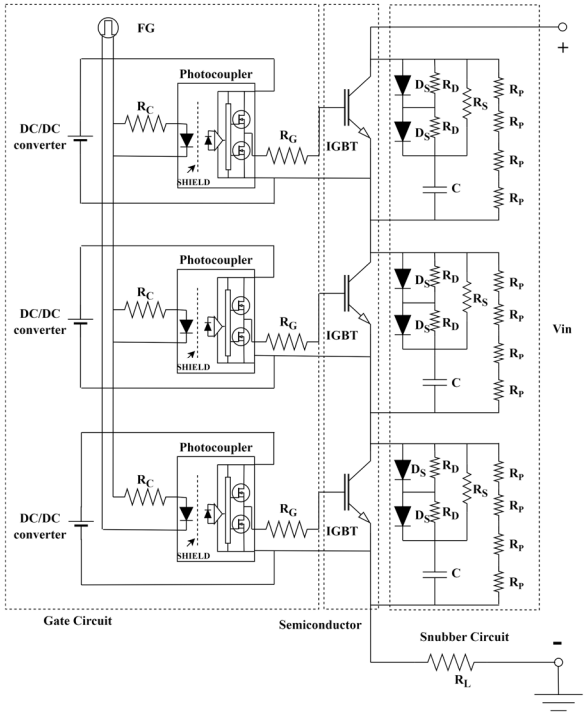


Figure 1. Circuit of semiconductor series connection. One stage consists of a gate circuit, semiconductors, and Snubber circuit. The diagram shows the circuit in three stages.

One of the causes leading to the destruction of serially connected semiconductors is the generation of surge voltage during the turn-off phase. This surge voltage is a high voltage generated by the floating inductance of the wiring when the current is interrupted. When this high voltage occurs, there is a possibility of applying a voltage exceeding the rated value to the semiconductor, which can result in its destruction. In this study, we addressed the issue of semiconductor destruction due to surge voltage by connecting a Snubber circuit to each IGBT. This was implemented in the proposed pulsed power supply used in the research. The Snubber circuit consists of a Snubber resistor (R_S = 33 Ω), a Snubber diode (GD60MPS17H, GeneSiC Semiconductor Inc., Dulles, VA, USA), a diode divider resistor (R_D = 1 MΩ), and a Snubber capacitor (C = 18 nF). The capacitor absorbs the energy stored in the floating inductance of the wiring. During this process, the current flows through diodes and charges the capacitor. Subsequently, the energy accumulated in the capacitor is dissipated through Snubber resistors. As a result, the Snubber circuit suppresses surge voltage, preventing semiconductor damage. Diodes used in the Snubber circuit require a high voltage rating, necessitating the use of two diodes. To prevent diode breakdown, it is essential to ensure that the reverse voltage applied to each diode is distributed evenly. To achieve this, very large resistors are connected in parallel with each diode, allowing for equal voltage division and mitigating diode breakdown. In component selection for this study, the following considerations were made for each component. For the Snubber capacitor, a film capacitor with a large capacitance, good frequency characteristics, and easy availability was used. These capacitors absorb energy from the floating inductance in the wiring during the turn-off phase. The Snubber resistor was chosen to be a cement resistor. Cement resistors were preferred due to their excellent heat dissipation properties, outstanding heat resistance, and insulation capabilities. This choice was made to withstand the high charging voltage from the Snubber capacitor and resist the heat generated by the current. For the Snubber diode, silicon carbide (SiC) Schottky barrier diodes were utilized. These diodes were selected for their ability to handle high charging voltages and generate minimal heat. To minimize heat generation, it is essential to reduce power losses associated with reverse recovery current and forward voltage drop. SiC Schottky barrier diodes, with their shorter reverse recovery times, higher voltage ratings, and lower forward

voltage drops, outperform silicon Fast Recovery Diodes (FRD). The voltage divider for the Snubber diode used metal film resistors to ensure precise voltage division and maintain resistance stability even when the resistor temperature rises. In terms of Snubber circuits, two common types are RC (resistor–capacitor) Snubber circuits and RCD (resistor–capacitor-diode) Snubber circuits. The Snubber circuit used in this study was an RCD Snubber circuit. RCD Snubber circuits, incorporating diodes, enable the use of larger Snubber resistor values, reducing the load on the semiconductor. This choice was particularly suitable when working with high-capacity semiconductors.

When semiconductors are connected in series, it is necessary to balance the voltages applied to each semiconductor. This is carried out to prevent the voltage difference between the voltage dividers of each semiconductor during turn-on and turn-off switching from exceeding the maximum rated voltage and causing breakdown [51]. In this study, the voltage division was achieved by connecting a voltage divider resistor, R_P. As for the voltage divider resistor in the main circuit, metal-clad resistors were chosen due to their superior cooling properties. Since high voltages were expected to be applied, potentially causing temperature rise due to Joule heating, the selection of metal-clad resistors was considered appropriate. However, the temperature of the voltage divider resistor becomes very high. Although the resistance value increases due to this temperature rise, the temperature rise of each resistor has an individual value and is not constant, so there is a possibility that the voltage division may not be equal. Therefore, heat dissipation fins and a fan were used to cool the resistors and maintain a constant resistance. In this case, the circuit was constructed on a PCB substrate to reduce its size. Additionally, the circuit was immersed in Class A insulating oil to prevent electrical discharge on the board since the circuit length was shortened due to miniaturization.

This paper describes an experiment conducted to vary the gate resistance in order to prevent breakdown of series-connected semiconductors when subjected to voltages higher than the rated voltage due to the voltage-sharing difference. In the experimental setup, the voltage waveforms of each semiconductor were measured with a gate resistance of $R_G = 3.6\ \Omega$. Subsequently, the voltage waveforms of each semiconductor were measured by changing the gate resistance and compared with the waveforms before the change. In this experiment, we connected 10 semiconductor stages and measured the voltage waveforms of each semiconductor. The input voltage for the experiment was set to approximately 1 kV, which is lower than the breakdown voltage of individual semiconductors.

Furthermore, the configuration of the gate circuit was modified to prevent electrical discharge in the circuit when switching at high voltages. The TLP250 with an insulation voltage of 2500 V was replaced with a TLP350 with an insulation voltage of 3750 V. To prevent the risk of the photocoupler experiencing insulation breakdown and subsequently damaging the function generator, a pulse transformer was connected between the primary side of the photocoupler and the function generator. A pulse transformer (PT4E, OEP) was connected to electrically isolate the primary side of the photocoupler from the function generator.

In the circuit created in this study, current flows through the charging resistor during the semiconductor turn-on phase, causing the semiconductor temperature to rise. Therefore, a capacitor ($C_{charging} = 4$ nF) is connected in parallel to the main circuit and charged via a charging resistor ($R_{charging} = 40\ k\Omega$), and the capacitor is discharged when the semiconductor turns on.

In this study, we connected SI [52–59] in series with the semiconductor switch to suppress the temperature rise of the semiconductor and increase the operating frequency. The SI utilizes the nonlinearity of the magnetization curve of ferromagnetic materials. When the semiconductor switch turns on, voltage is applied to the non-saturated SI. Over time, the SI saturates as the saturation duration elapses. Subsequently, the primary current flows through the SI. This means that there is a time difference from the turn-on phase of the semiconductor to the saturation of the SI, resulting in a phase difference between the voltage and current, as observed from the perspective of the semiconductor. The switching

losses of the semiconductor switch primarily stem from on-resistance, off-state leakage current, and losses during transitions between turn-on and turn-off states. Among these, the losses occurring during the transition to the turn-on state can be reduced by utilizing SI. The magnetic material is brought from an unsaturated to a saturated state, reducing the inductance by decreasing the magnetic permeability μ for switching. The unsaturated inductance of a SI is provided by Equation (1).

$$L_{US} = \frac{\mu_0 \mu_r A N^2}{\iota} \tag{1}$$

In Equation (1), μ_0 represents the magnetic permeability in vacuum, μ_r is the specific permeability of the magnetic material when unsaturated, A denotes the cross-sectional area of the core, N represents the number of turns of the coil and indicates the magnetic path length of the core. When a positive pulse voltage is applied to the SI, the magnetic flux density in the core can be set to the point of negative residual flux density on the magnetization curve by passing a negative current through the coil. The magnetic flux density at the transition from unsaturation to saturation can be used as the flux density change in the core. The inductance of the SI maintains the value expressed in Equation (1) when the core excitation state changes. To reset the core, a DC current is applied to the SI by an external circuit to adjust the core to the specified excitation state. If the core is adjusted to a negative residual flux density, the cross-sectional area of the core, A, and the number of turns of the coil, N, must satisfy Equation (2) to saturate the core in T_S seconds after the voltage is applied to the SI.

$$\int_0^{T_S} v dt = N \Delta B A \tag{2}$$

If the load voltage V_L is given by $V_L = V_m(1 - \cos \omega t)/2$, the product of the cross-sectional area of the core and the number of turns of the coil follows Equation (3) to achieve core saturation at T_S when the voltage is at its maximum.

$$AN = \frac{V_m T_S}{2\Delta B} \tag{3}$$

Transforming Equation (3) into an expression for T_S gives us Equation (4) for the saturation time of the Saturable Inductance.

$$T_S = A \cdot N \cdot \frac{2\Delta B}{V_m} \tag{4}$$

Considering the turn-on time of the semiconductor, the cross-sectional area of the SI was varied to obtain an appropriate saturation time. The ON/OFF control of the SI is achieved by allowing current to flow in a low inductance state during magnetic core saturation and preventing the flow of current in a high inductance state during non-saturation. As a result, the permeability of the magnetic core material during saturation and non-saturation significantly influences the SI's switching performance. The key characteristics required for the magnetic core material of SI include a high ratio of permeability during non-saturation to permeability during saturation ($\mu_{\mathrm{un}}/\mu_{\mathrm{sst}}$), high saturation magnetic flux density, high residual magnetic flux density, and low magnetic core losses. The magnetic material used for the SI was a nanocrystalline soft magnetic material called FINEMET® (FT-3H, Hitachi Metals, Ltd., Tokyo, Japan). In comparison to conventional amorphous materials, it is characterized by a higher saturation magnetic flux density and lower coercivity. This magnetic material is a soft Fe-based material with a maximum flux density of 1.23 T, a holding power of 0.6 A/m, an initial permeability of 2000, and a core size consisting of 2 or 4 pieces connected to vary the cross-sectional area.

To confirm the reduction in power consumption achieved by the SI, we conducted measurements of power consumption during the turn-on phase, on-state, and off-state of

the semiconductor. The parameters measured included input voltage, output voltage, and load current. High-voltage probes were used for voltage measurements, while a Current Transformer (CT) device was employed for load current measurements. The load resistance was set at 1 kΩ, the operating frequency was 1 Hz, and the signal pulse width was 40 μs for the experiments. In the assessment of semiconductor power consumption, the voltage imparted to the semiconductor is ascertained through the disparity between the input (*Vin*) and output voltages (*Vout*) at the instants of semiconductor turn-on phase, on-state, and off-state, sequentially, and then integrated with the current over the course of time (Equation (5)).

$$\int_{t_0}^{t_1} (Vout - Vin) \cdot I \, dt \tag{5}$$

In this case, t_0 represents the time when the gate is input, and t_1 represents the time when the maximum output voltage is reached. Similarly, t_2 is 40 μs after t_1, and t_3 is the time when the output voltage falls to 10% of the output voltage. The value of 40 μs for t_2 is derived from the pulse width set in the function generator. The turn-on time is defined as the duration from t_1 to t_2, while the off-state time is from t_2 to t_3. By connecting the SI, the current rises with a delay equal to the saturation time generated by the SI after the semiconductor is turned on. This creates a time difference between the rise of voltage and the rise of current, leading to an expected reduction in power consumption. To verify the actual reduction in semiconductor temperature achieved by the SI, a temperature measurement test was conducted. The collector, which is the hottest part of the semiconductor surface, was measured every 30 s until the temperature stabilized using a non-contact thermometer. Temperature comparison tests were performed under three conditions: without the SI connection, with The SI connection, and with a Snubber resistor changed to 1 kΩ due to its high temperature exceeding 100 °C. The temperature comparison test was conducted at an operating frequency of 200 Hz. The load resistor is 2 kΩ, and the pulse signal width is 40 μs. After confirming the reduction in semiconductor temperature due to SI connections, an operation test was conducted to increase the operating frequency. The frequency was incrementally increased by 10 Hz while conducting the operation test.

In this study, a three-stage circuit was employed to achieve an output voltage of 10 kV. To further increase the output voltage, the number of series-connected semiconductor stages was increased. The target output voltage was set at 20 kV, and the number of stages was set to six. The semiconductors used in this study have a withstand voltage of 4.5 kV, and the six stages provide a total withstand voltage of 27 kV, which is sufficient for the entire circuit. Subsequently, an operational test was conducted by applying a voltage of 20 kV to a load resistance of 2 kΩ. The challenge when increasing the output voltage is that discharge is more likely to occur on the substrate. It is necessary to improve the insulation performance of the circuit on the substrate. The circuit board, which constitutes the circuit, was created through etching and subsequent soldering of components. After its assembly, the circuit board was subjected to aeration treatment with high-voltage insulating oil and then immersed in it. Additionally, as the frequency increased, the temperature of the insulating oil also rose, necessitating its circulation using a pump. The semiconductor series-connected circuit developed in this study can withstand a high voltage of 10 kV. However, the pulse width cannot be adjusted and varies with the load. Therefore, we created a circuit that allows for arbitrary adjustment of the pulse width of the output voltage by utilizing two of these three-stage circuits. Initially, a semiconductor series circuit was connected in parallel with the load resistor to the circuit shown in Figure 1 as a mechanism to control the timing of voltage drop. Similar to the pre-connection stage, the semiconductors are turned on by a function generator using a gate circuit. Then, the circuit connected in parallel with the load resistor is turned on at the desired pulse width timing. This allows current to flow through the series-connected circuit with low resistance, reducing the voltage applied to the load resistor. The time between turning on the semiconductor in the main circuit and

turning on the semiconductor series-connected circuit in parallel with the load resistor can be used as the pulse width.

3. Results

3.1. Series Connection of Semiconductors

3.1.1. Adjustment of Gate Resistance for Uniform Voltage Sharing among Semiconductors in Series Connection

When semiconductors are connected in series, if the voltage sharing of each semiconductor is not the same during the turn-on phase, a voltage higher than the rated voltage is applied to the semiconductor, resulting in a breakdown. To achieve series-connected switching, we attempted to match the falling voltage waveforms by varying the gate resistance.

The voltage waveforms between the emitter and the collector at the turn-on phase for each stage were checked with a gate resistance of R_G = 3.6 Ω. Figure 2a shows the voltage waveforms of the rated stages. It can be observed that the voltage divider voltages of all semiconductors are uniform at the turn-on phase. However, there is a difference in the voltage-sharing voltage at the falling edge of the voltage after the turn-on phase.

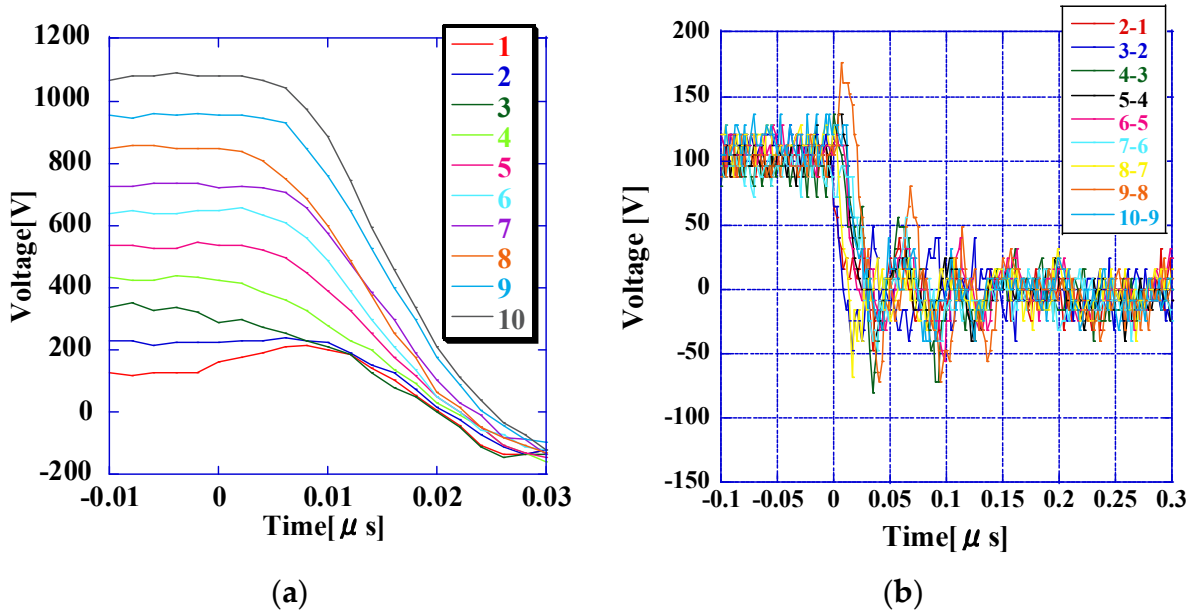
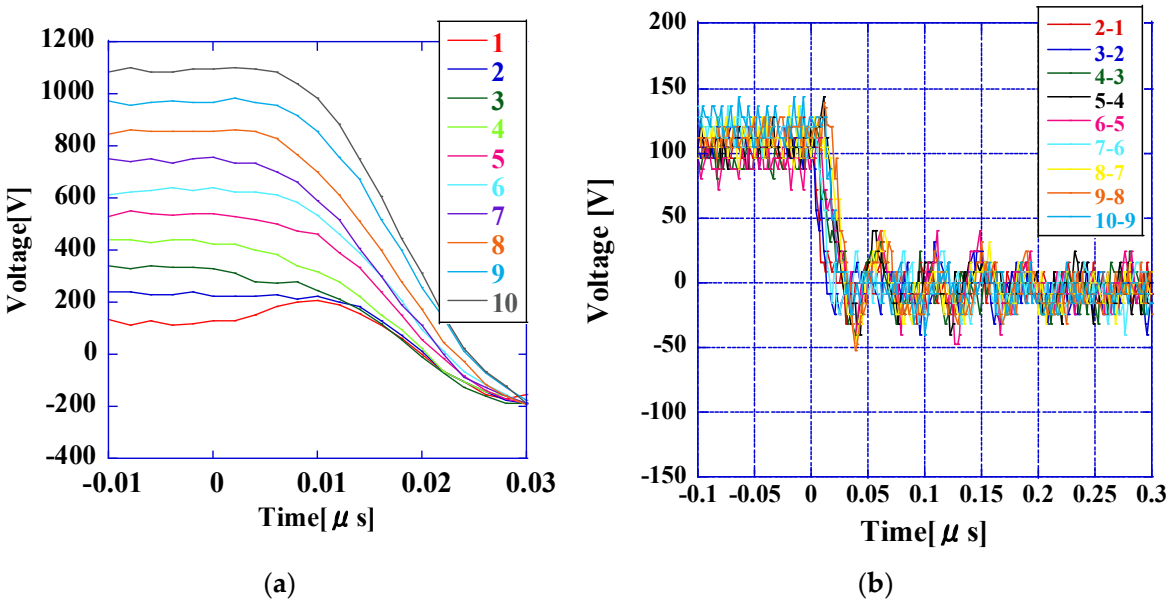


Figure 2. (**a**) The voltage waveforms for each semiconductor during the off state and turn-on state at R_G = 3.6 Ω. (**b**) The voltage waveforms for each semiconductor during the off state and turn-on state at R_G = 3.6 Ω.

Figure 2b illustrates the waveforms comparing the voltage differences applied to each semiconductor element, representing the potential difference at each stage. The voltage before adjusting the gate resistance ranged from a maximum of 182 V to a minimum of −80 V. A negative voltage indicates the application of reverse voltage to the semiconductor.

Therefore, an attempt was made to adjust the falling voltage waveform by changing the gate resistance R_G of the grading semiconductor. Gate resistors serve as charging resistors for the gate's MOS capacitor. By adjusting the gate resistors for each stage to equalize the charging time for electric charge, the falling edges of the voltage for each semiconductor are made uniform. Figure 3a shows the voltage waveforms of the grading semiconductors when the gate resistance R_G was changed to align the falling edge of each stage. It was confirmed that the voltage divider voltage of the third stage became higher than before changing the gate resistor.



(**a**) (**b**)

Figure 3. (**a**) The voltage waveforms for each semiconductor at the off and turn-on states after adjusting R_G. (**b**) The voltage waveforms for each semiconductor at the off and turn-on states after adjusting R_G.

From Figure 3b, it is evident that adjusting the gate resistance reduces the maximum voltage to 144 V and the minimum voltage to −51 V. This test shows that the voltage drops of each stage can be matched by adjusting the gate resistors.

3.1.2. Improved Circuit Isolation Performance Semiconductor Devices for Increased Operating Frequency

An operational test was conducted using a circuit modified to increase the isolation voltage in the gate circuit. The output waveforms are shown in Figure 4. The output voltage was 10 kV with a rise time of 800 ns and a fall time of 58.6 μs. This enabled stable gate voltage output at a frequency of 200 Hz. However, the temperature rose to the rated temperature of the semiconductor when operated above 200 Hz.

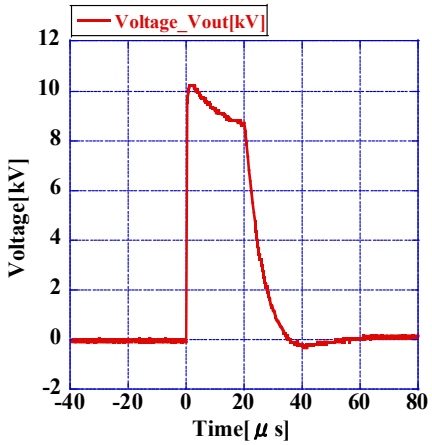


Figure 4. Output voltage waveform. The waveform rises when the semiconductor is turned on and falls rapidly when it is turned off.

3.1.3. Connecting a Charging Resistor and Capacitor to Increase the Operating Frequency

The output voltage rises immediately after the semiconductor turn-on phase, and then it is discharged from the capacitor to the load resistor, resulting in a gently falling output voltage waveform, as shown in Figure 5. During continuous operation, the maximum

operating frequency is 200 Hz due to the temperature rise of the semiconductor, making stable operation over a long period of time difficult. However, when the device was operated for short periods of time, up to about 1 min, the maximum operating frequency increased to 430 Hz.

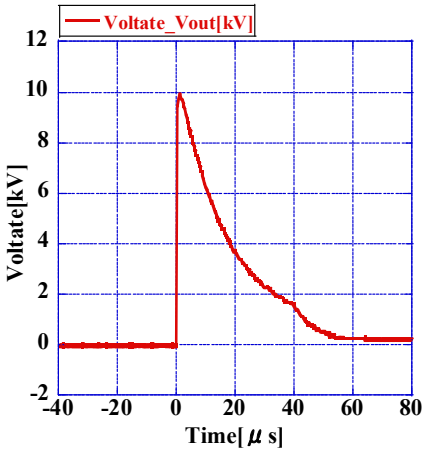


Figure 5. Output voltage waveforms after connecting capacitors and charging resistors. The waveform rises immediately after semiconductor turn-on phase and then falls gently.

3.2. Connecting a Saturable Inductor

3.2.1. Saturation Time Setting

In the previous section, we increased the maximum operating frequency at which 10 kV can be applied by connecting a charging resistor and capacitor. However, continuous voltage application may lead to a sudden increase in semiconductor temperature and cause destruction. To address this issue, we attempted to suppress the rise in semiconductor temperature and increase the maximum frequency for continuous operation by connecting a saturable inductance to the circuit.

Figure 6a shows a graph comparing the saturation time and output voltage for magnetic cross-sections of 1290 mm^2 and 645 mm^2. At an output voltage of 10 kV, the saturation times were 7.1 μs for the 1290 mm^2 cross-section and 4.3 μs for the 645 mm^2 cross-section. Although not exactly halved, these values were close to the theoretical values shown in Equation (4). Since the semiconductor turn-on time is 590 ns, a cross-section of 645 mm^2 is appropriate. The output waveform is shown in Figure 6b.

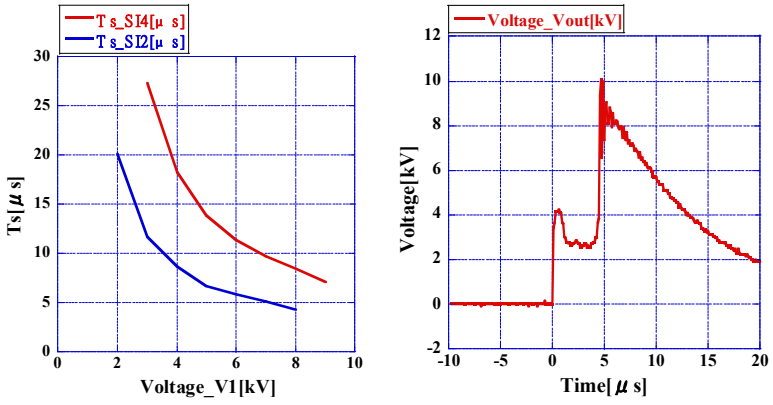


Figure 6. (**a**) Comparing saturation time for different cross-sections. Saturation time is reduced by approximately half by changing the cross-sectional area. (**b**) Output voltage waveform after connecting the saturable inductance. Saturation time is provided before the output voltage reaches its maximum.

3.2.2. Power Consumption Measurement to Confirm the Power Consumption Reduction by Connecting the SI

We calculated each power consumption using the voltage–current–time curve depicted in Figure 7. The specific method for calculating power consumption is as follows. We employed the numerical data that fell below the voltage–current–time curve and, for each infinitesimal time interval, computed the power consumption as the product of voltage and current at that moment. We then determined the average power consumption over these infinitesimal time intervals and accumulated this average power over the duration during which power was consumed, resulting in the total power consumption. Table 1 shows the results of power consumption measurements. During the turn-on phase, the power consumption decreased due to the lower voltage applied to the semiconductor. During the turn-off phase, the current value was very small, less than 0.4 A, the minimum current that can be measured with an oscilloscope. This is so small compared to the turn-on phase, and on timing currents that it was set to 0 W. This test showed that SI is effective in reducing power consumption.

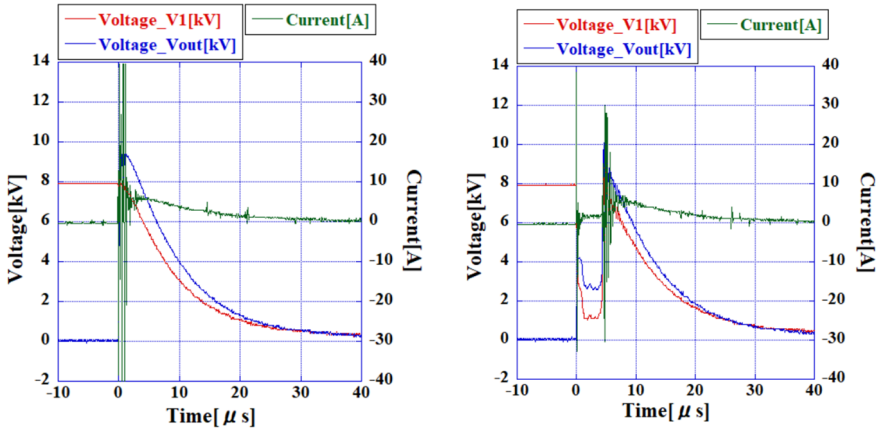


Figure 7. (**a**) Without SI connected, the voltage–current–time curve used to obtain power consumption. (**b**) When SI is connected, the voltage–current–time curve used to obtain power consumption.

Table 1. Power consumption under each condition. Power consumption was reduced after connecting the SI during both the turn-on and turn-off phases.

	SI No Connection [mW]	SI Connection [mW]
turn-on	23.79	15.74
on	96.16	74.97
off	0	0

3.2.3. Semiconductor Temperature Measurement to Confirm the Change in Temperature Characteristics of Semiconductors by Connecting the SI

Since it was confirmed in the previous section that the power consumption of the semiconductor was reduced, the operating frequency was increased, and the temperature of the semiconductor was measured. The temperature change graphs for each condition are shown in Figure 8. From Table 2, it is evident that connecting the SI results in a temperature reduction of more than 10°C. The temperature rise of the semiconductor was reduced by connecting the SI. When SI was connected to increase the operating frequency, it was observed that the Snubber resistor burned out. Consequently, the Snubber resistor was replaced with a resistor of higher power capacity, and stable operation up to a repeat frequency of 300 Hz was confirmed. Furthermore, operation at 310 Hz resulted in the breakdown of semiconductor devices.

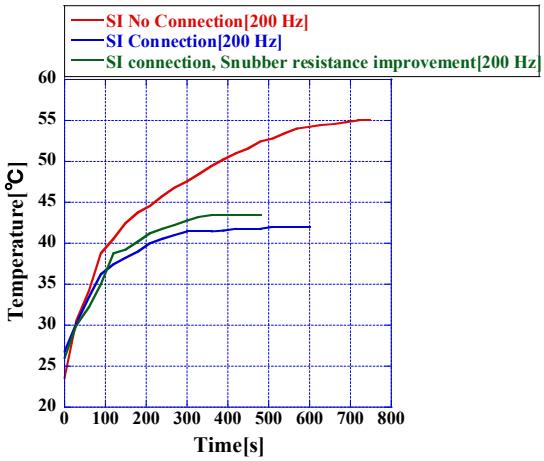


Figure 8. Temperature changes under each condition. The maximum temperature was reduced by connecting the SI. The time to reach the maximum temperature was also reduced.

Table 2. Maximum temperature under each condition. It was found that the temperature was reduced by more than 10 °C.

	Maximum Temperature [°C]
SI No Connection [200 Hz]	55.0
SI Connection [200 Hz]	42.0
SI Connection, Snubber resistance improvement [200 Hz]	43.4

3.3. Test of Increasing the Number of Semiconductor Connection Stages to Increase Output Voltage

The circuit created in this study consists of a gate circuit, semiconductors, the Snubber circuit, and voltage divider resistors, and the output voltage of 10 kV was confirmed by connecting three stages in series. In this test, the number of stages was increased to six to attempt switching with a higher output voltage. As shown in Figure 9, an output voltage of 20 kV was achieved by increasing the number of stages to six. However, the waveform, which should be a square wave, is attenuating. This is likely due to the voltage applied to the load decreasing as a function of the product of the load resistance and the capacitor.

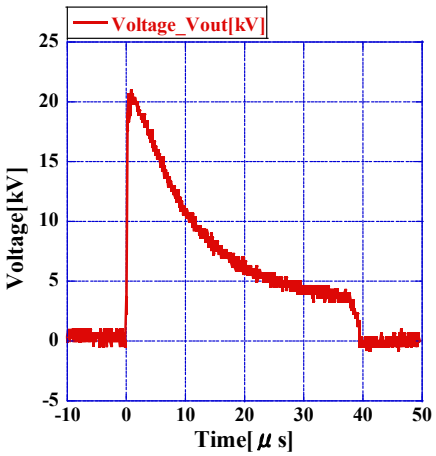


Figure 9. Output voltage after increasing the number of stages. The output voltage reached 20 kV by increasing the number of stages.

3.4. Test of a Semiconductor Series-Connected Circuit to Change the Pulse Width of Output Voltage

By using two semiconductor series connection circuits, a circuit that can change the pulse width to an arbitrary value was created. To change the pulse width, a semiconductor series-connected circuit was connected in parallel to a load resistor. The signal from the function generator is sent to the circuit connected in parallel with the load resistor with a delay of the pulse width to be output. This causes a current to flow in the circuit on the load resistor side, and no voltage is applied to the load resistor. This made it possible to change the pulse width of the pulse voltage applied to the load resistor. Figure 10 shows the output voltage waveforms changed to pulse widths of 5 μs, 20 μs, and 30 μs. To make the pulse output waveform more similar to a square wave, the capacitor connected in parallel to the main circuit was removed. In this study, switching beyond the rated voltage of the single discrete semiconductor became possible. This makes it possible to apply the device to a circuit that changes the pulse width.

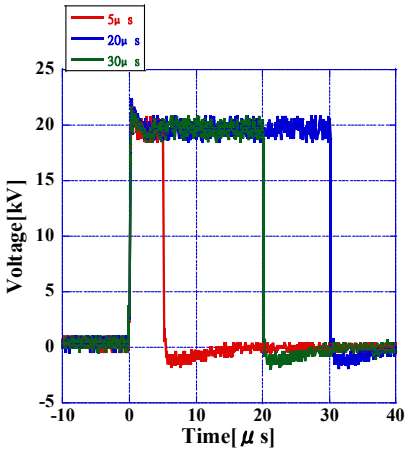


Figure 10. Pulse width change test. By connecting the semiconductor series connection circuit to the load resistor side as well, it became possible to apply an output voltage with an arbitrary pulse width.

4. Conclusions

In this study, semiconductor series connection tests were conducted to develop a pulsed power supply capable of outputting high voltage. A Snubber circuit was connected as a method of series-connecting the semiconductors to facilitate their turn-off phase, thereby balancing the voltage divider of each semiconductor and achieving switching beyond the rated voltage. Initially, a test was conducted to equalize the voltage divider by varying the gate resistance. As a result, it was possible to equalize the falling edge of the voltage in each stage. In the test for increasing the insulation voltage at the gate resistance, the insulation voltage was changed from 2500 V using the TLP350 to 3750 V using the TLP350. By connecting a pulse transformer between the function generator and the photocoupler, an operating frequency of 200 Hz was achieved. Further testing involving the addition of a charging resistor and capacitor enabled the maximum operating frequency to be increased to 430 Hz within a short period of time.

The concern in this study was the Snubber loss generated by the Snubber circuit, which caused an increase in the temperature of the semiconductors. To address this, the SI was connected to delay the rise of current and shift the voltage fall and current rise during the turn-on phase, aiming to reduce power consumption. In the power consumption measurement test, the power consumption before connecting the saturable inductor was 23.79 mW at the turn-on phase and 96.16 mW during operation, whereas after connecting the SI, the power consumption decreased to 15.74 mW at the turn-on phase and 74.97 mW during operation. This indicates that the SI is effective in reducing power consumption at both turn-on phase and operation times. In the temperature measurement test, the maximum temperature decreased from 55.0 °C before connecting the SI to 42.0 °C after

connection, confirming improved temperature characteristics. The power consumption measurements and temperature characteristic tests demonstrated the effectiveness of this method in reducing power consumption and improving temperature characteristics. Despite using a magnetic material as the SI, the cross-sectional area was approximately 60% smaller than that used for a transformer in a conventional MPC power supply, enabling a smaller circuit.

Furthermore, in a test to increase the output voltage by adding more semiconductor stages, an output voltage of 20 kV was confirmed by connecting six stages. Moreover, since the series connection of the semiconductors enabled switching beyond the rated value, two of these circuits were used to create a circuit that can be adjusted to any pulse width. As a result, the pulse width can be changed to 5 μs, 20 μs, and 30 μs.

Compared to existing semiconductor series connection circuits, the proposed semiconductor series connection circuit with the SI can reduce switching losses. This helps in controlling the temperature rise of the semiconductor, enabling prolonged operation. Consequently, it contributes to applications requiring high-repetition, high-voltage applications for sterilization, ranging from several hundred Hz to several kHz. The proposed semiconductor series connection circuit allows for the adjustment of the output voltage by varying the input voltage. Additionally, increasing the number of semiconductor stages can increase the maximum output voltage. Existing pulse sources, such as the Marx generator, have limitations as they can only output voltages that are multiples of the charging voltage of the capacitors, making fine voltage adjustments difficult. In comparison, the proposed semiconductor series circuit allows for precise output voltage adjustments.

In this study, we did not propose the pulsed power supply as a converter. However, the series connection of semiconductor elements using the SI in this work can increase the input-side primary voltage. With the increase in the primary voltage, it is expected that the output voltage can be raised without the need to increase the converter's switching frequency. However, since the SI itself contains inductance components, there is a possibility that it may lead to an increase in surge voltage during switching. If it were possible to minimize the inductance during saturation, the introduction of the SI as one of the elements in the inverter configuration could be anticipated.

To further increase the operating frequency in the future, considerations will be made to increase the power supply capacity on the charging power supply side and develop a structure that electrically separates the charging side and the main circuit side during the turn-on phase. In this circuit, we achieved an increase in operating frequency by using the SI. However, to further increase the frequency, an increase in the charging capacity is required. In the current circuit, capacitors were charged through charging resistors, meaning that a charging current always flows even during the semiconductor's on-time. Previously, we controlled the charging source using a gate controller and electrically disconnected the charging side, thereby increasing the input capacity of the power source [60–62]. This control allows us to increase the input capacity of the power source proposed in this study. Furthermore, as the number of stages increases, the output voltage increases, necessitating improved insulation. This can be achieved through circuit enhancements such as changing the substrate material from paper phenolic to glass composite.

Should we extend the number of semiconductor stages to amplify the output voltage, it becomes imperative to augment the circuit's insulation capabilities. Within the Snubber circuit, in instances where a surge voltage of such magnitude proves unassimilable, the parallel incorporation of spark gap switches [63,64] into the principal circuit can be employed to avert heightened voltage surges. Moreover, the adoption of insulating oil with heightened fluidity [65] and the integration of an additional cooling system to enhance semiconductor cooling serves to diminish the temperature of the cooling medium, thereby enabling the generation of even loftier voltages. Through the execution of these methodologies, the realization of a further augmentation in the output voltage becomes a tangible possibility.

The intended application for the developed pulsed power supply is the application of high-voltage pulse exposure for the purpose of sterilization. High-voltage electrical pulses induce electroporation of cell membranes, leading to a transient increase in membrane permeability when cells are exposed to them [66,67]. As the number of pulses and the amplitude of the electric field increase, irreversible electroporation occurs, and the sterilization intensity is enhanced due to Joule heating. However, when the target for sterilization is a liquid containing proteins, it is necessary to control this heat to minimize thermal damage [68,69]. By varying the pulse width, this heat can be adjusted, allowing the derivation of electrical parameters that achieve the optimal sterilization intensity. Furthermore, it is known that changing the frequency can alter the cellular response to the electric field [70,71], and the ability to easily vary the pulse width even with changes in circuit length is a characteristic of this system. With the realization of this circuit, the pulse width of the gate voltage can be readily adjusted, addressing a previously challenging issue. This capability opens up new possibilities for applications such as cell and gene transfection.

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