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Single Power Supply, Compact, Self-Adaptive Dynamic Range Lock-In Amplifiers

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Abstract: To meet the high dynamic voltage or current range measuring in real-time in the modern electrical industry, ranging from the surface science to non-destructive testing, this paper reports two broad dynamic ranging, universal, and compact digital lock-in amplifier methods for the huge dynamic range signal, termed as the hybrid and all-digital amplifiers. Both have reduced the complex components required in the traditional amplifiers to only two or three components without sacrificing the measuring accuracy, even by less than 0.05% in some situations, which has been evaluated via simulations and experiments with the FPGA circuit. Additionally, benefiting from the single-power supply strategy, the proposed methods are suitable for portable devices, including the pocket spectrometer, mechanical resonator monitor, and powered on battery. Such results in this paper illustrate the phase coherent technology with a compact, universal, and integrated circuit with a promising future.

Keywords: digital circuit; coherent theory; embedded signal processing

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1. Introduction

The lock-in amplifier (LIA) is a specialized electronic instrument utilized to capture weak, low-frequency signals in the presence of heavy noise in scientific research, engineering, and industry. Due to its high sensitivity, accurate recoverability, real-time ability, and narrow versatility [1] from the coherent detection theory, the applications of the LIA include biomedical signal recovery [2], geophysical surface science [3,4], magnetic field measuring [5], frequency response analysis [6], gravitational wave detection [7], environmental infrastructure monitoring [8], and optical spectroscopy caption [9]. Each of these applications requires the use of an LIA capable of seizing the weak signals buried under the heavy noise while reserving the high dynamic ranges (the ranges of signal, signal-to-noise ratio). Various techniques and algorithms have been investigated to overcome the traditional LIA shortages, ranging from the cost, sophisticated components, and bulkiness to the excessive power consumption [10–12]. There are three basic or main categories of LIA designs, which can be broadly characterized as the analog, digital, and hybrid ones [13–15]. Benefitting from the accelerating development of the integrated circuit, the digital ones, especially the integrated LIA at CMOS-level design, have attracted increasing attention in mobile devices with milliwatt or even microwatt power consumptions [16–18]. Alternatively, since the amplitude of the desired signal is much more meaningful than its initial phase part, the absolute design has been introduced [19]. Given that hybrid circuits leverage the strengths of digital circuits, which excel at handling discrete values and performing complex logic operations, with the advantages of analog circuits, which are highly efficient at processing continuous signals and interfacing with the real world [20–22], this technique illustrates a promising future among sensing, electromagnetic measuring, and weak optical signal detecting.

However, despite this critical significance, there has been no published systematic investigation into the methods of absolute voltage or current measuring range [23,24]. An

ideal version of such a method would meet the following requirements [25]: the high dynamic range, as the method should be applicable both in the weak signal and relatively high signal detections without sacrificing accuracy; the signal extraction, as it is convenient to modify the design for various applications, including the sensing, spectrum capturing, and mechanism measuring; the frequency selectivity, which means that the reference frequency can be selected easily, enabling the system to isolate and amplify the required signal at a given frequency; the phase sensitivity, as the reference signal should adjust its phase to the required signal smoothly; the power consumption; system complexity; multi-channels; and so on.

In this paper, inspired by the pulse width modulator (PWM) [26,27], the all-digital and analog hybrid, self-adaptive dynamic ranging LIA designs for in situ applications have been proposed to meet almost all of the above desires. In order to determine the method's feasibility and to further explore its high dynamic range in the engineering area, the method was implemented using an electric system illustrated in the following part. Both the systematic simulation and experimental investigation were then conducted under various conditions. In the experiments, the Field Programmable Gate Array (FPGA) is utilized to complete the digital signal processing, the ANALOG DEVICES^{TM} analog-to-digital converter (AD7760, 24bit) is introduced to provide the input signal for the experimental system, and a USB is used to exchange the data and commands between the LIA board and a personal computer (PC). The detailed results of this investigation are described below. Overall, the method as implemented takes fewer calculating resources and extra components than the traditional method without sacrificing the measuring accuracy for the given situations.

2. Theory and Methods

2.1. Overview

Figure 1 illustrates the block diagram of the two-channel LIA where the left and right are the in-phase and quadrature channels, respectively. And the original signal is enlarged by an amplifier and then sent to the in-phase and quadrature processing channels, and the modulated frequency of the original signal is shared by the referencing channels as well. The input signal that contains the desired amplitude and initial phase information flows through two channels, and its results can be extracted after the signal processing. There are the following parts in detail: the desired input signal, termed as $o(t)$, which is modulated at the given frequency f_s and contains the unwanted noise; the pre-amplifier is introduced to enlarge the original signal as $x(t)$; the two orthogonal references, including the two in-phase and quadrature components that are with the same frequency f_r, named as $r_p(t)$, $r_q(t)$, respectively; the phase sensitive detector (PSD), which is implemented with an analog or digital multiplier generally and its outputs are $m_p(t)$ and $m_q(t)$; the narrow bandwidth low pass filter (LPF), ensuring that only the processed signals with the desired frequency, $l_p(t)$ and $l_q(t)$, would pass; and the calculating module is utilized to interpret the magnitude, $A(t)$, and phase information, ϕ_s, of the original signal.

From the coherent measuring theory, it is clear that only when f_s equals f_r, the desired signal can be extracted by the LIA. And then the mathematical relations can be expressed as

$$o(t) = s(t) + n(t) + V_{bias} \quad (1)$$

where $s(t)$, $n(t)$, and V_{bias} are the signal wanted, system noise, and bias voltage, respectively. And the signal is

$$s(t) = A_s \sin(2\pi f_s t + \phi_s) \quad (2)$$

where A_s and ϕ_s are the magnitude and initial phase of the signal.

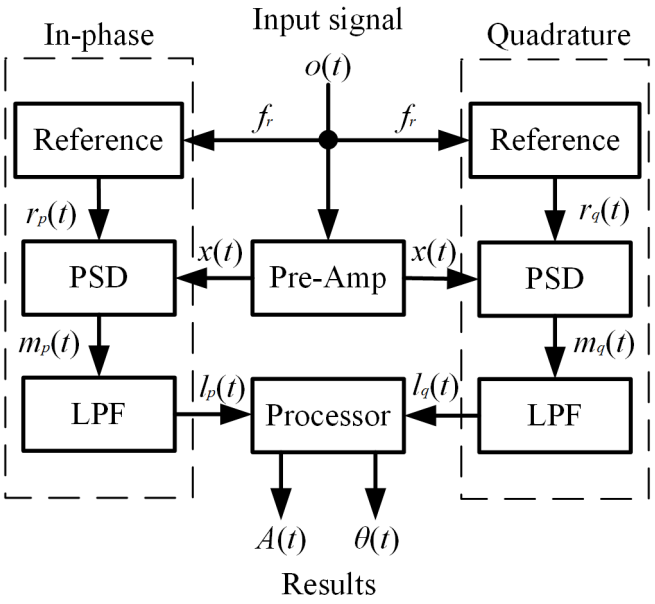


Figure 1. The LIA block diagram; the parameters for the In-Phase and Quadrature channels are the same. Pre-Amp, pre-amplifier utilized to enlarge the original signal; PSD, phase sensitive detector; LPF, low-pass filter.

Given that the gain of the pre-amplifier is K, and the amplitudes of reference are A_r, then the relations of the components can be illustrated as

$$x(t) = Ko(t) \tag{3}$$

$$\begin{aligned} r_p(t) &= A_r \sin(2\pi f_r) \\ r_q(t) &= A_r \cos(2\pi f_r) \end{aligned} \tag{4}$$

Considering that the mixer, or the multiplier, is implemented as the simplest PSD, then its outputs are

$$\begin{aligned} m_p(t) &= \tfrac{1}{2} K A_r \, A_s[\cos(\phi_s) - \cos(4\pi f_r t + \phi_s)] + n'(t) \\ m_q(t) &= \tfrac{1}{2} K A_r A_s[\sin(\phi_s) + \sin(4\pi f_r t + \phi_s)] + n'(t) \end{aligned} \tag{5}$$

where $n'(t)$ is the modulated noise by the PSD.

After the LPF, only the low frequency parts in $m_p(t)$ and $m_q(t)$ would remain as

$$\begin{aligned} l_p(t) &= \tfrac{1}{2} K A_r \, A_s[\cos(\phi_s)] + [n'(t)]_{lfp} \\ l_q(t) &= \tfrac{1}{2} K A_r A_s \, [\sin(\phi_s)] + [n'(t)]_{lfp} \end{aligned} \tag{6}$$

Benefiting from the narrow passband of the LPF utilized in the LIA, the system noise would be suppressed only in such spectrum as $[n'(t)]_{lfp}$.

Additionally, to maintain the same performance of the two channels, both the PSDs and LPFs implemented in LIA are supposed to share the same parameters.

If the influence of the narrow bandwidth noise left in the LPF has been ignored, the outputs of the LIA can be expressed as

$$A_s = \frac{2}{K A_r} \sqrt{l_p^2(t) + l_q^2(t)} \tag{7}$$

$$\phi_s = \tan^{-1}\left[\frac{l_q(t)}{l_p(t)}\right] \tag{8}$$

Since the initial phase information in some measuring applications is not as important as the amplitude part, only the magnitude detection, A_s, is discussed in this paper.

2.2. Self-Adaptive Theory

Considering the block diagram shown in Figure 1, there are several improvements made by the researchers, including the pre-amp, PSD structure, and the choice of the processor [27–29]. Different from the general direct current (DC) signal measuring, the LIA is proposed to capture the active current (AC) signal to extract the weak ones that are even at nanovolts [30]. Traditionally, there are ways to capture the AC signal desire dual supply voltages in the following two practices: one takes positive and negative voltage as the power supplies, and the other uses two positive voltages as the power supply and bias, respectively, to lift the original AC signal into the system dynamic range [5,16]. To reduce the power consumption in the LIA, various approaches have been proposed, ranging from integrated analog CMOS technology to the rectified signal single power supply [13,17] in battery-operated systems. However, the analog method must work at a constant frequency, which limits the applying areas; the rectified method requires an accurate phase shifter to invert the negative signal to the positive.

The pre-amplifier in a digital LIA system plays a significant role to build the bridge between the original signal and the ADC, which is the key part to convert the original input signal to the working voltage or current range of ADC. To overcome the previous problems, a single power supply design has been proposed, in which the Pre-Amp part has been modified with a single power supply, V_{DD}, as shown in Figure 2. And such voltage can be used for the other components as well.

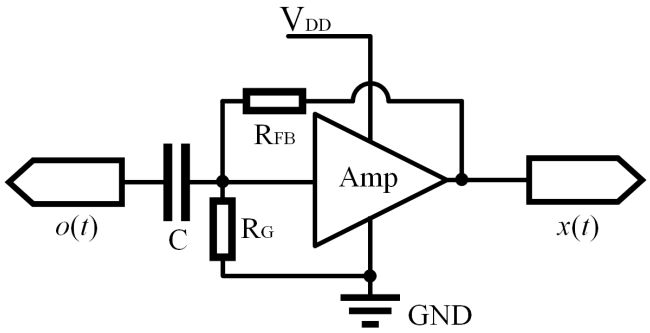


Figure 2. The modified pre-amplifier diagram. C, capacitor utilized for AC couple; VDD, single power supply; RFB, RG, resistors for the amplifier gain.

Inspired by the PWM theory, the duty cycle of the periodical signal is sufficient to represent the phase, amplitude, or period values in various applications [26,27,31]. Then, for the amplitudes of $o(t)$ that are greater than V_{DD}, the relations between the input and output of the modified Pre-Amp can be illustrated as in Figure 3.

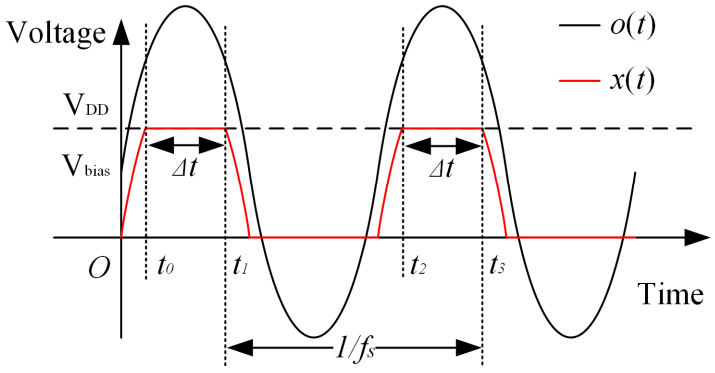


Figure 3. The input and output relation of the modified Pre-Amp. Vbias, bias voltage of the input original signal, $o(t)$; VDD, single power supply.

It is clear that the C in Pre-Amp would erase the V_{bias} in the $o(t)$, and the V_{DD} does not only provide the power supply for the amplifier, but also works as a threshold for the Pre-Amp. Then, from Equations (1) and (2), the mathematics can be expressed as

$$x(t) = \begin{cases} o(t) & 0 < o(t) \leq V_{DD} \\ V_{DD} & o(t) > V_{DD} \\ 0 & others \end{cases} \tag{9}$$

As the proposed design shown in Figure 2, the C is introduced to remove the original bias voltage influence, and the signal would be modulated by the V_{DD} to the PWM-like pattern as shown in red. Additionally, it is clear that the greater the magnitude of $S(t)$ is, the more V_{DD} signal of $x(t)$ contains as follows:

$$d = \Delta t \times f_s \in [0,\ 0.5) \tag{10}$$

where $\Delta t = t_3 - t_2 = t_1 - t_0$, and f_s is the frequency of the desired signal.

Then, for the signal with an amplitude, A_s, greater than the V_{DD}, its amplitude can be expressed as

$$A_s = \frac{V_{DD}}{\sin\left[\pi\left(\frac{1}{2} - d\right)\right]} \tag{11}$$

Considering that the d ranges from 0 to 0.5, the corresponding amplitude that can be captured in the proposed system ranges from 0 to infinity, and the accuracy of the d determines the measuring resolution.

Additionally, since the positive original signal part, $o(t) > 0$, contains the amplitude information, it is easy for the proposed self-adaptive LIA design signal to extract such values when the maximum of the original signal is less than V_{DD}.

Finally, there are two ways to complete the self-adaptive dynamic range LIA: all digital and hybrid designs, which are described in detail as follows.

2.3. All-Digital Implementation

As introduced in the above part, considering that the precise duty cycle, d, is sufficient to extract the desired magnitude for some measuring situations, and the comparator is almost the simplest digital component utilized in the electrical circuit, then, the Pre-Amp can be modified as shown in Figure 4. Additionally, both the PSD and LPF in I-Q channels are not required anymore in this method. For such a method, its input analog signal is quantified by a comparator and digital counter, which means that the ADC utilized in the general digital LIA is not necessary, or the analog modulated signal can be converted to all-digital ones. To illustrate the relationship between the comparator and the quantified digital counter understandably, there is an example depicted in Figure 5. The signal processing can be completed with a counter in the digital system, where the cnt[n] represents the counting value for the duty cycle as

$$d = c \times T_c \times f_s \tag{12}$$

And c, T_c, and f_s are the counter values, clock period for the system sampling and processing, and signal modulating frequency, respectively.

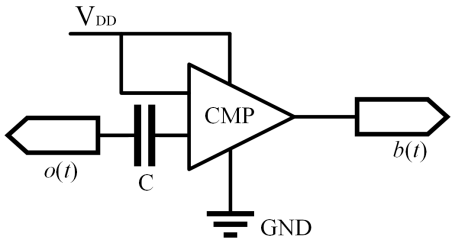


Figure 4. The modified Pre-Amp as the comparator. C, capacitor; CMP, comparator; input original signal, $o(t)$; VDD, single power supply; binary output signal, $b(t)$.

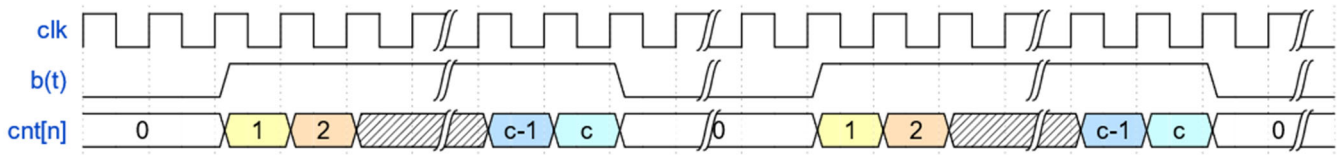


Figure 5. The timing relation among the $b(t)$, cnt[n], and clock. clk, the system clock; c, the counter value corresponds to the duty cycle; the colors represent different counter values.

In the all-digital design, it is clear that the CMP works as a bridge to convert the original analog signal to binary values [32]. From Equation (11) and Figure 5, the measuring accuracy of such a design is determined by the duty cycle accuracy. For a digital system, the above accuracy depends on the relative time resolution, R_t,which can be defined as follows:

Apart from the limitation of the traditional PWM theory such as system clock frequency, $1/T_c$, the measuring resolution of such a design is determined by the modulating frequency, f_s, of the desired signal as well.

$$R_t = T_c \times f_s \tag{13}$$

Then, the all-digital LIA block diagram can be simplified as in Figure 6, and the magnitude measuring at the voltage or current level has been converted to the time measuring.

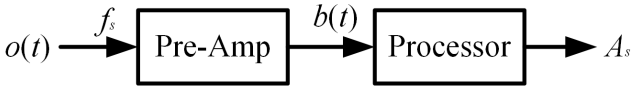


Figure 6. The all-digital LIA design block diagram. The signals are similar to the ones in the block diagram.

Besides the PWM time resolution, the accuracy of the sinusoid calculation in Equation (11) would also affect the result. For portable equipment with an embedded processor, since its calculating source is small-scale, the look-up table (LUT) can be implemented to complete the computation.

2.4. Hybrid Implementation

Different from the all-digital design mentioned above, the hybrid implementation contains the basic structure of the traditional LIA and relatively complex digital signal processing calculations as follows:

Firstly, the Pre-Amp shown in Figure 2 is utilized to achieve the self-adaptive ranging goal. However, from the Fourier Transform theory, the modified $x(t)$ in Equation (9) can be described as

$$x(t) = \frac{a_0}{2} + \sum_{n=1}^{N} [a_n \cos(2\pi n f_s t) + b_n \sin(2\pi n f_s t)] \tag{14}$$

where f_s is the modulating frequency of the original signal. There is no doubt that all the parameters, both a_n and b_n, are partial to the magnitude, A_s, of the original one. Thus, the first-order coefficients, a_1 and b_1, can be used to acquire the desired magnitude rather than the whole parameters in Equation (14). Additionally, because of the narrow bandwidth selection of both the PSD and LPF in LIA, the coherent signals with higher order would be suppressed at a relatively low level, and the A_s can be obtained as Equation (7) with a modulating coefficient.

Furthermore, as mentioned in Section 2.2, both the hybrid and all-digital designs are proposed to extend the measuring dynamic range, simplify the structure, and reduce the power consumption in the traditional LIA. Rather than the comparator in the all-digital method, the analog-to-digital converter (ADC) plays a significant role in building the bridge between the original signal and digital values. Traditionally, the input range of the ADC with the Pre-Amp determines the digital LIA dynamic range. Given that such a design

is sufficient to cover the desired range, the voltage resolution, or the digital resolution, decreases with the attenuating rate of Pre-Amp increasing. However, the linear relationship between the analog and digital signals is not a perfect solution to fully use the ADC input range for huge voltage range measuring situations.

As for the PSD and LPF, both of them can be completed with the digital structure as a digital multiplexor and LPF, respectively. And benefiting from the digital design, all the parameters, including time constant, reference frequency, and attenuating ratio, can be set for various situations to optimize LIA performances. Apart from the LPF, an average or mean filter, with a window size W_m, is added to the system to suppress the system noise further. There is no doubt that the hybrid design can be modified as the all-digital one when the ADC is modulated as a comparator.

Finally, to illustrate the performance of the proposed design, both the simulating and experimental results have been attached in the Section 3.

3. Simulating and Experimental Results

To validate the described self-adaptive dynamic range LIA method and evaluate its performance, both the simulation and experiment have been completed as shown in the following parts.

3.1. Simulations with Various Settings

In the simulations, to complete the fast data extraction goal in real time, the system is implemented with the 625,000 samples/second sampling rate ADC, and then, the simulation rate is selected as the same value. Additionally, there are extra parameters to complete the simulations: firstly, for the input signal, including the amplitude (A_s), initial phase (ϕ_s), and modulated frequency (f_s); in addition, for the referencing channels, including the amplitude (A_r) and frequency (f_r); apart from the above, for the hybrid and all-digital methods, the single power supply, V_{DD}, which is supposed to be less than the input signal's amplitude; and since the performance of the LPF implemented determines the final results, the more narrow the passband is (F_c, F_{stop}), the less system noise there is, which leads to more accurate results; furthermore, benefiting from the flexibility of the digital system, both the passband of the LPF and the averaging window, which determine the time constant, can be modified easily. To compare the performances of the proposed methods in various situations, the signal-to-noise ratio (SNR) is set with different values. And the following parameters shown in Table 1 are utilized to express the proposed design, where the SNR can be defined as

$$\text{SNR} = 20\log_{10}\left(\frac{A_s}{A_n}\right) \tag{15}$$

where A_n is the square root of the equivalent noise voltage.

Table 1. Parameters utilized in simulations.

Symbol	Values	Units
A_s	0–10, 0.5 step	a. u.
ϕ_s	$\pi/3$	Rad
f_s, f_r	1200	Hz
A_r	1	a. u.
V_{DD}	3	a. u.
F_c	100	Hz
F_{stop}	200	Hz
SNR	$-40, -20, 0, 20, 40$	dB
W_m	200	Sample
Sampling rate	625,000	Samples/s
Simulating time	2	s

The results are shown in Figure 7, in which the four methods are simulated at various A_s and SNR values, including the traditional, half-wave, hybrid, and all-digital methods. To quantify the average error, the Normalized Mean-Square Error (NMSE) is used [33], which takes the range of the data into account, and evaluates the accuracy of the prediction model. And the smaller the NMSE value, the more robust the performance of the system is in terms of accuracy. The formula for NMSE is

$$NMSE = \frac{\sum_{i=1}^{n}(\overline{y_i} - y_i)^2}{\sum_{i=1}^{n} y_i^2} \times 100\% \tag{16}$$

where n is the number of samples, $\overline{y_i}$ is the average of sample y. For the simulations, the calculated digital results are the samples, y_i, used in Equation (16) with an input amplitude, A_s, equal to 5.

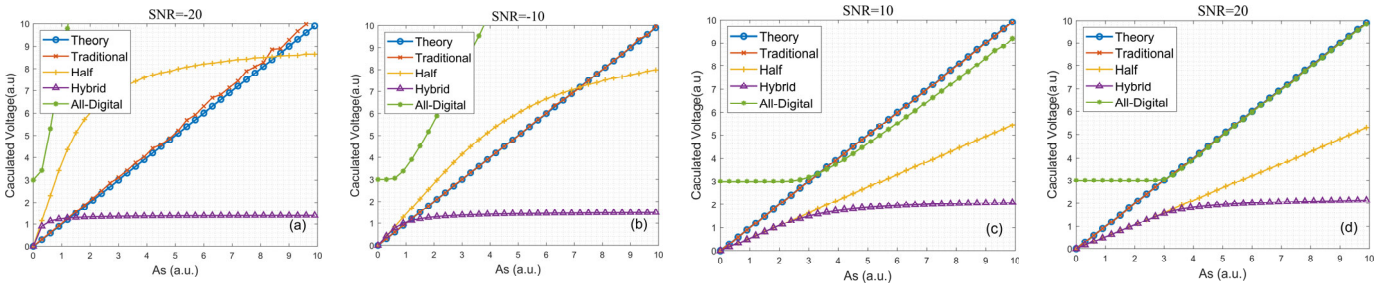


Figure 7. Simulating results for various SNR levels with the different methods; x-axis is the desired magnitude, A_s, and y-axis is the calculated results. (**a**) SNR = −20; (**b**) SNR = −10; (**c**) SNR = 10; (**d**) SNR = 20.

Then, the results are expressed in Table 2 as follows.

Table 2. Quantified in simulation results with NMSE at $A_s = 5$.

Snr	Traditional	Half	Hybrid	All-Digital
−20	2.35%	3.61%	4.42%	0.26%
−10	0.85%	0.95%	1.25%	0.21%
0	0.35%	0.38%	0.38%	0.31%
10	0.27%	0.27%	0.34%	0.19%
20	0.25%	0.26%	0.33%	0.05%

Even though the all-digital method has the lowest NMSE among these methods, which means such a method has a robust working performance, it is not suitable for the low SNR situations as shown in Figure 7. Since the LPF passband set in the simulation is not narrow enough, the traditional one is not sufficient to extract the accurate desired values. However, these four methods are sufficient to acquire the desired amplitude signals with the SNR increasing, and their performances vary distinctively and can be described as follows.

Traditional: there is no doubt that the traditional method shows its stability with diverse SNR levels by following the theoretical values, even if there is some skewness at the lowest simulated SNR.

Half: The only difference between the half-wave and traditional methods is that the negative parts of the original signal are discarded. As the only positive signal is sent to the processing units of LIA, such calculated voltages from the half-wave are about half of the traditional ones and with less noise sustainability than the former.

Hybrid: From the theory section, it is clear that such a method would work as the half LIA when the amplitude of the input signal is less than the power supply, V_{DD}, for the pre-amplifier. As in the zoom-in simulations shown in Figure 8, the corresponding LIA outputs increase nonlinearly with greater amplitudes than V_{DD} increasing.

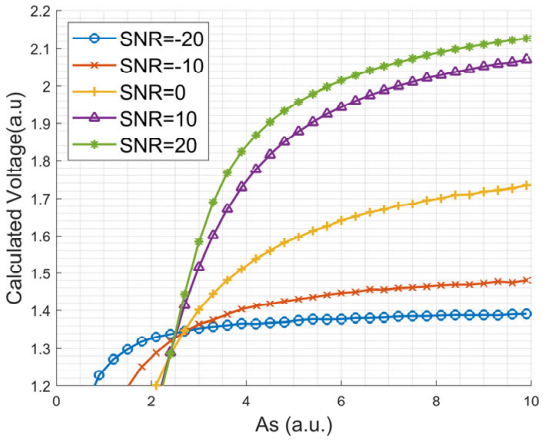


Figure 8. Zoom-in simulating results for hybrid design at the various SNR levels.

All-digital: Even though such a design is not eligible to deal with situations in which the amplitude is less than V_{DD}, or the noise is higher than the desired signals, the all-digital method promisingly reduces the system cost and complexity without sacrificing the accuracy when the SNR level is sufficient for such a design.

3.2. Experiments

To illustrate the proposed designs, some experiments have been completed on the same circuit, and the processing is completed by an FPGA (field-programmable gate array), the Xilinx XC7Z010-400. To minimize the influence caused by components, all the traditional, half, and hybrid methods share the same amplifier (TEXAS INSTRUMENTS^{TM} OPA182), analog-to-digital converter (ADC, AD7760 24bit, 625kSPS, roughly 4Vpp range), and the same LPF parameters that are the 3rd SOS (second-order section) structure, $F_c = 100$ Hz and $F_{stop} = 200$ Hz. Furthermore, there is extra time averaging followed by the LPF output to reduce the undesired vibrations, which is with 200-sample window averaging in the digital embedded system. Additionally, different from the data structure used in the simulations, the processing data in the embedded system are the fixed-point values.

Similar with the setup mentioned in the simulating part, there are some parameters required in the experiments. For the traditional, half, hybrid, and all-digital methods, the only difference between them is the power supply for the OPA182, which is a high-precision, operational amplifier in ultra-low noise, fast-setting, zero-drift, and rail-to-rail devices, as described in Table 3. Since the dynamic range of the ADC is limited in -2 V to 2 V, the power supply for the traditional method is ± 2 V to fulfill it. Then, for the others, the power supply remains almost same. As for the half and all-digital methods, even if they are with the same power supplies, the processing routes vary: the analog values of the former method are kept for mixing and extracting the values in Q and P channels. As for the hybrid method, the half power supply is set to prove the proposed theory in Section 2; the OPA182 in the latter one works as a comparator to modulate the original signal as a step function as shown in Figure 5 for the followed ADC, and then, the desired amplitude can be extracted by using Equation (11). Then, an arbitrary waveform generator is utilized to verify the above methods, and the results are plotted in Figure 9, and the zoom-in results from the hybrid method are plotted in Figure 10. Similar to the simulations, the NMSE is utilized at the $A_s = 2V_{pp}$ situation as shown in Table 4.

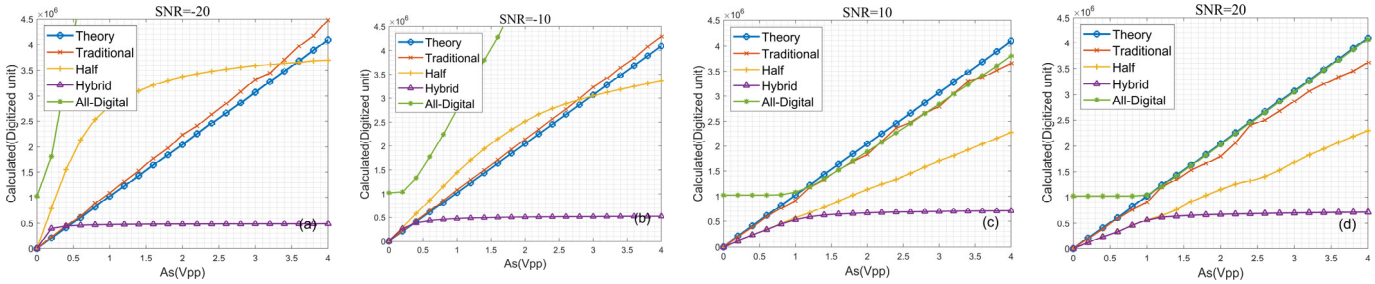


Figure 9. Experimental results for various SNR levels with the different methods; x-axis is the desired magnitude, A_s, with unit Vpp and y-axis is the digitalized results. (**a**) SNR = −20; (**b**) SNR = −10; (**c**) SNR = 10; (**d**) SNR = 20.

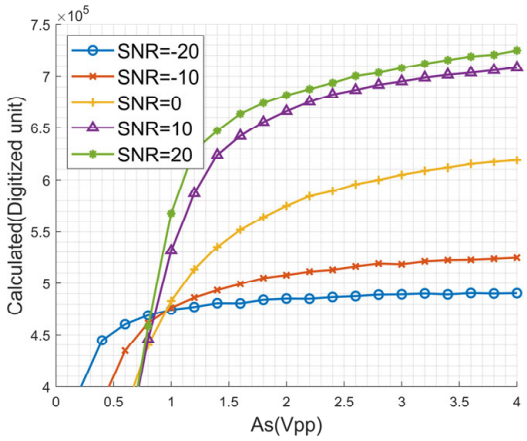


Figure 10. Zoom-in experimental results for hybrid design at the various SNR levels.

Table 3. Parameters and settings in experiments.

Methods	Power Supply for OPA182
Traditional	±2 V
Half	+2 V
Hybrid	+0.5 V
All-Digital	+2 V

Table 4. Quantified in experimental results with NMSE at $A_s = 2V_{pp}$.

Snr	Traditional	Half	Hybrid	All-Digital
−20	4.89%	5.31%	5.42%	0.40%
−10	0.97%	1.95%	1.27%	0.41%
0	0.65%	0.90%	0.37%	0.40%
10	0.49%	0.33%	0.35%	0.17%
20	0.35%	0.26%	0.33%	0.12%

On the one hand, the experimental results share the similar performance shown in the simulating section as both the hybrid and all-digital work well with the SNR at relatively high levels. On the other hand, different from the simulations, the experimental results suffer from the digital accuracy loss that is caused by the fixed-point data in digital systems.

Compared with the traditional method, the hybrid design has expanded the measuring dynamic range greatly by taking the advantages of the nonlinear voltage response. Take the SNR = 20 experiments as an example, the same dynamic ranges are in the traditional and hybrid methods by using the 24-bit and 19-bit digital numbers, respectively. In other words, the latter method can expand the digital LIA measuring range greatly for relatively high SNR situations.

As for the all-digital design, even both the division and sinusoid calculation from Equation (11) are complex to progress in the FPGA platform, and the memory on-chip can be utilized to reduce the complexity using look-up-table (LUT) technology, which means the preprocessed sinusoid and division values can be saved to the memory and selected at processing. In other words, the system measuring accuracy has been converted to the main clock frequency utilized, or the counter accuracy determines the system resolution.

The main resources, including the LUT, DSP, BRAM, and power supply, required in the embedded FPGA system for the above methods can be summarized as in Table 5. Even though the LUT resources increase in the all-digital method, its DSP requirement has reduced. It is clear that compared with the resources used in the traditional and hybrid methods, the resources utilized in the proposed ones have reduced, which would be helpful for portable devices that require an LIA structure in the future.

Table 5. The main resources required for the various methods.

Resources	Traditional	Half	Hybrid	All-Digital
LUT	14,527	14,312	12,268	16,549
DSP	20	20	16	12
BRAM	915	915	623	124
Power number	2	1	1	1

4. Conclusions

To summarize, this work demonstrates the viably integrated lock-in amplifier designs for pocket devices with high accuracy, minimal complexity, and cost, termed as hybrid and all-digital methods. From the observed experimental results, it can safely be concluded that the LIAs can reduce the calculating resources by about 30%, and double the power consumption required in the traditional ones without sacrificing the measuring accuracy for some application situations. Thus, the low cost and digitally integratable nature of both designs are suitable to be integrated with on-battery devices, which will further reduce the system cost, promote the phase coherent theory adoption, and broaden its application areas, such as the in situ current measuring technologies, gas sensors, health monitoring, etc.

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