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Design Techniques for L-C-L T-Type Wideband CMOS Phase Shifter with Suppressed Phase Error

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Abstract: In this study, we designed a K-band CMOS switch-type phase shifter. Equivalent circuits of shift and pass modes were analyzed to minimize phase errors in a wide frequency range. In particular, the impedance inside the equivalent circuit of the pass mode was analyzed to derive a frequency region in which the equivalent circuit of the pass mode becomes an L-C-L structure. Based on the fact that equivalent circuits in shift and pass modes can be regarded as L-C-L structures beyond a specific frequency, a design methodology of the wideband phase shifter was proposed through slope adjustment of the phase according to the frequency of each of the two modes. To verify the feasibility of the proposed design methodology, a 20°-bit phase shifter was designed through a 65 nm RFCMOS process. As a result of the measurement at 21.5 GHz to 40.0 GHz, the phase error was within 0.87°.

Keywords: CMOS; phase error; phase shifter; wideband

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1. Introduction

With the introduction of 5G mobile communication, research related to beamforming systems has recently been actively conducted [1–4]. Accordingly, millimeter-wave (mm-Wave) circuits constituting the beamforming system are also developing. Recently, research has been active in securing more frequency bands with one beamforming system by securing wideband characteristics as well as improving the performance of mm-Wave circuits that make up the beamforming system [5–10].

With the development of such a beamforming system, research on a phase shifter for antenna beam control is also attracting attention [11–13]. Such a phase shifter is divided into an active type using a vector sum and a passive type using a filter consisting of a passive device and switch. Active phase shifters have the advantage of fine-tuning the phase and amplifying the signal, while only one-way signal paths are possible [14–21]. On the other hand, in the case of a passive phase shifter, there is a disadvantage that insertion loss occurs due to power loss caused by passive devices, but there is an advantage that a bidirectional signal path is possible [22–25]. The passive phase shifter consists of several bits that can control the phase, and each bit has a different amount of phase control function. The advantages and disadvantages of each phase shift structure have been summarized in previous studies [26]. These phase shifters, like other mm-Wave circuits [5,9], require wideband characteristics to be secured for the application of beamforming systems that can support multiple frequency bands [11,25].

In this study, a method of designing a unit bit of a phase shifter that can secure wideband characteristics in a passive phase shifter consisting of several bits and suppress phase error at the same time was proposed. The proposed design methodology relates to the L-C-L T-type structure, and a method of maintaining phase differences in a wide range of frequency bands through impedance analysis in pass and shift modes was proposed. The

proposed design methodology was applied to the phase shifter fabricated with the 65 nm RFCMOS process, and its feasibility was confirmed through the measurement results.

2. Proposed Design Method of the Wideband L-C-L T-Type Unit Bit for Phase Shifters

Here, in order to explain the proposed design methodology of a wideband phase shifter with a suppressed phase error, the equivalent circuits in shift and pass mode were first analyzed. After considering the simplified equivalent circuit for each mode, a design technique for a wideband phase shifter with suppressed phase errors was presented using the derived equivalent circuits.

2.1. Analysis of Equivalent Circuits by Mode in T-Type Structure

Figure 1 shows the schematic and its equivalent circuits of the unit bit of a wideband phase shifter for the application of the proposed design methodology. The unit bit of the phase shifter operates in shift and pass modes, respectively, depending on the on- and off-states of the transistor acting as a switch. Figure 1b,c show equivalent circuits in shift and pass modes of the unit bit, respectively.

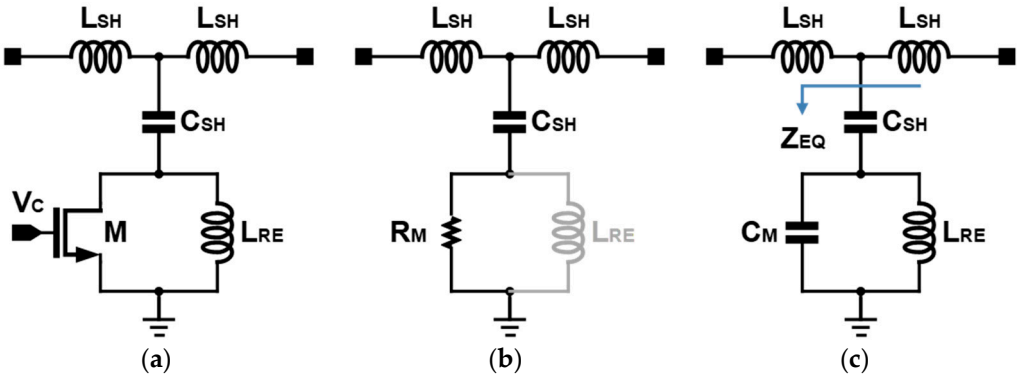

Figure 1. L-C-L T-type structure of unit bit for phase shifter: (**a**) schematic of the used T-type structure, and equivalent circuits for the (**b**) shift and (**c**) pass modes.

In the shift mode shown in Figure 1b, the transistor M is turned on, and for convenience of analysis, it is assumed equivalent to the on-resistance, R_M of the transistor. Assuming that the impedance of R_M is small enough, the impedance by L_{RE} connected in parallel with R_M can be ignored. In this case, the equivalent circuit of the shift mode is in the form of a low-pass filter composed of a T-type L_{SH}-C_{SH}-L_{SH}.

On the other hand, in the case of the pass mode, M is turned off, and for the convenience of analysis, it is assumed equivalent to C_M due to parasitic capacitances of the transistor M, as shown in Figure 1c. In this case, unlike the shift mode, direct equalization with the L-C-L structure is difficult. Therefore, the Z_{EQ} of Figure 1c was developed as follows.

$$Z_{EQ} = \frac{1 - \omega^2 L_{RE}(C_{SH} + C_M)}{j\omega C_{SH}(1 - \omega^2 L_{RE} C_M)} \tag{1}$$

Here, for convenience of analysis, it was assumed that the parasitic resistance was small enough to be negligible. The frequencies at which Z_{EQ} becomes 0 and infinite using Equation (1) are calculated as follows.

$$\begin{aligned} \omega_{Z_{EQ}=0} &= \frac{1}{\sqrt{L_{RE}(C_{SH}+C_M)}}, \\ \omega_{Z_{EQ}=\infty} &= \frac{1}{\sqrt{L_{RE}C_M}} \end{aligned} \tag{2}$$

Here, $\omega_{Z_{EQ}=0}$ and $\omega_{Z_{EQ}=\infty}$ denote frequencies at which Z_{EQ} becomes 0 and infinity, respectively. Figure 2 shows the simulation results of the resistance and capacitance of Z_{EQ} according to frequency. Since the simulation was performed using models of actual devices,

there is a slight difference from the results of the analyzed equations, but the tendency is the same as that of the equations. The main difference between equations and simulation is that parasitic resistances were ignored in equations, but were considered in simulation.

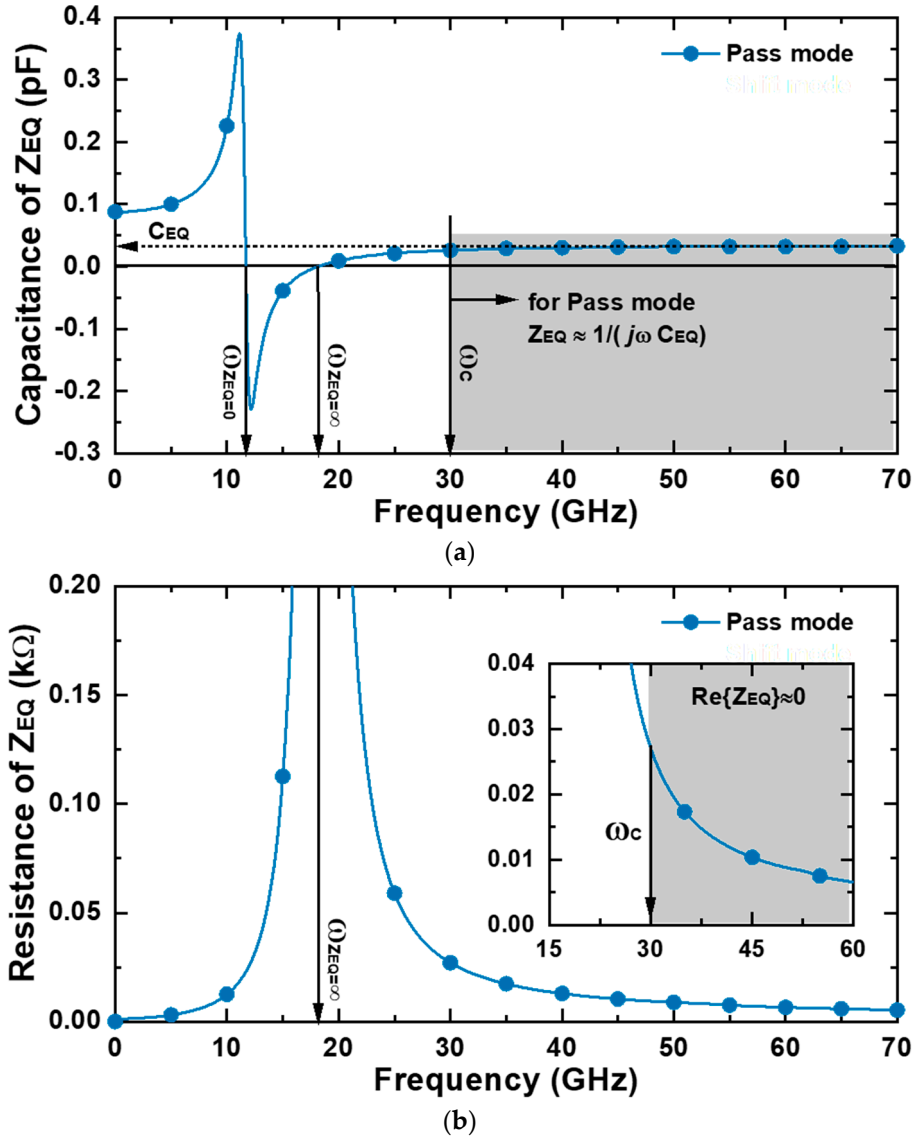

Figure 2. Simulated conceptual Z_{EQ} according to operating frequency: (**a**) capacitance and (**b**) resistance.

The capacitance of Z_{EQ} shown in Figure 2a has a value of 0 at $\omega_{Z_{EQ}=0}$ and $\omega_{Z_{EQ}=\infty}$. As the operating frequency gradually increases from $\omega_{Z_{EQ}=0}$, the capacitance of Z_{EQ} converges to a specific value, and the converging capacitance is expressed as C_{EQ}. At this time, the frequency at which the capacitance of Z_{EQ} begins to be regarded as C_{EQ} was defined as ω_C. On the other hand, the resistance shown in Figure 2b has the highest value at $\omega_{Z_{EQ}=\infty}$, which is determined by the L_{RE} and C_M as shown in Equation (2). As the operating frequency increases from $\omega_{Z_{EQ}=\infty}$, the resistance gradually decreases, and eventually approaches 0 Ω. In addition, even near ω_C set from Figure 2a, the resistance of Z_{EQ} can be considered 0 Ω. As a result, in the frequency region higher than ω_C, the resistance and capacitance of Z_{EQ} are 0 Ω and C_{EQ}, respectively, so Z_{EQ} can be expressed as follows.

$$Z_{EQ} \cong \frac{1}{j\omega C_{EQ}} \quad for \quad \omega > \omega_C \tag{3}$$

Therefore, in the case of pass-mode, a circuit consisting of C_{SH}, C_M, and L_{RE} may be represented by C_{EQ} in the frequency region higher than ω_C. This allows an equivalent circuit in pass mode to be T-type L_{SH}-C_{EQ}-L_{SH}, similar to shift mode, in frequency regions higher than ω_C. Figure 3 shows equivalent circuits of shift and pass modes in frequency regions higher than ω_C.

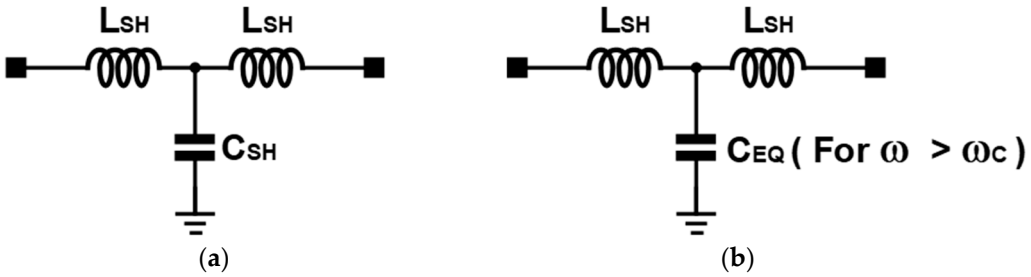

Figure 3. Equivalent circuits in frequency regions above ω_C: (**a**) shift and (**b**) pass modes.

2.2. Proposed Design Methodology for Wideband Phase Shifter with Suppressed Phase Error

Figure 4 is a conceptual diagram for explaining the proposed design methodology of a wideband phase shifter with suppressed phase errors using the previously derived equivalent circuit for each mode. In the case of an equivalent circuit in shift mode, it has a structure of L_{SH}-C_{SH}-L_{SH} regardless of the operating frequency, so the phase in shift mode in Figure 4 shows linear characteristics according to the frequency. On the other hand, in the case of an equivalent circuit in pass mode, it can only be regarded as the structure of L_{SH}-C_{EQ}-L_{SH} in the higher operating frequency region than ω_C, so the phase in pass mode in Figure 4 shows linear characteristics according to the frequency after ω_C.

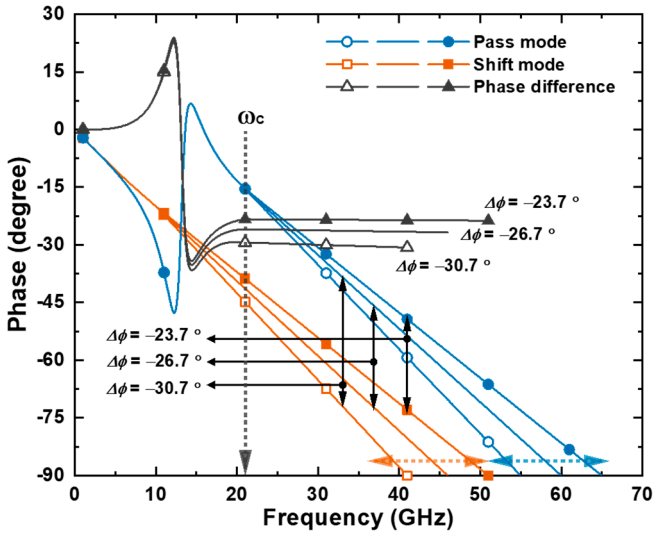

Figure 4. Conceptual diagram for securing wideband characteristics with suppressed phase error.

That is, in the frequency regions after ω_C, for both shift and pass modes, the phase according to the frequency maintains a linear characteristic. Therefore, in the frequency region after ω_C, if the slopes of the phases according to the frequency in the shift and pass modes are set to be the same, the phase difference between shift and pass modes can be maintained to be the same in the frequency region after ω_C. When the slopes of the shift and pass modes are set the same as each other, the phase difference between the two modes also increases as the absolute value of the slope in the two modes increases.

As a result of qualitative analysis, wideband characteristics can be secured by equalizing the phase slopes according to the frequency of the two modes. In addition, the desired phase difference can be secured by adjusting the equalized slope.

In order to quantify such a qualitative analysis, the phase of each mode in the frequency region after ω_C can be calculated as follows.

$$\varphi_{Shift} = \tan^{-1}\left(-\frac{2\omega L_{SH} - \omega^3 L_{SH}^2 C_{SH}}{Z_0(1-\omega^2 L_{SH} C_{SH})}\right) \quad (4)$$

$$\varphi_{Pass} = \tan^{-1}\left(-\frac{2\omega L_{SH} - \omega^3 L_{SH}^2 C_{EQ}}{Z_0(1-\omega^2 L_{SH} C_{EQ})}\right) \quad (5)$$

where φ_{Shift} and φ_{Pass} are phases of the shift and pass modes, respectively. In addition, we assumed that the termination impedance Z_0 is 50 Ω. Here, for convenience of analysis through equations, it was assumed that parasitic resistances including R_M were small enough to be negligible. In this study, instead of directly setting the phase slope according to the frequency, the desired slope for each mode was secured by adjusting the frequency at which the phase in each mode becomes $-90°$. In order to set the slope of the phase in this manner, the frequency at which the phase becomes $-90°$ for each mode is considered as follows.

$$\begin{aligned} \omega_{Shift-90} &= \frac{1}{\sqrt{L_{SH}C_{SH}}} \\ \omega_{Pass-90} &= \frac{1}{\sqrt{L_{SH}C_{EQ}}} \end{aligned} \quad (6)$$

where $\omega_{Shift-90}$ and $\omega_{Pass-90}$ are frequencies when the phase becomes $-90°$ in shift and pass modes, respectively.

As a result of quantitative analysis of the proposed design methodology, if the frequency with a phase of $-90°$ in each mode is adjusted through Equation (6), a wideband phase shifter with a suppressed phase error can be secured.

3. Design Examples of the Phase Shifter Using Proposed Design Methodology

In this study, in order to verify the effectiveness of the proposed design methodology, several unit bits of the phase shifter were first designed through simulation.

Here, if Equation (6) and Figure 4 are analyzed again, in the case of the unit bit of the L-C-L structure of a wideband phase shifter with a large phase difference, the absolute value of the phase slope according to frequency must increase. This means that $\omega_{Shift-90}$ and $\omega_{Pass-90}$ of Equation (6) should decrease, and $L_{SH}C_{SH}$ and $L_{SH}C_{EQ}$ should increase. As such, when the required inductance and capacitance increase for a large phase difference, the power loss and the size of the integrated circuit also increase accordingly. Therefore, the wideband unit bit with suppressed phase error using the T-type L-C-L structure proposed in this study is relatively more suitable for securing a small phase difference. For this reason, in this study, as shown in Figure 5, unit bits for phase shifters of 5°, 10°, 15°, and 20° were designed to verify the proposed structure through simulation.

In this study, the 65 nm RFCMOS process which provides eight metal layers was used to design the phase shifter. The schematics for the simulation results of Figure 5 are all the same as Figure 1a. The device values used for each bit to obtain the phase shift of 5°, 10°, 15°, and 20° shown in Figure 5 are summarized in Table 1. When designing for each bit to obtain simulation results, the effects of metal lines, inductors, and test pads were all considered through electromagnetic (EM) simulation to secure the accuracy of the simulation results. Spiral inductors are designed using the top metal layer to minimize loss due to the Silicon substrate. In addition, the gate voltages of the transistor were 1 V and 0 V, respectively, for the on and off states of the transistor. The simulation results in Figure 5 were conducted at a temperature of 25 °C in a typical corner.

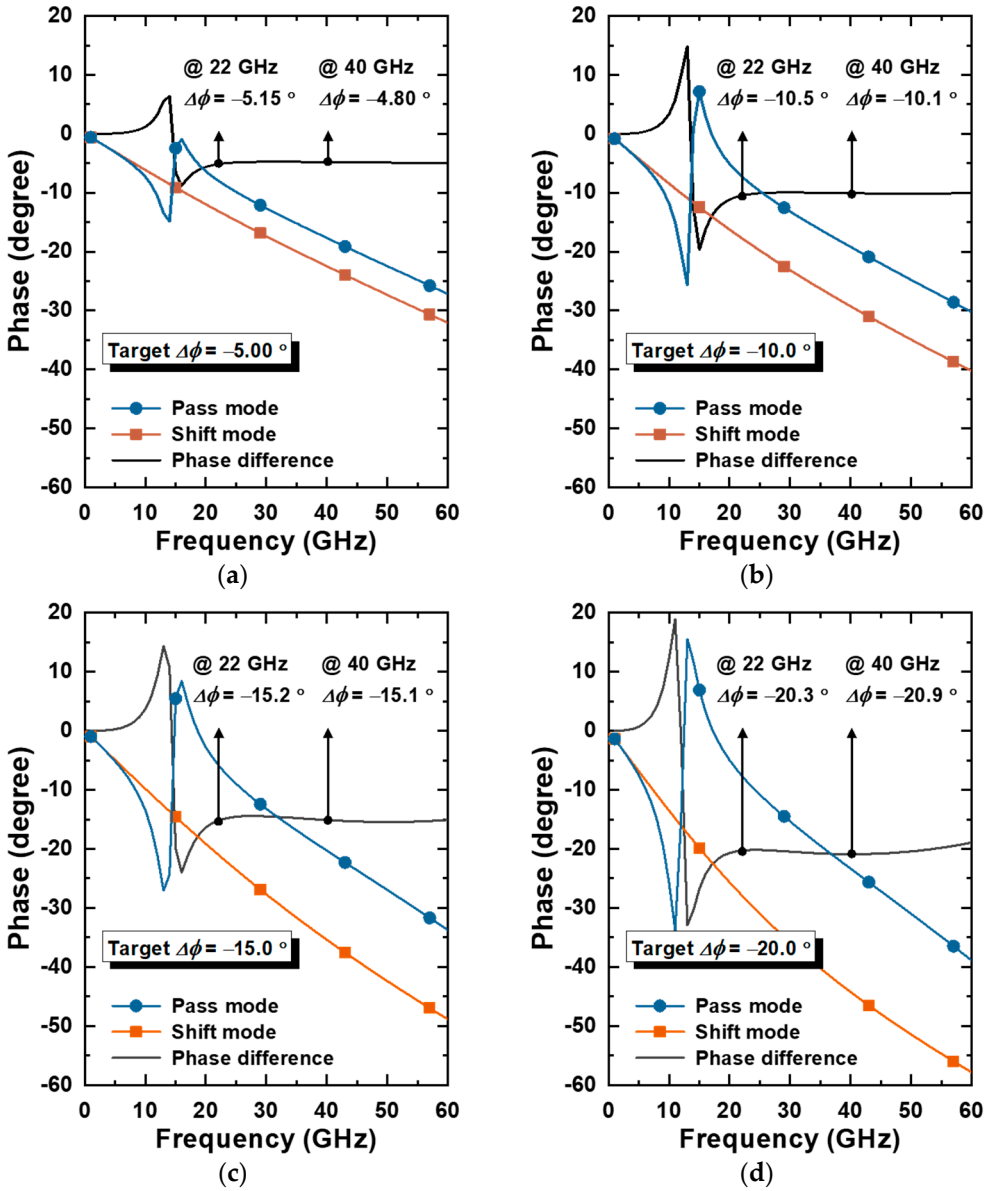

Figure 5. Simulation results of design examples of the wideband phase shifter: (**a**) 5°, (**b**) 10°, (**c**) 15°, and (**d**) 20°.

Table 1. Size of the used transistors, inductors, and capacitors.

Bits	5°	10°	15°	20°
M (μm) [1]	4.8	6.8	10.5	12.0
C_M (fF)	5.0	7.4	10.5	12.4
C_{SH} (fF)	29.1	47.6	80.5	106.2
L_{SH} (pH)	220	220	220	220
L_{RE} (nH)	1.73	1.44	1.44	1.13

[1] Total gate width.

Among the simulation results of the four designed phase shifters, the phase shifter of 20° was actually fabricated, measured, and analyzed. Accordingly, the phase shifter of 20° was investigated in more detail. As shown in Figure 5d, the simulation results of the phase difference of −20.9° were obtained at the 25 °C typical corner with the operating frequency of 40 GHz. In addition, simulation results at −40 °C, 25 °C, and 80 °C were examined in fast, typical, and slow corners to confirm the impact of process and temperature variations.

For the 20° phase shifter with the operating frequency of 40 GHz, simulation results of the phase difference of −19.2° and −22.3° were obtained in the −40 °C fast corner and 80 °C slow corner, respectively. It was confirmed as a simulation result that there was a deviation of approximately 3.1° by process and temperature variations with the operating frequency of 40 GHz.

As described above, in order to ensure wideband characteristics with suppressed phase errors, the slopes of the phase according to the frequency of shift and pass modes for each bit were designed to be the same. For all 5°-, 10°-, 15°-, and 20°-bits, the phase error from the operating frequency of 22 GHz to 40 GHz was within 0.6° under 25 °C typical corner conditions. If the operating frequency was expanded from 22 GHz to 60 GHz, the phase error was less than 0.97°. Such a frequency range includes all of the frequency ranges for 5G applications in the mm-Wave band. As a result, from the simulation results shown in Figure 5, it can be seen that the proposed design methodology is effective in securing wideband characteristics and suppressing phase errors in the phase shifter.

4. Measurement Results of the Designed Wideband Phase Shifter

In order to verify the effectiveness of the proposed design methodology through measurement, a phase shifter of the unit bit of the T-type L-C-L structure was designed using the 65-nm RFCMOS process. The phase shift target of the designed unit bit was set to 20°. For shift- and pass-modes, the gate voltages of the transistor were 1 V and 0 V, respectively. The measurement was carried out at room temperature. Figure 6 shows a chip photograph of the designed 20°-bit phase shifter. The chip and core sizes are 0.290×0.455 mm^2 and 0.130×0.260 mm^2. The designed phase shifter of the unit bit is actually integrated and used in the transceiver for the beamforming system. Therefore, although test pads were implemented in this study to verify the feasibility of the phase shifter itself, these test pads are removed when applied to the actual transceiver. On-wafer probes were used to measure RF input and output signals, and gate voltage was applied through a bonding wire.

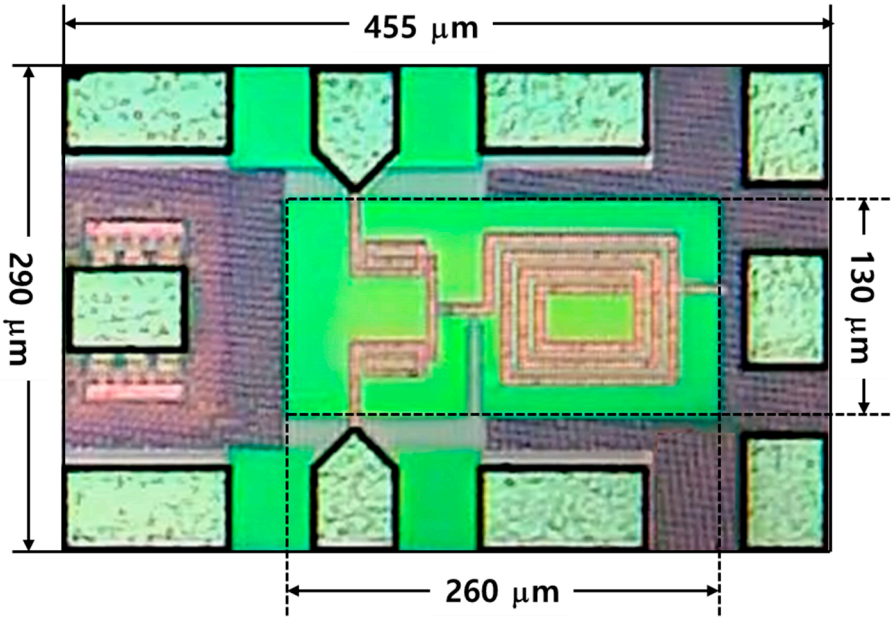

Figure 6. Chip photograph of the designed unit bit phase shifter.

Figure 5d shows the simulated phase characteristics according to the frequency of the designed unit bit phase shifter, and Figure 7 shows the measured phase characteristics. Due to the limitation of the measurement environment, the operating frequency of the designed unit bit phase shifter was measured up to 40 GHz. The target phase was 20°, but the measured phase was slightly reduced. One of the causes of the difference between

measurement and simulation results may be the accuracy of EM simulation. In addition, as described in the previous section, process–voltage–temperature (PVT) variation can also be one of the important causes of the difference.

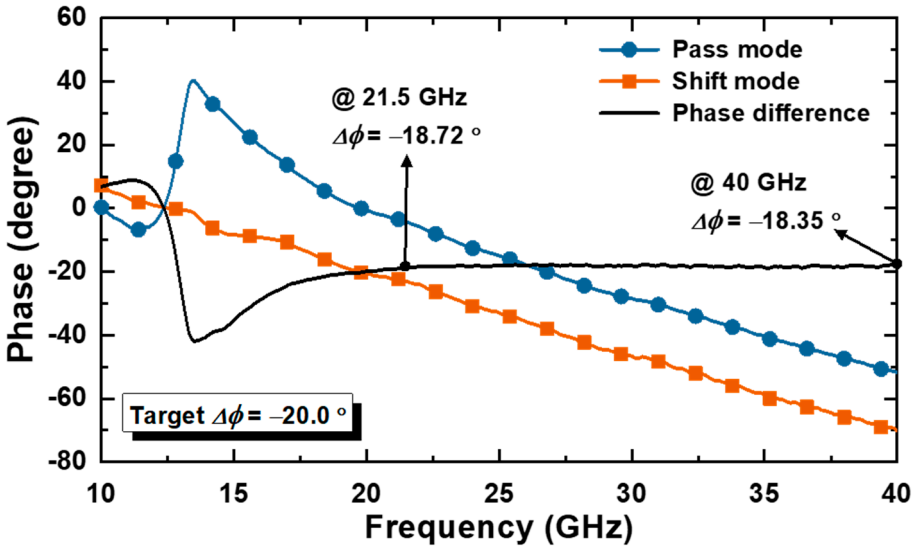

Figure 7. Measured phases for shift and pass modes and phase difference.

The measured phase differences of the shift and pass modes were 18.72° and 18.35° at 21.5 GHz and 40.0 GHz, respectively. In the operating frequency range of 21.5 GHz to 40.0 GHz, the measured phase difference was in the range of 17.85° to 18.72°. Therefore, based on the target phase difference of 20°, the phase error was less than 2.15°. However, considering the wideband characteristics of the proposed designed technique, the deviation of the phase difference in the operating frequency range from 21.5 GHz to 40.0 GHz was less than ±0.5°. Figure 8 shows the measured and simulated insertion losses of the designed unit bit phase shifter.

In Table 2, the performance of CMOS-based wideband phase shifters was compared. While phase shifters in most previous studies consist of several bits, the phase shift in this study consists of a unit bit. Therefore, accurate comparative evaluation is somewhat difficult. However, it can be seen that the phase shifter of this study generally has a low phase error in a wide frequency range.

Table 2. Performance comparison of CMOS phase shifters.

Ref.	Tech. (nm)	Type /Bits	Freq. (GHz)	BW (%)	IL [1] (dB)	RMS Phase Error (°)	P_{DC} (mW)	Core Size (mm^2)
[27]	28	VSPS/2.8° [2]	22–44	66.7	<5.81	<2.6	25	0.19
[28]	180	VSPS/22.5° [2]	27–33	20.0	<10.0	<4.0	6.6	0.44
[29]	65	RTPS/>360° [3]	27.8–31.2	11.5	<9.0	-	0	0.08
[30]	65	RTPS/>180° [3]	25–43	53.0	<9.1	-	0	0.15
[31]	65	STPS/5-bits	27–42	43.5	<14.5	<3.8 [4]	0	0.40
[32]	28	STPS/4-bits	29–37	24.2	<15.3	<8.8	0	0.07
This work	65	STPS/1-bits	21.5–40.0	63	<5.0	<0.5	0	0.03

[1] Insertion loss, [2] resolution, [3] phase-shift range, [4] controlled by bi-phase modulator.

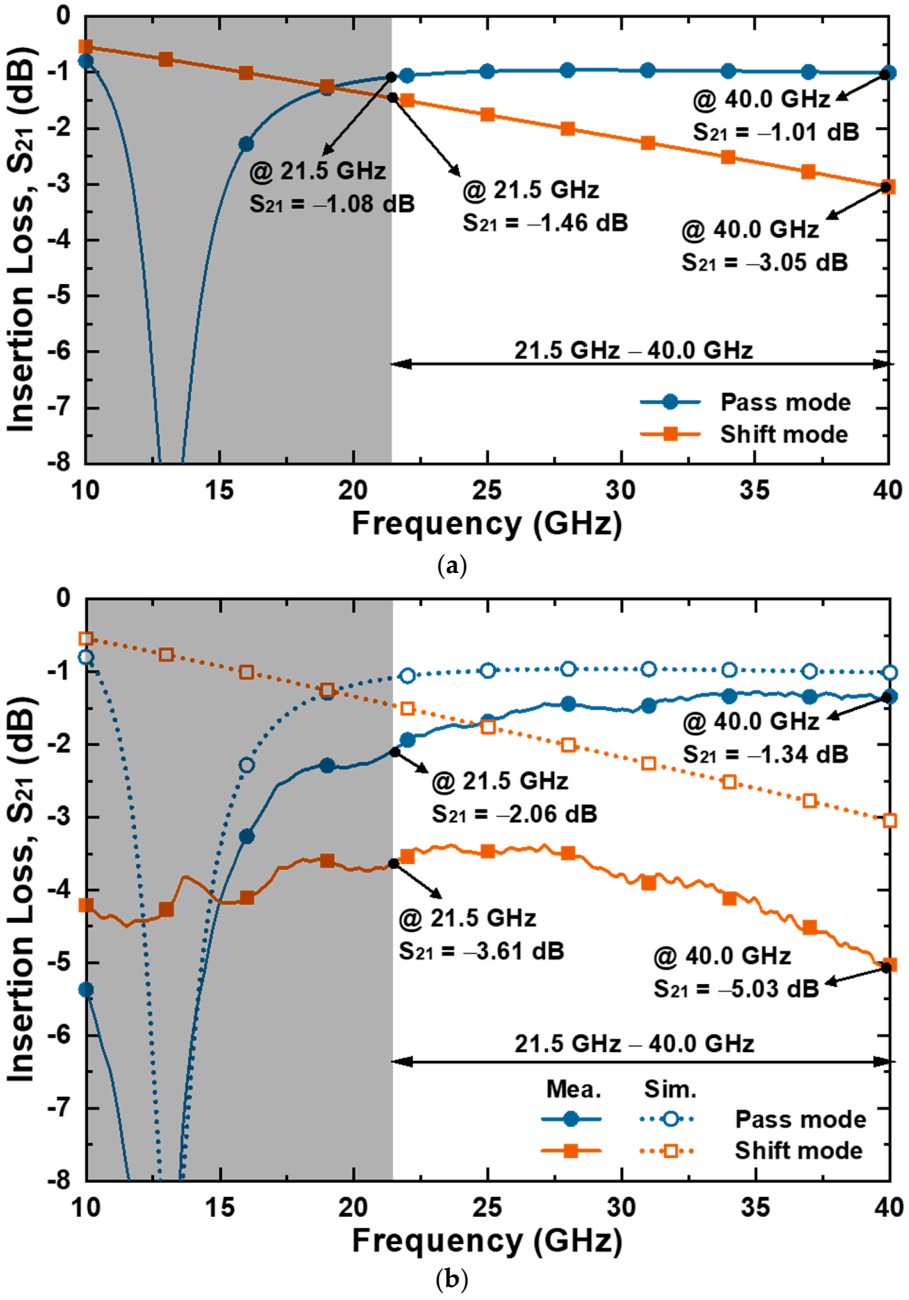

Figure 8. Insertion loss: (**a**) simulation and (**b**) measurement results.

5. Conclusions

In this study, we propose a design methodology for a wideband phase shifter with suppressed phase errors. To this end, the equivalent circuits in shift and pass modes of the phase shifter were analyzed. Through internal impedance analysis of equivalent circuits, it was shown using mathematical and simulation results that both modes can be represented by equivalent circuits of the L-C-L structure beyond a specific frequency. In shift and pass modes represented by equivalent circuits of L-C-L structure, it was confirmed that phase errors can be minimized in a wide range of frequency bands when the slope of the phase according to frequency is adjusted. Adjustment of the slope can be achieved by adjusting the frequency of -90° in each mode, which can be achieved by adjusting the inductance and capacitance in the equivalent circuit for each mode. The proposed design methodology was applied to a 20°-bit phase shifter designed with a 65 nm RFCMOS process. As a result of the measurement, at 21.5 GHz to 40.0 GHz, the phase error was within 0.87°.

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