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Article

A 10 GHz Compact Balun with Common Inductor on CMOS Process

Chatrpol Pakasiri [1], Jian-Long Xu [2] and Sen Wang [2,*]

[1] College of Advanced Manufacturing Innovation, King Mongkut's Institute of Technology Ladkrabang, Bangkok 10520, Thailand
[2] Department of Electronic Engineering, National Taipei University of Technology, Taipei 10608, Taiwan
* Correspondence: wangsen@mail.ntut.edu.tw

Abstract: This paper presents a compact balun with a common inductor design. The design used Wilkinson-type balun topology with modified lumped transmission lines and a common inductor to realize circuit size reduction on a lossy CMOS process. Measurements of the prototype chip had a reflection coefficient below 17.8 dB at all ports, an insertion loss of 1.98 dB, and an isolation of 16.8 dB. The chip size was only $0.025\lambda_0 \times 0.034\lambda_0$.

Keywords: Wilkinson-type balun; lumped transmission line; common inductor; CMOS

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1. Introduction

Baluns have been used widely in many microwave and millimeter-wave applications such as antenna feed networks, balanced mixers, push–pull power amplifiers, and frequency doublers. For power requirement categorization, baluns can be divided into passive and active. Active baluns are usually unidirectional signal couplers. Their advantages are circuit gain and less chip area [1–3]. Nevertheless, the cons of them are noise figures and power consumption. Many techniques were used to improve active balun performances [4–6]. Passive baluns are, in general, more linear, without power consumption. One of the main disadvantages of passive baluns compared to active ones is their larger size. Some types of passive baluns are Marchand baluns, lumped component baluns, transformer-type baluns, and Wilkinson-type baluns. They are designed to work in broadband and narrowband applications [7–19]. Marchand baluns use coupled transmission lines in the design, which typically result in wideband operation and large chip area [7–9].

Lumped component baluns are designed on printed circuit boards [10–12] and on chips [13–15]. Because of the narrowband properties of lumped circuits, lumped component baluns are more suitable for narrowband applications. Another type of balun is the transformer-type balun [16–18]. Transformer-type balun sizes are generally small since the circuit has few components. However, they might suffer from relatively high return losses at all ports.

The other type of balun is based on the Wilkinson power divider structure [19]. In that work, the circuit was implemented on a printed circuit board. One of the transmission lines that led to the output ports was a left-handed transmission line, while the other was distributed transmission line. Two resistors and a transmission line replaced the resistor between the output in the Wilkinson power divider circuit. The output ports yield the same signal strength with opposite phases.

In this work, a Wilkinson-type balun with a common inductor was designed and fabricated on a 0.18 µm CMOS process. The designed circuit used lumped components to yield a compact chip area, $0.025\lambda_0 \times 0.034\lambda_0$, at a 10 GHz operating frequency. The new design improved the circuit size by modifying two circuit parts. Firstly, modified lumped transmission lines in the design reduced the chip area. Since the silicon substrate was lossy, a single-section lumped transmission line circuit with an electrical length longer

than 60 degrees could not perform as a distributed transmission line at the operating frequency [20]. Cascaded lumped transmission lines could replace the required ones, leading to a larger circuit. With single-section modified transmission lines in the design, the phase difference at the output ports could maintain a differential form. Secondly, larger lumped transmission line circuits could be avoided by instead using a common inductor in the design.

This paper is organized as follows. Section 2 introduces a Wilkinson-type balun. Section 3 describes a balun with lumped transmission lines and a common inductor. Section 4 shows simulated and measured results of 10 GHz balun. Finally, Section 5 concludes this paper.

2. Conventional Wilkinson-Type Balun

Conventional Wilkinson-type baluns used transmission lines with opposite phases with distributed lines and a resistor placed between the output ports, as shown in Figure 1. The additional circuit branch between the output ports can be configurated in other forms as well [1,2]. Nevertheless, the distributed transmission lines in series branches must have the same characteristic impedance with an opposite phase. The even- and odd-mode circuits of the conventional Wilkinson-type balun are shown in Figures 2 and 3.

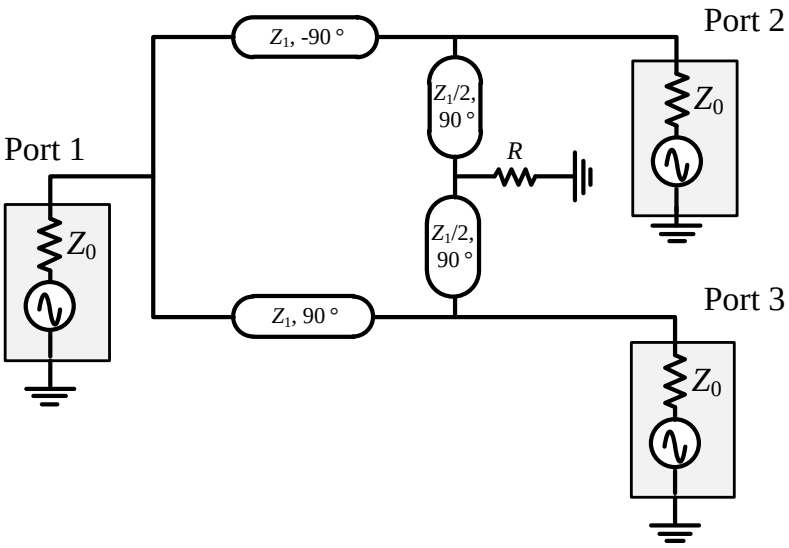
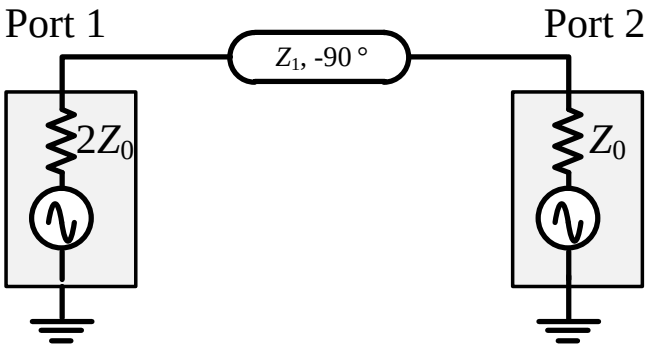


Figure 1. Schematic of the conventional Wilkinson−type balun.



(**a**)

Figure 2. *Cont.*

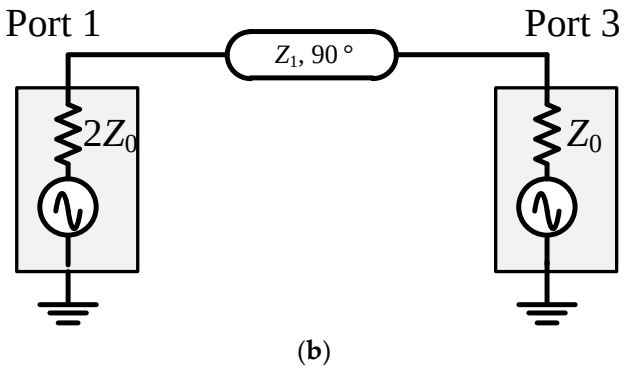


Figure 2. Schematic of the even−mode circuits between (**a**) Port 1 and Port 2 and (**b**) Port 1 and Port 3.

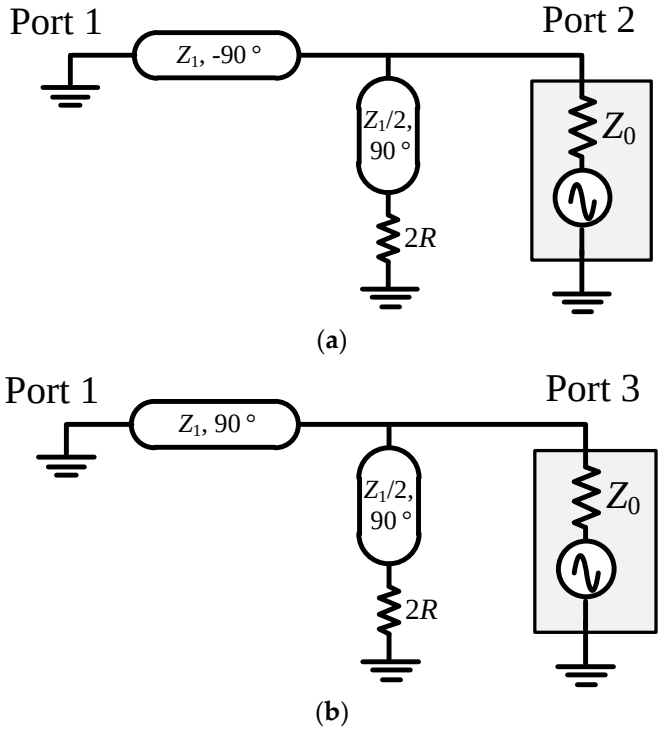


Figure 3. Schematic of the odd−mode circuits between (**a**) Port 1 and Port 2 and (**b**) Port 1 and Port 3.

For the even-mode circuits in Figure 2, the matching condition at both ports yield

$$Z_1 = \sqrt{2}Z_o \tag{1}$$

where Z_1 is the characteristic impedance of the transmission lines and Z_0 is the port impedance. For the odd-mode circuits in Figure 3, the matching condition at both ports yield

$$R = \frac{Z_o}{4} \tag{2}$$

In CMOS implementation, the distributed transmission lines were replaced by lumped-transmission lines, e.g., right-handed or left-handed transmission lines [21]. The positive-phase transmission lines were replaced by right-handed transmission lines (RHTL), while the negative-phase transmission lines were replaced by left-handed transmission lines (LHTL). The lumped transmission line topologies use inductors and capacitors, as shown in Figure 4.

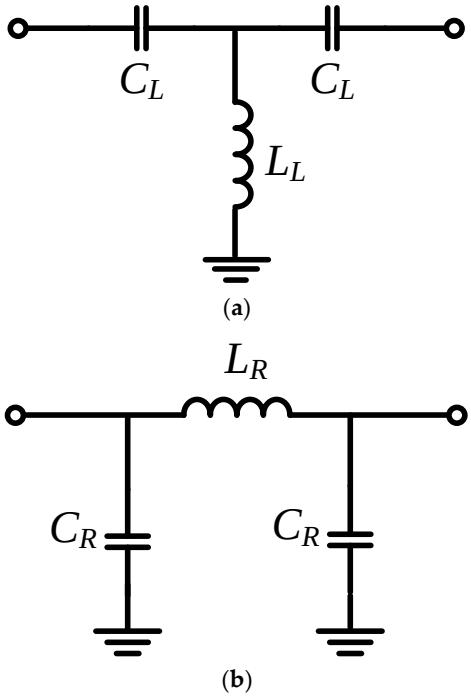


Figure 4. Schematic of (**a**) left-handed and (**b**) right-handed transmission lines.

The inductor and capacitor values of the lumped transmission lines are related, as shown below.

$$L_L = \frac{-Z_o}{\omega \sin\theta} \tag{3a}$$

$$C_L = \frac{-\sin\theta}{\omega Z_o(1-\cos\theta)} \tag{3b}$$

$$L_R = \frac{Z_o}{\omega}\sqrt{1-\cos^2\theta} \tag{3c}$$

$$C_R = \frac{1}{\omega Z_o}\sqrt{\frac{1-\cos\theta}{1+\cos\theta}} \tag{3d}$$

where θ is the electrical length of the transmission line and ω is the angular frequency. Using the left- and right-handed transmission lines, the lumped transmission line balun circuit is shown in Figure 5.

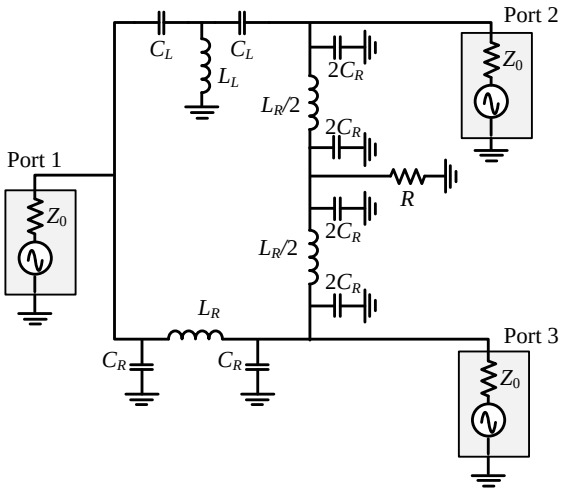


Figure 5. Schematic of conventional lumped transmission line balun.

3. Balun with a Common Inductor

Figure 6 shows the proposed balun with a common inductor. The lumped transmission line balun was modified by replacing the transmission lines between the output Port 2 and Port 3 with a common inductor, a capacitor, and a resistor. Additional shunt capacitors were also added to the end of both left- and right-handed transmission lines. The capacitors of the left- and right-handed transmission lines were also modified to account for phase balance due to the resistive losses of the transmission lines. The effects of inductor losses will be discussed later.

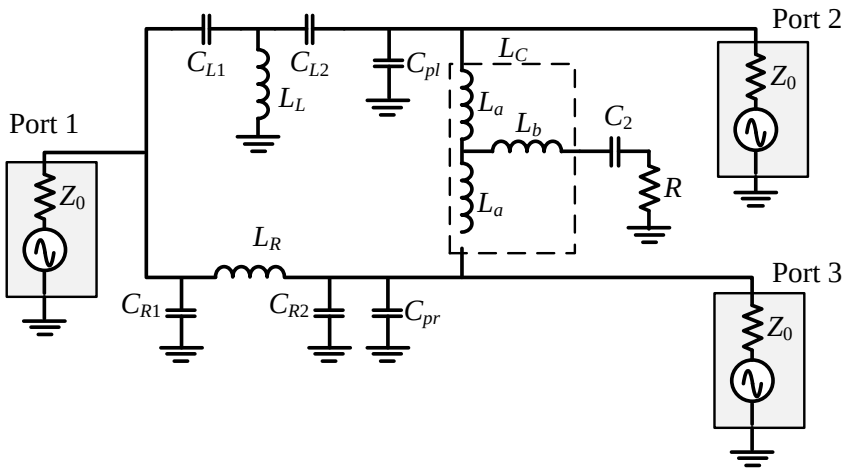


Figure 6. Schematic of the balun with a common inductor.

3.1. Phase Balance of Transmission Lines with Inductor Losses

In the CMOS process, the inductor losses were the main source of resistive losses of the circuit. The ideal lumped transmission line circuits, as shown in Figure 4, with the resistive losses in the inductor are discussed next. For a normal lumped transmission line circuit with $\pm 90^\circ$ electrical length at 10 GHz, the capacitors C_{L1}, C_{L2}, C_{R1}, and C_{R2} are equal and chosen as 0.225 pF. The inductors L_L and L_R of the transmission lines have the same inductance as 1.125 nH. For an inductor, low resistive loss implies high quality factor values. Figure 7 shows the study of various quality factors (Q) of the inductors versus the transmission coefficient, S_{21}. The phases of S_{21} are shown as the deviation from lossless transmission line ones, Δ_{phase}, as

$$\Delta_{phase} = -90 - phase(S_{21}) \text{ for RHTL} \tag{4a}$$

$$\Delta_{phase} = phase(S_{21}) - 90 \text{ for LHTL} \tag{4b}$$

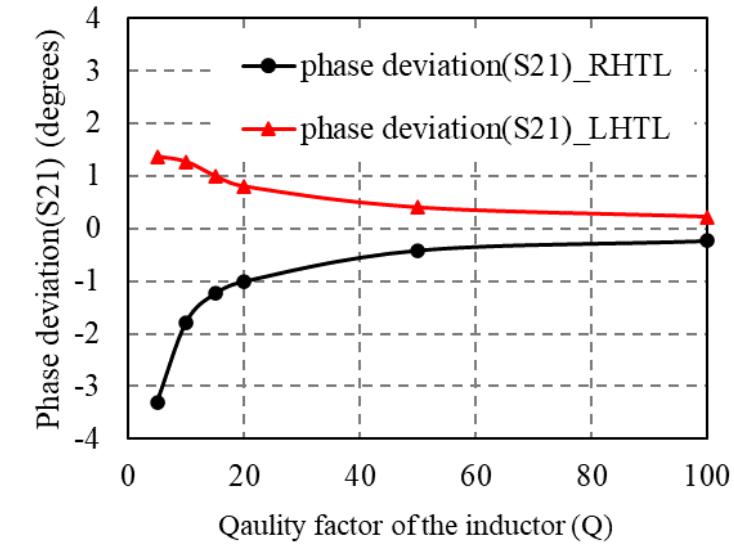
As the quality factor of the inductors lowered, the phase obtained more deviation from those of the lossless transmission lines. The lower Q inductor in the left-handed transmission line tends to increase the phase S_{21}, while that in the right-handed transmission line tends to decrease the phase S_{21}. Therefore, for a lower Q inductor, the differential phase between the transmission lines is less than 180°. For example, with a Q of 5, the right-handed transmission line has a phase S_{21} of -86.7° while the left-handed transmission line has a phase S_{21} of 91.37°. Then, the differential phase is only 178.07°.

3.2. Improvement of Phase Balance

To improve the phase balance of the circuit, the capacitors of the transmission lines are varied as C_{L1}, C_{L2}, C_{R1}, and C_{R2}. The impedances of inductors, L_L and L_R, are defined as

$$Z_{LL} = R_L + j\omega L_L \tag{5a}$$

$$Z_{RR} = R_R + j\omega L_R \tag{5b}$$



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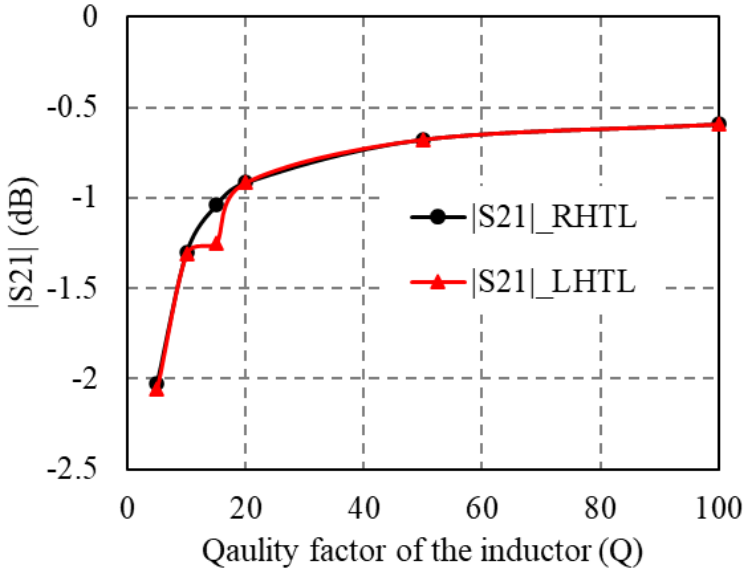

(**b**)

Figure 7. Magnitude and phase deviation of the left- and right-handed transmission lines. (**a**) Phase deviation of $|S_{21}|$ and (**b**) magnitude of $|S_{21}|$.

The impedance of each part (L_a and L_b) in the common inductor, L_C, are defined as

$$Z_a = R_a + j\omega L_a \tag{6a}$$

$$Z_b = R_b + j\omega L_b \tag{6b}$$

The phase S_{21} of the left- ($\theta_{s21,LHTL}$) and right-handed transmission lines ($\theta_{s21,RHTL}$) are shown in (7).

$$\theta_{S21,LHTL} = -\tan^{-1}\left[\frac{\frac{1}{R_L^2+(\omega L_L)^2}\left[-\frac{R_L}{\omega}\left(\frac{1}{C_{L1}}+\frac{1}{C_{L2}}\right)+\frac{L_L}{\omega C_{L1}C_{L2}Z_o}-\omega L_L Z_o\right]-\frac{1}{\omega Z_o}\left(\frac{1}{C_{L1}}+\frac{1}{C_{L2}}\right)}{2+\left(\frac{1}{R_L^2+(\omega L_L)^2}\right)\left[R_L Z_o-\frac{R_L}{\omega^2 C_{L1}C_{L2}Z_o}-L_L\left(\frac{1}{C_{L1}}+\frac{1}{C_{L2}}\right)\right]}\right] \tag{7a}$$

$$\theta_{S21,LHTL} = -\tan^{-1}\left[\frac{\omega R_R(C_{R1}+C_{R2})+\frac{\omega L_R}{Z_o}+\omega Z_o(C_{R1}+C_{R2})-\omega^3 L_R Z_o C_{R1}C_{R2}}{2+\frac{R_R}{Z_o}-[R_R Z_o C_{R1}C_{R2}+L_R(C_{R1}+C_{R2})]\omega^2}\right] \tag{7b}$$

To impose the amplitude balance and phase balance of both transmission lines, the design equation becomes

$$|S_{21,LHTL}| = |S_{21,RHTL}| \tag{8a}$$

$$|\theta_{21,RHTL} - \theta_{21,LHTL}| = \pi \tag{8b}$$

where $S_{21,LHTL}$ and $S_{21,\ RHTL}$ are shown in (9).

$$S_{21,LHTL} = \frac{2}{2 + \left(\frac{1}{R_L + j\omega L_L}\right)\left[\frac{1}{j\omega}\left(\frac{1}{C_{L1}} + \frac{1}{C_{L2}}\right) - \frac{1}{\omega^2 C_{L1} C_{L2} Z_o} + Z_o\right] + \frac{1}{j\omega Z_o}\left(\frac{1}{C_{L1}} + \frac{1}{C_{L2}}\right)} \tag{9a}$$

$$S_{21,RHTL} = \frac{2}{2 + (R_R + j\omega L_R)\left[j\omega(C_{R1} + C_{R2}) + \frac{1}{Z_o} - Z_o\omega^2 C_{R1} C_{R2}\right] + j\omega Z_o(C_{R1} + C_{R2})} \tag{9b}$$

With some choices of the capacitor selection in Table 1, the phase balance can be improved with some deteriorated S_{21} magnitudes.

Table 1. Various balun designs for different *Q* values.

Q	C_{R1} (pF)	C_{R2} (pF)	C_{L1} (pF)	C_{L2} (pF)	$\lvert S_{21,LHTL} \rvert$ and $\lvert S_{21,\ RHTL} \rvert$ (dB)
5	0.16	0.33	0.18	0.33	−2.46
10	0.29	0.17	0.19	0.29	−1.49
20	0.19	0.28	0.29	0.17	−1.10
50	0.18	0.28	0.20	0.27	−0.82
100	0.17	0.28	0.19	0.27	−0.75

3.3. Even-Mode Analysis of Balun with Common Inductor

To analyze the balun circuit, an even/odd mode signal was excited to the balun. Then, the circuit could be analyzed separately with even- and odd-mode circuits, as shown in Figures 8 and 9.

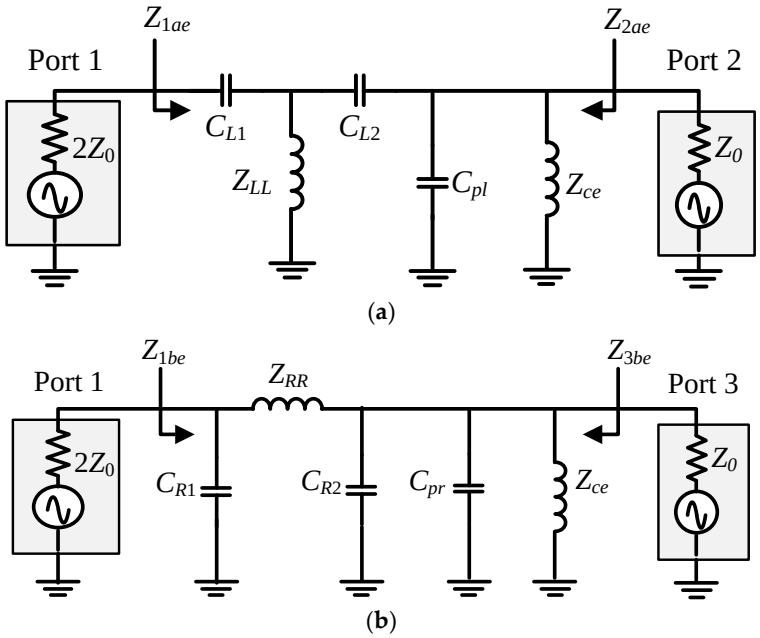

Figure 8. The even-mode circuits of balun with the common inductor between (**a**) Port 1 and Port 2 and (**b**) Port 1 and Port 3.

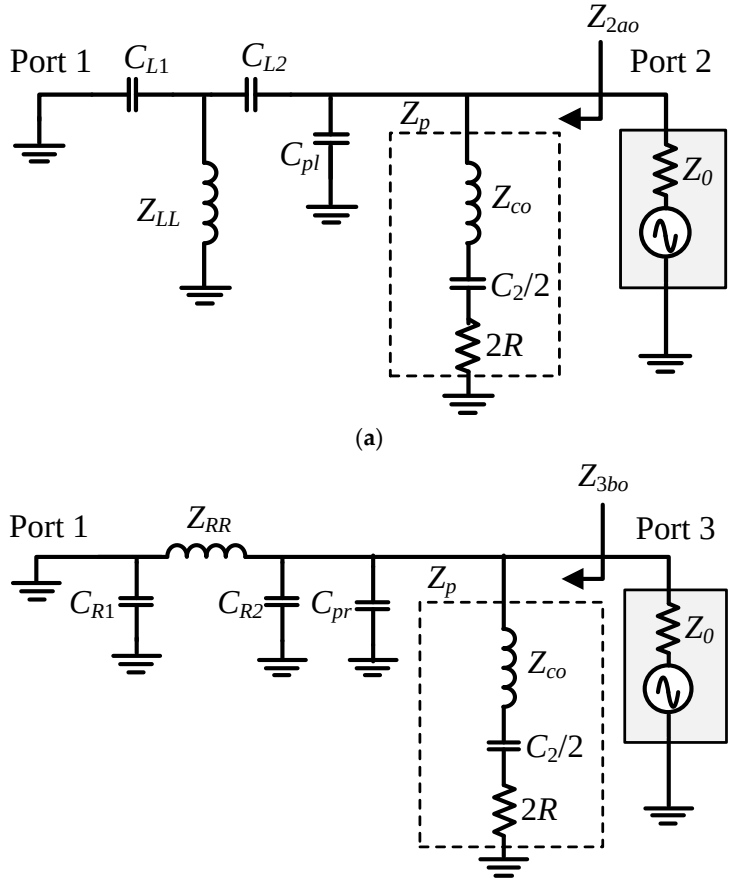

Figure 9. The odd-mode circuits of balun with common inductor between (**a**) Port 1 and Port 2 and (**b**) Port 1 and Port 3.

Equations (10)–(12) show the input impedance at each port, which is needed to match the port impedances. All capacitors are assumed to be lossless, while all inductors have inductive loss as their impedances are shown in (5) and (6).

$$Z_{1ae} = \frac{1}{j\omega C_{L1}} + \frac{(R_L + j\omega L_L)\{(R_a + j\omega L_a)[1 + j\omega Z_0(C_{p1} + C_{L2})] + Z_0\}}{[1 + j\omega C_{L2}(R_L + j\omega L_L)][(R_a + j\omega L_a)(1 + j\omega Z_0 C_{p1}) + Z_0] + j\omega Z_0 C_{L2}(R_a + j\omega L_a)} \tag{10a}$$

$$Z_{2ae} = \frac{(R_a + j\omega L_a)\left[\left(2Z_0 + \frac{1}{j\omega C_{L1}}\right)\left(R_L + j\left(\omega L_L - \frac{1}{\omega C_{L2}}\right)\right) + \left(\frac{L_L}{C_{L2}} - j\frac{R_L}{\omega C_{L2}}\right)\right]}{(1 - \omega^2 C_{p1} L_a + j\omega C_{p1} R_a)\left[\left(2Z_0 + \frac{1}{j\omega C_{L1}}\right)\left(R_L + j\left(\omega L_L - \frac{1}{\omega C_{L2}}\right)\right) + \left(\frac{L_L}{C_{L2}} - j\frac{R_L}{\omega C_{L2}}\right)\right] + (R_a + j\omega L_a)\left[R_L + 2Z_0 + j\left(\omega L_L - \frac{1}{\omega C_{L1}}\right)\right]} \tag{10b}$$

$$Z_{1be} = \frac{1 + (R_R + j\omega L_R)\left[j\omega(C_{R2} + C_{pr}) + \frac{1}{R_a + j\omega L_a} + \frac{1}{Z_0}\right]}{j\omega C_{R1} + (1 - \omega^2 C_{R1} L_R + j\omega C_{R1} R_R)\left[j\omega(C_{R2} + C_{pr}) + \frac{1}{R_a + j\omega L_a} + \frac{1}{Z_0}\right]} \tag{11a}$$

$$Z_{2be} = \frac{\frac{2Z_0}{j\omega C_{R1}} + (R_R + j\omega L_R)(2Z_0 + \frac{1}{j\omega C_{R1}})}{2Z_0 + \frac{1}{j\omega C_{R1}} + \left[\frac{2Z_0}{j\omega C_{R1}} + (R_R + j\omega L_R)\left(2Z_0 + \frac{1}{j\omega C_{R1}}\right)\right]\left[j\omega(C_{R2} + C_{pr}) + \frac{1}{R_a + j\omega L_a}\right]} \tag{11b}$$

$$Z_{2ao} = \frac{-Z_p\left[\frac{R_L}{\omega^2 C_{pl}}(C_{L1} + C_{L2}) + j\left(\frac{L_L}{\omega C_{pl}}(C_{L1} + C_{L2}) - \frac{1}{\omega^3 C_{pl}}\right)\right]}{\left[L_L(C_{L1} + C_{L2}) - \frac{1}{\omega^2} - j\frac{R_L}{\omega}(C_{L1} + C_{L2})\right]\left(Z_p + \frac{1}{j\omega C_{pl}}\right) + \frac{Z_p}{C_{L1}C_{L2}}\left(\frac{L_L C_{L1} C_{L2}}{C_{pl}} - \frac{C_{L2}}{\omega^2 C_{pl}} - j\frac{R_L C_{L1} C_{L2}}{\omega C_{pl}}\right)} \tag{12a}$$

$$Z_{2bo} = \frac{Z_p(R_R + j\omega L_R)}{R_R + j\omega L_R + Z_p + j\omega Z_p(C_{R2} + C_{pr})(R_R + j\omega L_R)} \tag{12b}$$

The impedances of the common inductor for the even mode, Z_{ce}, and odd mode, Z_{co}, are

$$Z_{ce} = R_a + j\omega L_a \tag{13a}$$

$$Z_{co} = R_a + 2R_b + j\omega(L_a + 2L_b) \tag{13b}$$

The impedance of the parallel branch in Figure 9 is

$$Z_p = \frac{j\omega C_2}{2 - \omega^2 C_2(L_a + 2L_b) + j\omega C_2(R_a + 2R_b + 2R_p)} \tag{14}$$

In summary, the design equations are

$$Z_{1ae} = 2Z_o \tag{15a}$$

$$Z_{2ae} = Z_o \tag{15b}$$

$$Z_{1be} = 2Z_o \tag{15c}$$

$$Z_{3be} = Z_o \tag{15d}$$

$$Z_{2ao} = Z_o \tag{15e}$$

$$Z_{3bo} = Z_o \tag{15f}$$

which can be applied to find capacitors, inductors, and common inductor values.

4. Simulated and Measured Results

Balun circuits were designed to operate at 10 GHz. For the ideal lumped circuit simulation study, Equation (15) was applied to find optimum component values for fixed quality factor (Q) values of all inductors. The study used Q values of 1000, 100, and 10. Then, the balun circuit was designed and implemented on an 0.18-µm CMOS process. All the design component values are shown in Table 2. Design 1, 2, and 3 and parasitic components were found by using (15), while the 'Layout' components were found by using Advanced Design System (ADS) software (2014).

Table 2. Component values of various balun designs.

Design	Left-Handed Transmission Line				Right-Handed Transmission Line				Common Inductor		Other Components	
	C_{L1} (pF)	C_{L2} (pF)	L_L (nH)	C_{pl} (pF)	C_{R1} (pF)	C_{R2} (pF)	L_R (nH)	C_{pr} (pF)	L_a (nH)	L_b (nH)	C_2 (pF)	R_p (Ω)
1 (Q = 1000)	0.27	0.19	0.95	0.30	0.17	0.47	0.95	0.10	0.50	0.22	0.94	12.87
2 (Q = 100)	2.99	0.23	1.13	0.24	0.22	0.51	1.13	0.16	0.57	0.24	0.75	7.97
3 (Q = 10)	0.42	0.26	1.19	0.10	0.21	0.11	1.19	0.24	1.93	0.11	0.28	15.00
Parasitic	0.268	0.362	0.953	0.3	0.31	0.14	0.953	0.411	1.926	0.11	0.29	0.1
Layout	0.462	0.265	0.953	0.11	0.10	0.10	0.953	0.276	1.926	0.11	0.246	-

For the layout design, the common inductor was designed to have L_a = 1.926 nH and L_b = 0.11 nH. Figure 10 shows the chip photo. The size of the circuit is merely 1019 µm × 764 µm, or $0.025\lambda_0 \times 0.034\lambda_0$. In order to account for the layout effect, parasitic inductors were added to the circuit model, as shown in Figure 11. Design Equation (15) can still be applied with Equations (10)–(12), adjusted accordingly. Without loss of generality, the modified equations are not presented here but they can be easily found using the method described above. The estimated parasitic inductors at 10 GHz are shown in Table 3, while the designed components are shown in Table 2 as 'Parasitic'.

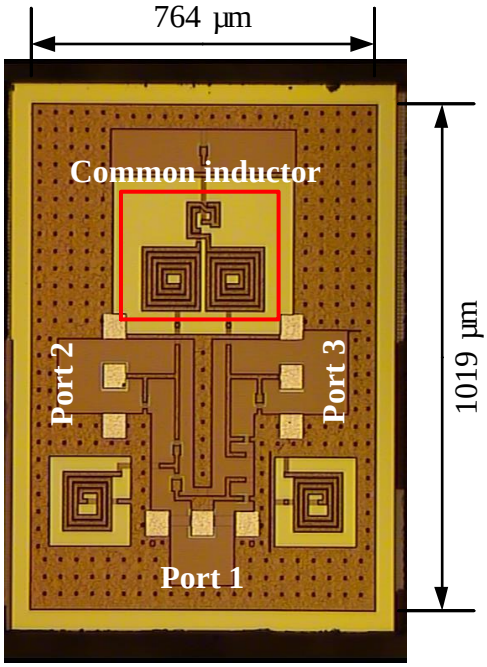

Figure 10. Balun circuit photo.

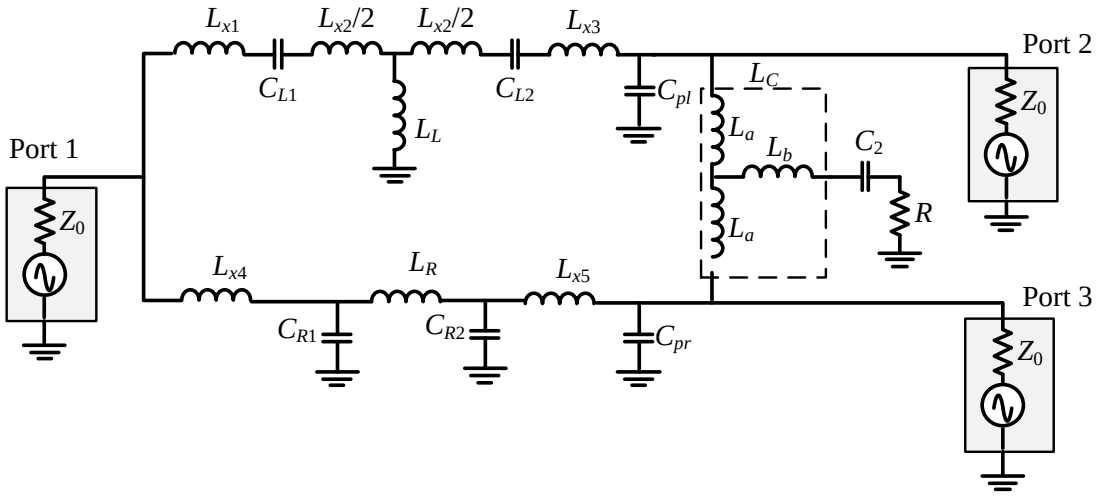

Figure 11. Lumped balun circuit with parasitic inductors.

Table 3. Estimated parasitic inductors from the layout at 10 GHz.

Parasitic Inductor	Resistance (Ω)	Inductance (nH)
L_{x1}	0.273	0.072
L_{x2}	0.319	0.012
L_{x3}	1.246	0.142
L_{x4}	0.371	0.038
L_{x5}	0.935	0.09

For the layout, all other lumped components were adjusted using ADS to account for the parasitic parts of the layout. The inductors in both transmission lines were set at L_L = L_R = 0.953 nH. The capacitors of the left-handed transmission line were optimized to C_{L1} = 0.462 pF, C_{L2} = 0.265 pF, C_{pl} = 0.11 pF and those of the right-handed transmission line were

C_{R1} = 0.1 pF, C_{R2} = 0.1 pF, C_{pr} = 0.276 pF. Because the optimized resistor R value was small, it was omitted from the circuit layout.

Figure 12 shows the comparison of $|S_{11}|$, $|S_{22}|$, $|S_{33}|$, $|S_{21}|$, $|S_{31}|$, and $|S_{23}|$ of the simulated and measured results. The ideal circuits with different Q values are referred to as 'Design Q = 1000', 'Design Q = 100', 'Design Q = 10' and 'Design_parasitic'. The layout simulation and measured results were referred to as 'layout simulation' and 'measurement'. The measurement was performed by a Keysight network analyzer, Model N5247A.

For the ideal lump circuits, the performances of the baluns are similar to an ideal one if the quality factor of inductors is high, e.g., Q = 1000 and Q = 100. The balun performances worsen as the quality factor of the inductors is lower, Q = 10. The reflection coefficients rise with the lower Q inductors as port impedance matching worsens. The transmission coefficients are also lower because of signal loss on lossy components and impedance mismatch. The output signal coupling between the output ports also rises due to the port impedance mismatch. The simulation study results imply that the balun performance limitation is related to the quality factor of the inductors.

'Design_parasitic', 'layout simulation', and 'measurement' yielded similar performance to the 'design Q = 10'. In particular, 'Design_parasitic' and 'layout simulation' were very close in all values at 10 GHz. For the design choices, 'layout simulation' just needed some adjustments from 'Design_parasitic', e.g., capacitor values, to account for the complex layout effect. The 'measurement' performance had A small deviation from 'layout simulation'. The measured reflection coefficients of all ports were below −22.6 dB, while the simulated ones were below −17.8 dB. The measured transmission coefficients were more than −4.99 dB at both output ports. The measured phase difference at the output ports was 174.9°. Table 4 shows the comparison of this work with previously reported on-chip baluns.

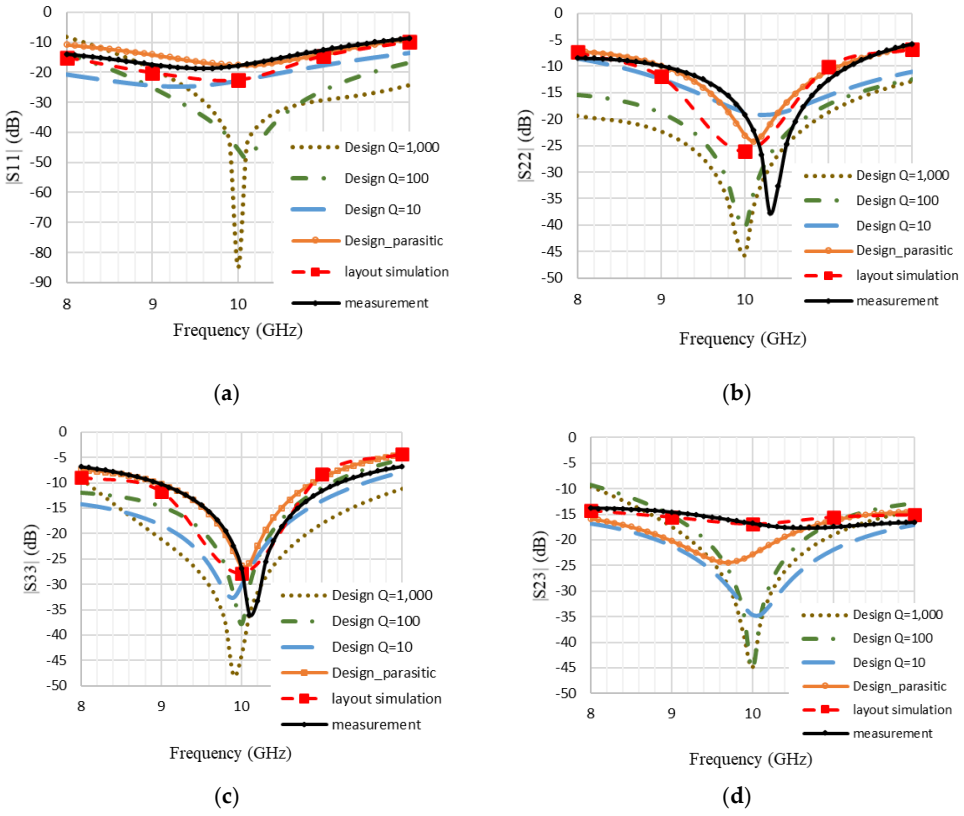

Figure 12. *Cont.*

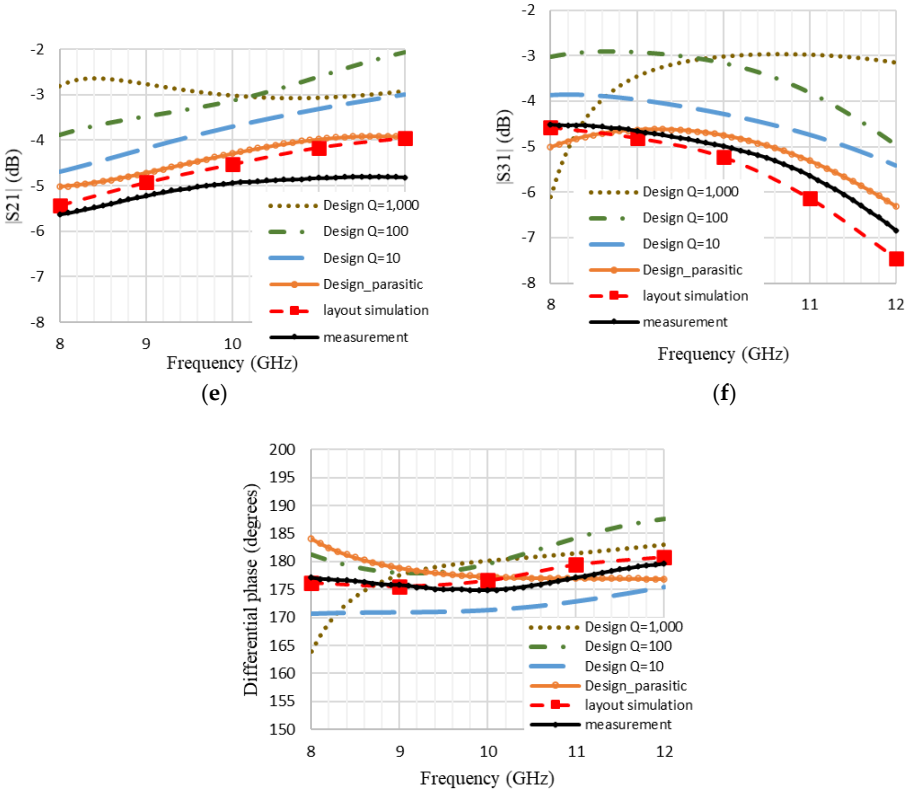

Figure 12. Frequency response of the simulated and measured balun. (**a**) |S11|, (**b**) |S22|, (**c**) |S33|, (**d**) |S23|, (**e**) |S21|, (**f**) |S31|, (**g**) differential phase output.

Table 4. Comparison of previously reported on-chip baluns.

Refs.	[2] Balun	[2] Miniature Balun	[8]	[15]	This Work
Process	0.18 µm CMOS	0.18 µm CMOS	0.18 µm CMOS	IPD	0.18 µm CMOS
f_0(GHz)	37.8	36.9	94	2.4	10
$\lvert S_{21} \rvert$, $\lvert S_{31} \rvert$ (dB)	>−6.281	>−5.809	>−6.178	−3.25	>−4.99
$\lvert S_{11} \rvert$, $\lvert S_{22} \rvert$, $\lvert S_{33} \rvert$ (dB)	<−9.6	<−14.5	<−6.3	−21	<−17.8
$\lvert S_{23} \rvert$ (dB)	−20.9	−16.8	−6 *	N/A	<−16.8
Amplitude balance (dB)	1.227	0.637	0.098	0.45	0.045
Phase difference deviation (degrees)	0	0	−4.9	2.6	5.1
Size ($\lambda_0 \times \lambda_0$)	1.1×10^{-3}	1×10^{-3}	3.5×10^{-3}	1.12×10^{-3}	8.662×10^{-4}

* Estimation.

In Table 4, the measurement of the proposed balun showed that the transmission coefficient was the best among other circuits based on lossy CMOS processes. It had the smallest size and amplitude balance among all circuits. Moreover, the reflection and isolation coefficients were all low. The measured results indicated good performance in narrowband applications.

5. Conclusions

The balun circuit was designed and implemented on a standard 0.18-μm CMOS process to operate at 10 GHz. The proposed topology uses left- and right-handed transmission lines to generate out-of-phase output signals at the output ports. With the modified lumped transmission line circuits, only single-section lines were used to replace $\lambda/4$ distributed transmission lines. A common inductor was also used to replace larger transmission line circuits. The resulting circuit was small at 1019 μm × 764 μm, or $0.025\lambda_0 \times 0.034\lambda_0$. It is convinced that the superior electrical performances and compact size of the design were suitable for narrowband applications.

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