electronics

MDPI

Article

Design and Analysis of Complementary Metal–Oxide–Semiconductor Single-Pole Double-Throw Switches for 28 GHz 5G New Radio

Yo-Sheng Lin [1,*], Chin-Yi Huang [1], Chung-Ta Huang [1], Jin-Fa Chang [2], Nai-Wen Tien [1] and Yu-Hao Chuang [1]

[1] Department of Electrical Engineering, National Chi Nan University, Puli 54561, Taiwan; s107323509@ncnu.edu.tw (C.-Y.H.)
[2] Department of Electronic Engineering, National Changhua University of Education, Changhua 50074, Taiwan; jfchang@cc.ncue.edu.tw
* Correspondence: stephenlin@ncnu.edu.tw

Abstract: We propose a single-pole double-throw (SPDT) switch with low insertion loss (IL), high isolation, and high linearity for a 28 GHz 5G new radio. The transmit (TX) path is a π-network consisting of a parallel dynamic-threshold metal–oxide–semiconductor (DTMOS) transistor, M_1, with large body-floating resistance, R_B (DTMOS-R M_1), a series one-eighth-wavelength (λ/8) transmission line (TL), and a parallel capacitance, C_{ant}. The series λ/8-TL in conjunction with the parallel C_{ant} and transistors' capacitance constitute an equivalent λ/4-TL with a characteristic impedance of 50 Ω. This leads to low IL in the TX mode and decent isolation in the receive (RX) mode. The RX path is an L-network constituting a series impedance (of parallel inductance L_1 and DTMOS-R M_2) and a parallel DTMOS-R M_3. This leads to a decent IL in the RX mode and isolation in the TX mode. The first SPDT switch (SPDT SW1) is designed and implemented in a 90 nm complementary metal–oxide–semiconductor (CMOS) with a top metal thickness (TMT) of 3.4 μm. A comparative SPDT switch (SPDT SW2) in a 0.18 μm CMOS with a thinner TMT of 2.34 μm is also designed and implemented. In the TX mode, SPDT SW1 achieves a measured IL of 0.67 dB at 28 GHz and 0.58–1 dB for 17–34.9 GHz and a measured isolation of 44.3 dB at 28 GHz and 25.6–62.3 dB for 17–34.9 GHz, one of the best IL and isolation results ever reported for millimeter-wave CMOS SPDT switches. The measured input 1 dB compression point (P_{1dB}) is 28.5 dBm at 28 GHz. Moreover, in the RX mode, SPDT SW1 attains a measured IL of 1.9 dB at 28 GHz and 1.83–2.1 dB for 25–38.3 GHz and an isolation of 25 dB at 28 GHz and 24.5–27 dB for 25–38.3 GHz. The measured P_{1dB} is 24 dBm at 28 GHz.

Keywords: CMOS; SPDT switch; equivalent quarter-wavelength TL; insertion loss (IL); isolation; linearity; millimeter-wave; DTMOS; body-floating resistance R_B

Citation: Lin, Y.-S.; Huang, C.-Y.; Huang, C.-T.; Chang, J.-F.; Tien, N.-W.; Chuang, Y.-H. Design and Analysis of Complementary Metal–Oxide–Semiconductor Single-Pole Double-Throw Switches for 28 GHz 5G New Radio. *Electronics* **2023**, *12*, 4156. https://doi.org/10.3390/electronics12194156

Academic Editors: Simona Donati Guerrieri and Lida Kouhalvandi

Received: 27 July 2023
Revised: 29 September 2023
Accepted: 2 October 2023
Published: 7 October 2023

1. Introduction

A millimeter-wave (mm wave) single-pole double-throw (SPDT) switch is a crucial component in mm wave phased-array transceivers. It is used in switching between the transmit (TX) mode and receive (RX) mode of each array element [1–13]. The requirements of an SPDT switch include low insertion loss (IL), good TX-to-RX isolation in the TX mode, good antenna-to-TX isolation in the RX mode, and decent power handling capability (evaluated via the input 1 dB compression point (P_{1dB})) in the TX and RX modes [3–10]. CMOS processes have the advantages of high integration and relatively low cost. Recently, several mm wave CMOS SPDT switches have been reported [3–6]. However, their overall performance still has room for improvement. For instance, [3] demonstrates a 21–38 GHz SPDT switch using body-floating resistance (R_B) and negative body bias (V_B) for the NMOS switch transistors in a 0.18 μm CMOS. A high P_{1dB} of 25.6 dBm at 28 GHz is achieved. However, its IL of 3.6–5.9 dB is not low enough due to the high loss of the π-matching CLC-network at the input port (port 1) and the travelling-wave matching CLCL-network

at the output ports (ports 2 and 3). The author of [4] reports a symmetrical 25–39.5 GHz SPDT switch using a switched inductor in a 65 nm CMOS. A low IL of 0.89–1.5 dB is achieved. Yet, its isolation of 18.2 dB and P_{1dB} of 12.55 dBm are not satisfactory because the on-state channel resistance (R_{on}) of the switch transistors is not low enough, and the off-state impedance (R_{off}) of the switch transistors is not high enough. In [5], an asymmetrical 25–30 GHz SPDT switch with matching network and body-floating resistance, R_B, in a 65 nm CMOS is demonstrated. It achieves a low IL of 0.74–1.16/0.96–1.1 dB in the RX/TX mode and a high P_{1dB} of 31.8 dBm in the TX mode. However, an isolation of 16.4 dB and P_{1dB} of 5.2 dBm in the RX mode indicates that there is still room for improvement. This is mainly because the R_{off} of the series switch transistor in the TX path is not high enough. In [6], an asymmetrical 20–25 GHz SPDT switch with matching network and body-floating resistance, R_B, in a 65 nm CMOS is reported. It achieves a low IL of 1.5–2/1.8–2.1 dB in the RX/TX mode and a high P_{1dB} of 32.5 dBm in the TX mode. However, its P_{1dB} of 4.7 dBm in the RX mode is not good enough because of the poor open circuit of the TX path due to the poor ground of the parallel stack-transistor at the TX node.

The body-floating transistor technique, i.e., an NMOS transistor with large body-floating resistance, R_B, connected to the ground or a negative bias voltage (denoted as NMOS-R), is effective in substrate leakage (I_B) suppression [3]. Therefore, it is widely used in SPDT switches for a high P_{1dB} [14] and in LNAs for low noise [15]. Due to threshold voltage (V_{th}) reduction, the on-state dynamic threshold MOSFET (DTMOS), i.e., the gate connected to the body, and then, connected to a positive bias voltage, is useful in low-voltage and power circuits [16]. For a high-power-operated SPDT switch, I_B suppression is crucial for a low IL and a high P_{1dB}. Large body-floating resistance, R_B, (refer to Figures 1 and 2), normally 2–10 kΩ, can be included in the DTMOS (denoted DTMOS-R) for on-/off-state I_B suppression. This can be explained in more detail as follows: In the on-state, the body-to-source (B-to-S) junction of the DTMOS-R is forward-biased due to the connection of the body and gate, corresponding to a smaller threshold voltage (V_{th}), and hence, a lower R_{on}, i.e., a better on-state. This leads to a lower IL of the SPDT switch due to the better on-state of the series DTMOS-R. Moreover, the inclusion of a large R_B can significantly reduce I_B since the gate bias $V_G = I_B R_B + V_{BS}$, in which V_{BS} is the forward-biased B-to-S voltage. In other words, I_B reduces with an increase in R_B in the on-state. In the off-state, the B-to-S junction of the DTMOS-R is reverse-biased, corresponding to a larger V_{th}, and hence, a higher R_{off}, i.e., a better off-state. This leads to a lower IL of the SPDT switch due to the better off-state of the parallel DTMOS-R. Moreover, the inclusion of a large R_B can reduce I_B since the gate bias $V_G = I_B R_B + V_{BS}$, in which V_{BS} is the reverse-biased B-to-S voltage. In other words, I_B reduces with an increase in R_B in the off-state. Furthermore, I_B (suppression) simulation can be conducted using the function of I_Probe in Advanced Design System (ADS), a piece of circuit design and simulation software provided by Agilent Technologies, Santa Clara, United States. That is, the simulated I_B can be obtained through the insertion of the icon of an I_Probe in the R_B path between the control voltage (V_{sw1} or V_{sw2}) and gate/body nodes of a DTMOS-R in the schematic.

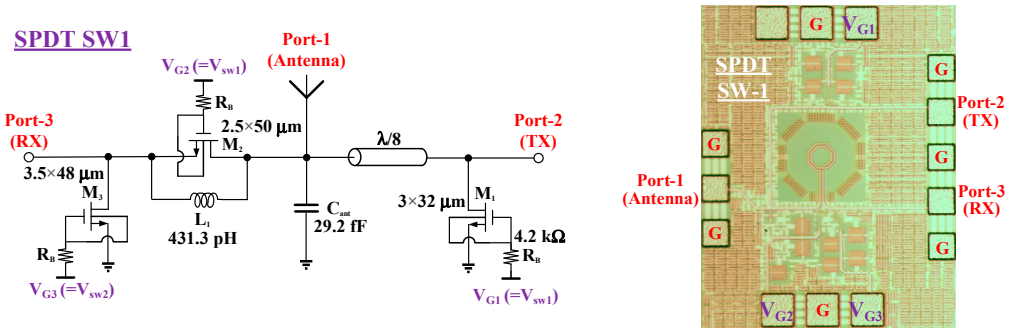

Figure 1. Circuit diagram and chip photo of the SPDT switch in a 90 nm CMOS (SPDT SW1).

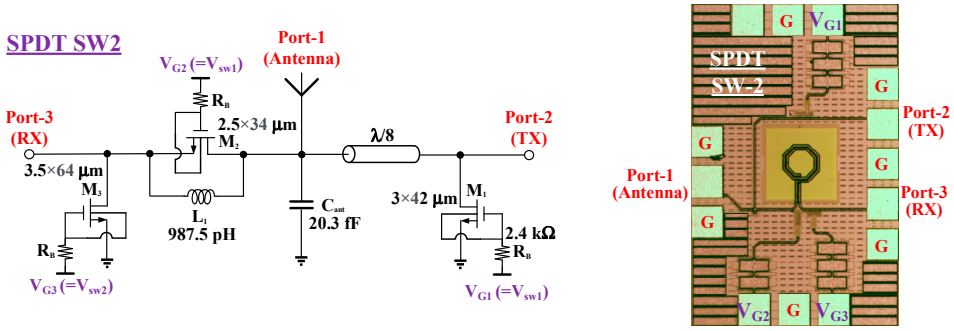

Figure 2. Circuit diagram and chip photo of the SPDT switch in a 0.18 µm CMOS (SPDT SW2).

In this work, we propose a CMOS SPDT switch with a low IL, high isolation, and a decent P_{1dB} for a 28 GHz 5G NR. The first SPDT switch (SPDT SW1) is designed and implemented in a 90 nm CMOS with a top metal thickness (TMT) of 3.4 µm. A comparative SPDT switch (SPDT SW2) in a 0.18 µm CMOS with a thinner TMT of 2.34 µm is also designed and implemented. Figure 1 shows a circuit diagram and chip photo of SPDT SW1. Figure 2 shows a circuit diagram and chip photo of SPDT SW2. The transistor size and important component parameters are also labeled. The chip area, excluding the DC and RF pads, is 0.26 × 0.26 mm^2, i.e., 0.068 mm^2. R_B values of 4.2 kΩ and 2.4 kΩ are used for SPDT SW1 and SPDT SW2, respectively. In the TX path, a parallel DTMOS-R, a series TL (equivalent λ/4 TL), and parallel capacitance, C_{ant}, are included for a low IL in the TX mode and decent isolation in the RX mode. In the RX path, a series impedance and a parallel DTMOS-R are included for a high-P_{1dB} in the RX mode and decent isolation in the TX mode.

2. SPDT Switch Design

The SPDT SW1 is designed via a 1P9M 90 nm CMOS process. Figure 3 shows a cross-sectional illustration diagram of the 90 nm CMOS process. The interconnection lines and the TL inductors are placed on the 3.4 µm thick topmost metal (MT_9) to minimize the resistive loss. The bottom-most metal (MT_1) with a pattern density of 70% is used as the ground plane of the TLs. The distance (D) between MT_9 and MT_1 is 6.085 µm. To avoid performance degradation, the space between the TLs is at least 5 times that of D (i.e., 30.425 µm) to control the mutual coupling and parasitics [17–20]. The RX path is an L-network constituting a series impedance (of a parallel inductance L_1 and a DTMOS-R M_2) and a parallel DTMOS-R M_3. This leads to high linearity in the RX mode and decent isolation in the TX mode. Moreover, the TX path is a π-network consisting of a parallel DTMOS-R M_1, a series λ/8 TL, and a parallel capacitance, C_{ant}. A Low IL in the TX mode and good isolation in the RX mode are achieved since the series λ/8-TL in conjunction with the parallel C_{ant} and parasitic capacitance of the DTMOS-R transistors M_1/M_2 constitute an equivalent λ/4-TL with a characteristic impedance (Z_C) of 50 Ω. The gate width of transistors M_1/M_2 (96-/125 µm for SPDT SW1) is determined according to the required parallel capacitance, C_P (in Figure 4), to constitute a λ/8-TL-based λ/4-TL in the TX path. A DTMOS-R transistor, M_3, with a relatively large gate width (168 µm for SPDT SW1) is adopted to achieve a better TX-to-RX isolation in the TX mode. The cost is a slight increase in IL in the RX mode due to lower off-state parallel resistance R_{off3}. In other words, a trade-off exists between the TX-to-RX isolation in the TX mode and the IL in the RX mode.

The reason why the L-type network (in both the RX path and TX path) of the SPDT switch can achieve high linearity and decent isolation in both the RX and TX modes can be explained in more detail as follows. Ideally, in the RX mode, transistors M_1 and M_2 are in the on-state (i.e., short circuit) and M_3 is in the off-state (i.e., open circuit). The λ/8-TL, parallel C_{ant}, and parallel capacitance of M_1/M_2 constitute an equivalent λ/4-TL, leading to an infinite input impedance Z_{in} (i.e., open circuit) looking from the antenna node to the TX node since a short-circuit-loaded λ/4-TL exhibits an infinite Z_{in}. That is, ideally, perfect

(antenna-to-TX) isolation in the RX mode is achieved. And perfect IL, linearity, and Z_{in} matching (at the RX and antenna nodes) are also achieved. Moreover, ideally, in the TX mode, transistors M_1 and M_2 are in the off-state (i.e., open circuit) and M_3 is in the on-state (i.e., short circuit). Inductance L_1 and the off-state capacitance $C_{ds2,off}$ of M_2 are in parallel resonance (i.e., open circuit) at an operation frequency of 28 GHz, leading to an infinite Z_{in} (i.e., open circuit) looking from the antenna node to the RX node. The $\lambda/8$-TL, parallel C_{ant}, and parallel capacitance of M_1/M_2 constitute an equivalent $\lambda/4$-TL with a Z_C of 50 Ω. That is, ideally, no IL in the TX mode is achieved due to the lossless equivalent $\lambda/4$-TL with a Z_C of 50 Ω in the TX path and an open circuit of the RX path. And perfect (TX-to-RX) isolation, linearity, and Z_{in} matching (at the TX and antenna nodes) are also achieved.

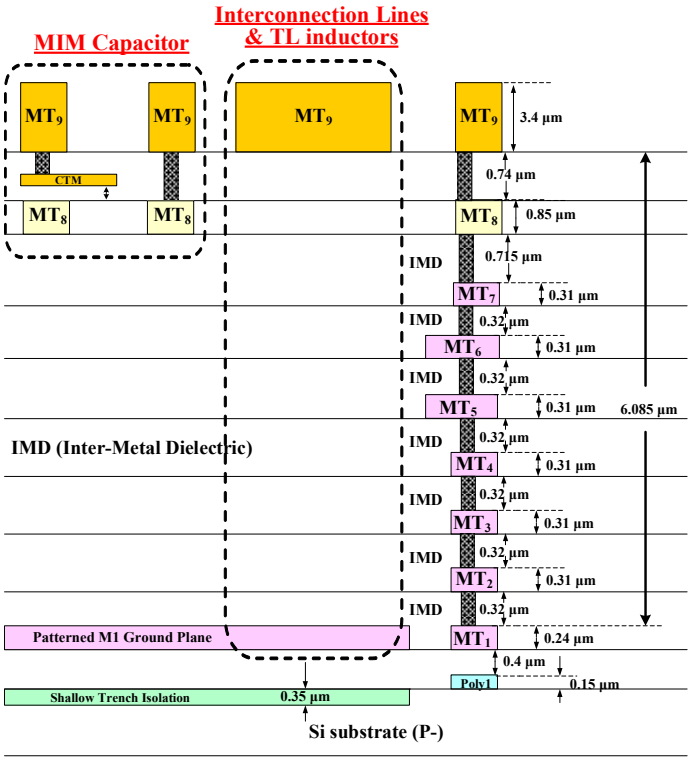

Figure 3. Cross-sectional illustration diagram of the 90 nm CMOS process.

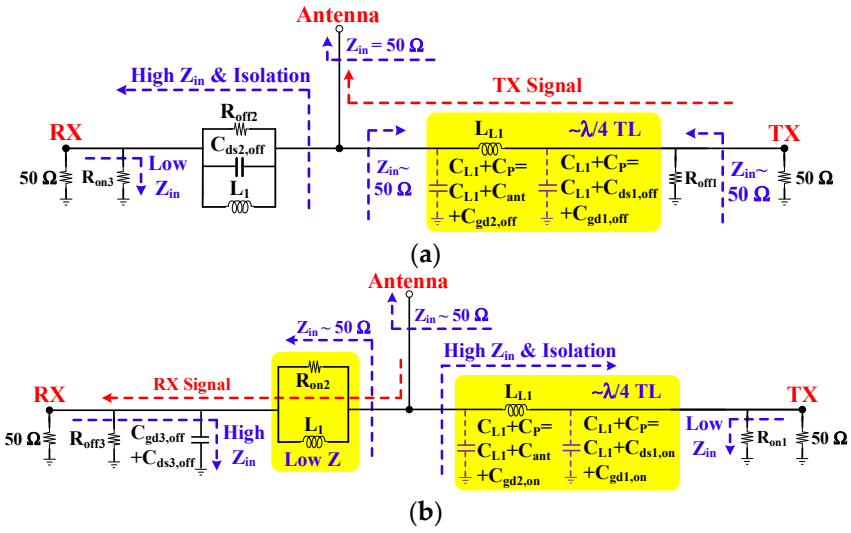

Figure 4. Equivalent circuit of the proposed SPDT switch in (**a**) the TX and (**b**) the RX mode.

The reason why a series DTMOS-R transistor is used in the RX path but not adopted in the TX path is for achieving a lower IL, higher linearity, and a better isolation in the TX mode. This can be explained in more detail as follows. To avoid high power loss in the high-output-power TX path, low IL and high linearity are essential for the TX path of an SPDT switch. Compared with a series active DTMOS-R transistor in the on-state, a series passive TL shows a lower IL and higher linearity (due to its metal-based structure). Moreover, compared with an equivalent λ/4-TL with a short-circuited load, a series DTMOS-R transistor in the off-state normally shows a better open circuit (needed for the high isolation operation of the RX path in the TX mode) due to the switching property of the transistor. Therefore, a series DTMOS-R transistor is used in the RX path. Instead of using a series DTMOS-R transistor (in the RX path), a λ/8-TL-based λ/4-TL is used in the TX path for a low IL, high linearity, and high isolation.

The SPDT SW2 is designed via a 1P6M 0.18 μm CMOS process. The interconnection lines and the inductors are placed on the 2.34 μm thick MT_6 to minimize the resistive loss. The lowermost MT_1 with a pattern density of 90% is used as the ground plane of the TLs. The D between MT_6 and MT_1 is 5.14 μm. To avoid performance degradation, the space between the TLs is at least 5 times that of D (i.e., 25.7 μm) to control the mutual coupling and parasitics. The design and simulation of the spiral inductor L_1 and the λ/8-TL are conducted using ADS Momentum, a 2.5D EM piece of simulation software (suitable for the planar inductor and TL simulation) provided by Agilent Technologies, Santa Clara, United States. Then, EM-circuit co-simulation is performed using ADS to ensure the post-layout simulation results are close to the measured ones.

For the CMOS SPDT switches in the literature, a gate voltage (or control voltage) V_G of 1.8 V is normally adopted to turn on the switch transistors, and a V_G of −1.8 V is normally used to turn off the switch transistors. For a fair comparison, V_G values of 1.8 V and −1.8 V, respectively, are adopted to turn on and turn off the switch transistors in this work. To obtain a better IL, isolation, and linearity performance, a V_G slightly higher than 1.8 V can be adopted to turn on the switch transistors to achieve a better on-state (i.e., lower on-state channel resistance), and a V_G slightly lower than −1.8 V can be adopted to turn off the switch transistors to achieve a better off-state (i.e., higher off-state channel resistance). Figure 4a shows the equivalent circuit of the SPDT switch in the TX mode. The control voltage V_{sw1} (=V_{G1} = V_{G2}) is equal to −1.8 V, and V_{sw2} (=V_{G3}) is equal to 1.8 V. That is, transistors M_1 and M_2 (controlled by V_{sw1}) are in the off-state and M_3 (controlled by V_{sw2}) is in the on-state. Ideally, R_{off1} and R_{off2} are high-resistance and R_{on3} is low-resistance (close to 0). According to the TL theory, the series λ/8-TL is equivalent to a series inductance L_{L1} and two parallel end-capacitance C_{L1}. The π-network consisting of a parallel end-capacitance C_{L1}+ $C_{ds1,off}$ +$C_{gd1,off}$ (i.e., C_{L1} + C_P), a series inductance L_{L1}, and a parallel end-capacitance C_{L1} + C_{ant} + $C_{gd2,off}$ (i.e., C_{L1} + C_P) in the TX path is equivalent to a λ/4-TL with a Z_C of 50 Ω. The parallel $C_{ds2,off}$ and L_1 in the RX path are designed to be in resonance and open at a center frequency of 28 GHz. This leads to decent input impedance matching at the TX and antenna nodes (i.e., a decent S_{11} and S_{33}), a low IL, and high TX-to-RX isolation. This can be explained in more detail as follows. In the RX path of the SPDT switch, inductor L_1 is in parallel with DTMOS-R M_2. In the RX mode, DTMOS-R M_2 is in the on-state, equivalent to a small resistance R_{on2},to achieve a decent IL. L_1 is negligible since R_{on2} dominates the RX path impedance. In the TX mode, DTMOS-R M_2 is in the off-state, equivalent to a large resistance R_{off2}, in parallel with a capacitance $C_{ds2,off}$. To achieve decent isolation with the RX path, L_1 and $C_{ds2,off}$ should be in parallel resonance at an operation frequency of 28 GHz. For SPDT SW1, $C_{ds2,off}$ is equal to 74.9 fF, so an L_1 of 431.3 pH is chosen. For SPDT SW2, $C_{ds2,off}$ is equal to 32.7 fF, so an L_1 of 987.5 pH is used.

The design and simulation of the λ/8-TL-based equivalent λ/4-TL in the TX path can be explained in more detail as follows. According to the TL theory, the ABCD matrix of a lossless TL with electrical length of θ is given by [21]

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} \cos(\theta) & jZ_C \sin(\theta) \\ j\sin(\theta)/Z_C & \cos(\theta) \end{bmatrix} \quad (1)$$

From (1), Z_C and θ can be written as

$$Z_C = \sqrt{B/C} \tag{2}$$

$$\theta = \cos^{-1}(A) \left(\text{or } \cos^{-1}(D)\right) \tag{3}$$

That is, the Z_C and θ of a TL can be obtained from the simulated ABCD-parameters converted from the simulated S-parameters. For a lossless TL with a θ of 90° (i.e., length of λ/4) and Z_C of R_0 (i.e., 50 Ω), (1) can be simplified as

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} 0 & jR_0 \\ j/R_0 & 0 \end{bmatrix} \tag{4}$$

Additionally, the lossless TL can be modeled by a π-network consisting of a series inductor (L_L) and two parallel end capacitors (C_L). The ABCD matrix of the π-network is given by

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} 1-\omega_0^2 L_L C_L & j\omega_0 L_L \\ j\omega_0 C_L(2-\omega_0^2 L_L C_L) & 1-\omega_0^2 L_L C_L \end{bmatrix} \tag{5}$$

If we let (5) equal (4), we obtain

$$L_L = \frac{R_0}{\omega_0} \tag{6}$$

$$C_L = \frac{1}{R_0 \omega_0} \tag{7}$$

In Figure 4a, two additional parallel capacitances C_P (equal to $C_{ds1,off}$ + $C_{gd1,off}$ or C_{ant}+ $C_{gd2,off}$) are incorporated to the shorter (electrical length θ_1 of 45° or length of λ/8 in this work) TL with a Z_C of Z_{C1} to form an equivalent λ/4 TL. It has the potential of a small chip area since the TL θ_1 (45° in this work) can be any value less than or equal to 90° in theory. For the TL, suppose the corresponding L_L is L_{L1}, and C_L is C_{L1}. From (1) and (5), L_{L1} and C_{L1} can be written as

$$L_{L1} = \frac{Z_{C1} \sin\theta_1}{\omega_0} \tag{8}$$

$$C_{L1} = \frac{1-\cos\theta_1}{\omega_0 Z_{T1} \sin\theta_1} \tag{9}$$

The equivalence of the λ/8 TL with a Z_C of Z_{C1} (i.e., C_{L1}-L_{L1}-C_{L1} π-network) and two additional parallel capacitances (C_P) to a λ/4 TL with a Z_C of R_0 (i.e., C_L-L_L-C_L π-network) requires L_{L1} = L_L and C_{L1} + C_P = C_L. This leads to Z_{C1} and C_P, given by

$$Z_{C1} = \frac{R_0}{\sin\theta_1} \tag{10}$$

$$C_P = \frac{\cos\theta_1}{R_0 \omega_0} \tag{11}$$

In this work, θ_1 is equal to 45° (i.e., length of λ/8). From (10) and (11), the required Z_{C1} of the λ/8-TL is 70.7 Ω, and the required additional parallel capacitance, C_P, is 80.4 fF.

Figure 4b shows the equivalent circuit of the SPDT switch in the RX mode. The control voltage V_{sw1} is equal to 1.8 V and V_{sw2} is equal to −1.8 V. That is, transistors M_1 and M_2 are in the on-state and M_3 is in the off-state. Ideally, R_{on1} and R_{on2} are low-resistance (close to 0) and R_{off3} is high-resistance. The π-network consisting of parallel end-capacitance (C_{L1} + $C_{ds1,on}$ + $C_{gd1,on}$), series inductance (L_{L1}), and parallel end-capacitance (C_{L1} + C_{ant} + $C_{gd2,on}$) in the TX path is roughly equivalent to a λ/4-TL with characteristic impedance of 50 Ω. Z_{in} looking from the antenna node to the TX node is infinite (i.e., an open circuit) since a short-circuit-loaded λ/4-TL exhibits an infinite Z_{in}. The parallel R_{on2} and L_1 in the RX path is low-impedance (close to

0). This leads to decent input impedance matching at the RX and antenna nodes (i.e., a decent S_{11} and S_{22}), a low IL, and high antenna-to-TX isolation.

In the TX path of the SPDT switch, the series λ/8-TL has a Z_C of 70.7 Ω. The λ/8-TL in conjunction with the end-capacitance contribution from the DTMOS-R transistors, M_1 and M_2, and capacitance, C_{ant}, constitutes a λ/4-TL with a Z_C of 50 Ω (according to Equations (10) and (11)). Figure 5a shows the simulated equivalent electrical length (θ_{eff}) versus the frequency characteristics of the TL in the TX path of SPDT SW1 according to Equation (3). The simulated ABCD parameters are converted from the simulated S-parameters. At 28 GHz, the corresponding θ_{eff} is 45.1° (about λ/4), consistent with the theoretical analysis. Figure 5b shows the simulated Z_C versus the frequency characteristics of the TL in the TX path of SPDT SW1 according to Equation (2). At 28 GHz, the corresponding Z_C is 70.7 Ω; the same applies to the theoretical value.

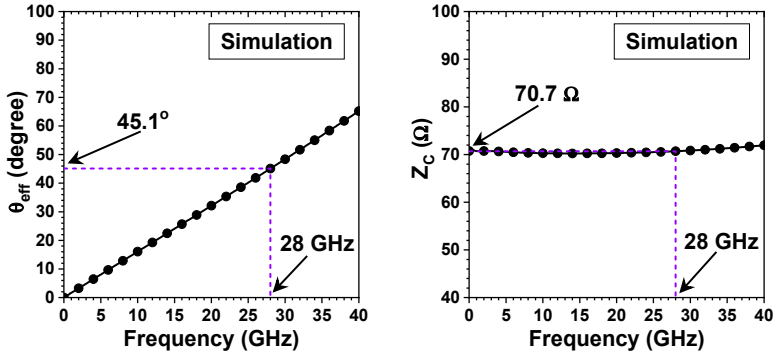

Figure 5. Simulated (**a**) θ_{eff} and (**b**) Z_C of the λ/8-TL in the TX path of SPDT SW1.

Figure 6a shows the simulated P_{1dB} of SPDT SW1 in the TX mode using the proposed DTMOS-R switching transistors and the traditional NMOS switching transistors. In the case of using DTMOS-R switching transistors, SPDT SW1 achieves a simulated IL of 0.52 dB (at a low P_{in} of −10 dBm) and P_{1dB} of 30.6 dBm. These results are better than those (simulated IL of 1.75 dB (at a low P_{in} of −10 dBm) and P_{1dB} of 11.6 dBm) using traditional NMOS switching transistors. Figure 6b shows the simulated P_{1dB} of SPDT SW1 in the RX mode using the proposed DTMOS-R switching transistors and the traditional NMOS switching transistors. In the case of using DTMOS-R switching transistors, SPDT SW1 achieves a simulated IL of 1.9 dB (at a low P_{in} of −10 dBm) and P_{1dB} of 25.4 dBm. These results are better than those (simulated IL of 3.8 dB (at a low P_{in} of −10 dBm) and P_{1dB} of 23.7 dBm) using traditional NMOS switching transistors. Overall, these results show that the proposed body-floating technique, i.e., the DTMOS-R switching transistors technique, in this work is effective for the IL and P_{1dB} enhancement of SPDT SW1 in both the TX and RX modes.

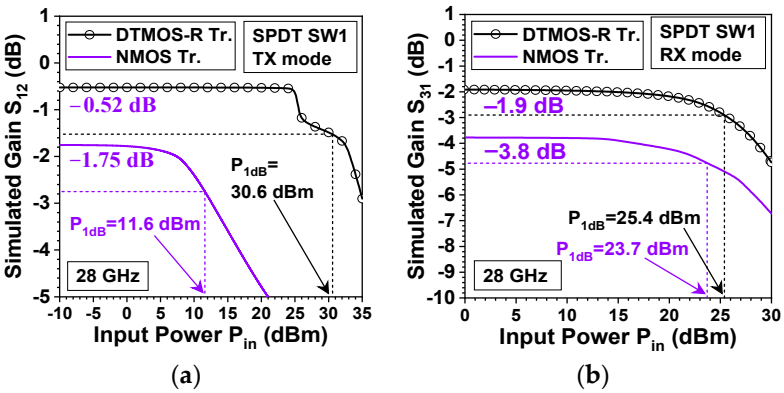

Figure 6. Simulated P_{1dB} in (**a**) the TX mode, and (**b**) the RX mode of SPDT SW1 at 28 GHz.

3. Results and Discussion of SPDT SW1

The on-wafer S-parameter measurements of SPDT SW1 and SW2 were performed using a Keysight N5227B PNA microwave network analyzer, as shown in Figure 7. Figure 8a shows the measured and simulated IL (i.e., $|S_{12}|$) and isolation (i.e., $|S_{32}|$) of SPDT SW1 in the TX mode. SPDT SW1 achieves a measured minimum IL (IL_{min}) of 0.58 dB at 24.8 GHz and an IL better than 1 dB for 17–34.9 GHz, corresponding to a 1 dB bandwidth (f_{1dB}) of 17.9 GHz. This result is close to the simulated one, i.e., an IL_{min} of 0.47 dB at 25 GHz and an IL lower than 1 dB for 15.1–39.4 GHz, corresponding to an f_{1dB} of 24.3 GHz. This decent IL is attributed to the low loss of the equivalent λ/4-TL, the good TX-RX isolation, and the high impedance of the off-state DTMOS-R M_1. Moreover, SPDT SW1 achieves a measured maximum isolation ($|S_{32}|_{max}$) of 62.3 dB at 31.4 GHz and isolation of 25.6–62.3 dB for 17–34.9 GHz. This result is close to the simulated one, i.e., an $|S_{32}|_{max}$ of 59.5 dB at 31.7 GHz and isolation of 27.7–59.5 dB for 17–34.9 GHz.

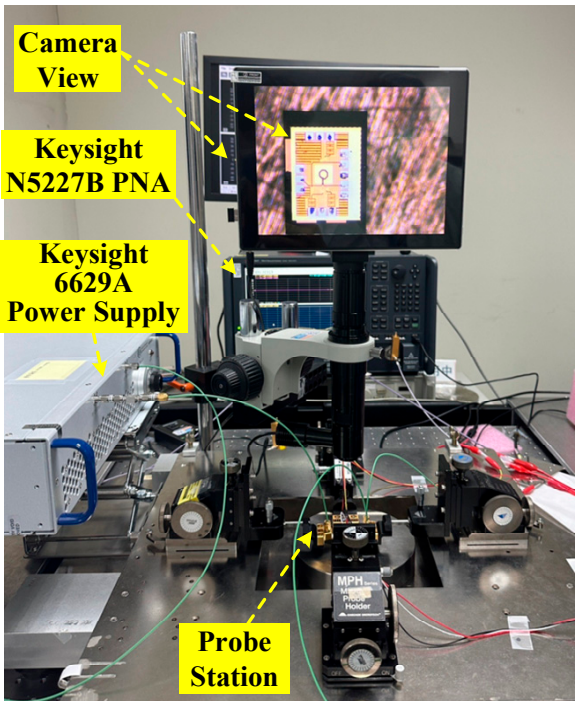

Figure 7. Measurement setup of SPDT SW1 and SW2.

Figure 8b shows the measured and simulated S_{11} and S_{22} of SPDT SW1 in the TX mode. SPDT SW1 achieves a measured minimum S_{11} ($S_{11,min}$) of −21.9 dB at 23.7 GHz and S_{11} better than −15 dB for 18.4–31.4 GHz, equivalent to a −15 dB input matching bandwidth (f_{15dB}) of 13 GHz. This result is close to the simulated one, i.e., an $S_{11,min}$ of −37.6 dB at 25.9 GHz and an f_{15dB} of 16.4 GHz (18.8–35.2 GHz). Moreover, SPDT SW1 achieves a measured minimum S_{22} ($S_{22,min}$) of −30.6 dB at 26.8 GHz and an S_{22} better than −15 dB for 18.9–39.2 GHz, equivalent to an f_{15dB} of 20.3 GHz. This result is close to the simulated one, i.e., an $S_{22,min}$ of −43.5 dB at 26.8 GHz and an f_{15dB} of 18.9 GHz (18.8–37.7 GHz).

Figure 8c shows the measured and simulated IL (i.e., $|S_{31}|$) and isolation (i.e., $|S_{21}|$) of SPDT SW1 in the RX mode. SPDT SW1 achieves a measured IL_{min} of 1.83 dB at 30.9 GHz and an IL of 1.83–2.1 dB for 25–38.3 GHz. This result is close to the simulated one, i.e., an IL_{min} of 1.33 dB at 38.4 GHz and an IL of 1.33–2.1 dB from 26.6 GHz to over 50 GHz. Moreover, SPDT SW1 achieves a measured isolation of 24.5–27 dB for 25–38.3 GHz. This result is close to the simulated one, i.e., an isolation of 22.2–25.1 dB for 25–38.3 GHz.

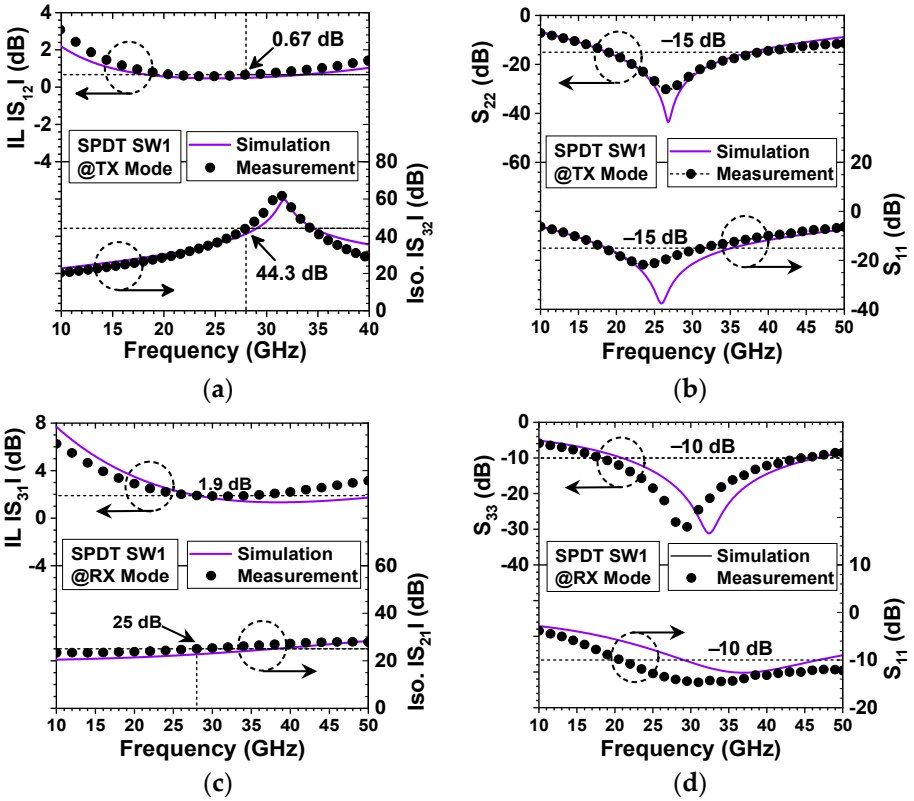

Figure 8. Measured and simulated (**a**) IL and isolation and (**b**) S_{11} and S_{22} of SPDT SW1 in the TX mode. Measured and simulated (**c**) IL and isolation and (**d**) S_{11} and S_{33} of SPDT SW1 in the RX mode.

Figure 8d shows the measured and simulated S_{11} and S_{33} of SPDT SW1 in the RX mode. SPDT SW1 achieves a measured $S_{11,min}$ of −14.7 dB at 30.9 GHz and an S_{11} better than −10 dB for 20.7–50 GHz, corresponding to an f_{10dB} of 29.3 GHz. This result is consistent with the simulated one, i.e., an $S_{11,min}$ of −12.7 dB at 36.8 GHz and an f_{10dB} of 17.7 GHz (29.1–46.8 GHz). Moreover, SPDT SW1 achieves a measured minimum S_{33} ($S_{33,min}$) of −30.4 dB at 29 GHz and an S_{33} better than −10 dB for 18.1–44.9 GHz, equivalent to f_{10dB} of 26.8 GHz. This result is consistent with the simulated one, i.e., an $S_{33,min}$ of −31.1 dB at 32.4 GHz and an f_{10dB} of 25.6 GHz (20.9–46.5 GHz).

Figure 9a shows the measured and simulated power gain S_{12} (i.e., $P_{out}-P_{in}$ in dBm) against the input power (P_{in}) characteristics of SPDT SW1 at 28 GHz in the TX mode. That is, DTMOS-R M_1 and M_2 (controlled by V_{sw1}) are in the off-state and M_3 (controlled by V_{sw2}) is in the on-state. SPDT SW1 achieves a measured S_{12} of −0.67 dB at a low P_{in} of 0 dBm and an S_{12} of −1.67 dB at a high P_{in} of 28.5 dBm. The corresponding P_{1dB} is 28.5 dBm. This result is consistent with the simulated one, i.e., an S_{12} of −0.52 dB at a low P_{in} of 0 dBm and an S_{12} of −1.52 dB at a high P_{in} of 30.6 dBm, corresponding to simulated P_{1dB} of 30.6 dBm. The decent P_{1dB} performance of SPDT SW1 in the TX mode is mainly attributed to the novel SPDT switch topology and the adoption of DTMOS-R switch transistors. This can be explained in more detail as follows. In contrast to the traditional common-source (CS) switch transistors using a V_{sw1}/ V_{sw2} of 0/V_{DD} and a body voltage of 0 V, DTMOS-R M_1 and M_2 achieve a better off-states due to higher off-state channel/substrate resistance ($R_{off,ch}/R_{off,sub}$) because of a higher threshold voltage (V_{th}) and the suppression of substrate leakage (I_B). Moreover, DTMOS-R M_3 achieves a better on-state due to lower on-state channel/substrate resistance ($R_{on,ch}/R_{on,sub}$) because of a lower V_{th}, i.e., a higher over-drive voltage V_{ov} (=$V_{gs}-V_{th}$). In other words, a higher P_{in} (with a more negative peak voltage) is required to conduct the off-state shunt/series M_1/M_2. This leads to a high P_{1dB} in the TX mode. Moreover, the high P_{1dB} of 28.5 dBm is partly due to the prominent TX-to-RX isolation of 62.3 dB (see Figure 8a).

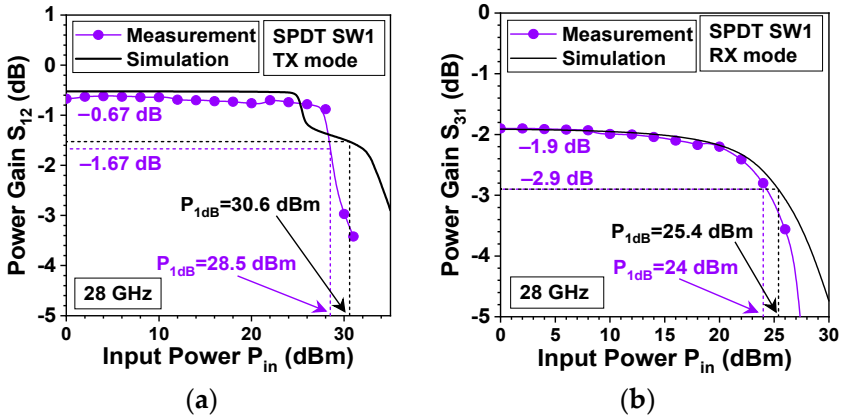

Figure 9. Measured and simulated P_{1dB} in (**a**) the TX mode, and (**b**) the RX mode of SPDT SW1 at 28 GHz.

Figure 9b shows the measured and simulated power gain S_{31} against P_{in} the characteristics of SPDT SW1 at 28 GHz in the RX mode. That is, DTMOS-R M_1 and M_2 are in the on-state and M_3 is in the off-state. SPDT SW1 achieves a measured S_{31} of −1.9 dB at a low P_{in} of 0 dBm and −2.9 dB at a high P_{in} of 24 dBm. The corresponding P_{1dB} is 24 dBm. This result is consistent with the simulated one, i.e., an S_{12} of −1.91 dB at a low P_{in} of 0 dBm and an S_{12} of −2.91 dB at a high P_{in} of 25.4 dBm, corresponding to a simulated P_{1dB} of 25.4 dBm. This decent P_{1dB} performance of the SPDT switch in the RX mode is also attributed to the novel SPDT switch topology and the adoption of DTMOS-R switch transistors.

Figure 10a shows the measured fundamental (P_{out}) and third-order intermodulation output power (IM3) versus the P_{in} characteristics of SPDT SW1 in the TX mode at 28 GHz. SPDT SW1 achieves an excellent IIP3 of 38.5 dBm. Figure 10b shows the measured P_{1dB} and IIP3 versus the frequency characteristics of SPDT SW1 over the 24.25–29.5 GHz (N257/N258) 5G mm wave band. SPDT SW1 achieves a P_{1dB} of 28–29 dBm and an IIP3 of 38.1–39 dBm in the TX mode, and a P_{1dB} of 24–24.8 dBm and an IIP3 of 34.1–35 dBm in the RX mode. This result is reasonable since it is consistent with the theoretical analysis, i.e., IIP3 is about 9.6 dBm larger than P_{1dB} [17].

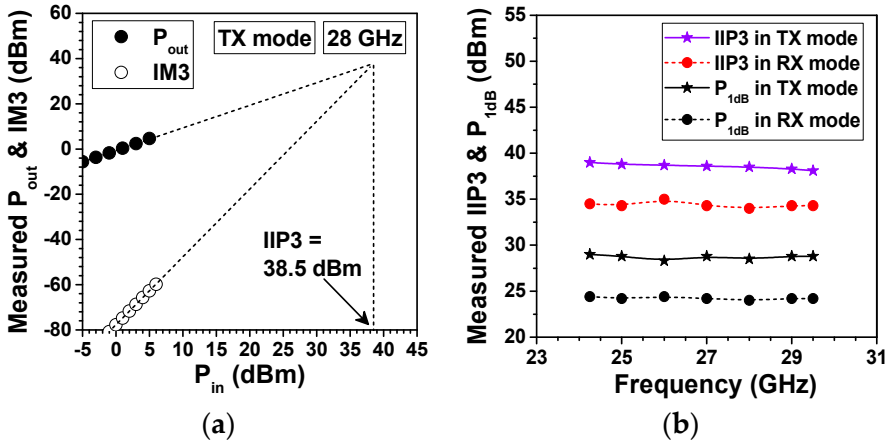

Figure 10. (**a**) Measured P_{out} and IM3 versus P_{in} characteristics of SPDT SW1 in the TX mode at 28 GHz. (**b**) Measured P_{1dB} and IIP3 versus frequency characteristics of SPDT SW1 in the TX and RX modes.

4. Results and Discussion of SPDT SW2

Figure 11a shows the measured and simulated IL (i.e., $|S_{12}|$) and isolation (i.e., $|S_{32}|$) of SPDT SW2 in the TX mode. SPDT SW2 achieves a measured IL_{min} of 0.74 dB at 20.2 GHz and an IL better than 1.2 dB for 13.6–30.5 GHz, corresponding to a bandwidth of 16.9 GHz.

This result is close to the simulated one, i.e., an IL_{min} of 0.7 dB at 21.5 GHz and an IL lower than 1.2 dB for 12.4–38.1 GHz, corresponding to a bandwidth of 25.7 GHz. The decent IL is attributed to the low-loss of the equivalent λ/4-TL, the good TX-to-RX isolation, and the high impedance of the off-state DTMOS-R M_1. Moreover, SPDT SW2 achieves a measured $|S_{32}|_{max}$ of 59.2 dB at 30 GHz and isolation of 25.2–59.2 dB for 13.6–30.5 GHz. This result is close to the simulated one, i.e., an $|S_{32}|_{max}$ of 62.4 dB at 26.9 GHz and isolation of 29.7–62.4 dB for 13.6–30.5 GHz. Figure 11b shows the measured and simulated S_{11} and S_{22} of SPDT SW2 in the TX mode. SPDT SW2 achieves a measured $S_{11,min}$ of −15.9 dB at 20.2 GHz and an S_{11} better than −10 dB for 12.6–37.3 GHz, equivalent to an f_{10dB} of 24.7 GHz. This result is close to the simulated one, i.e., an $S_{11,min}$ of −26.4 dB at 24.7 GHz and an f_{10dB} larger than 38.4 GHz (11.6–50 GHz). Moreover, SPDT SW2 achieves a measured $S_{22,min}$ of −30.7 dB at 20.7 GHz and an S_{22} better than −10 dB from 10.9 GHz to larger than 50 GHz, equivalent to an f_{10dB} larger than 39.1 GHz. This result is close to the simulated one, i.e., an $S_{22,min}$ of −28.2 dB at 46.4 GHz and an f_{10dB} larger than 39 GHz (11–50 GHz).

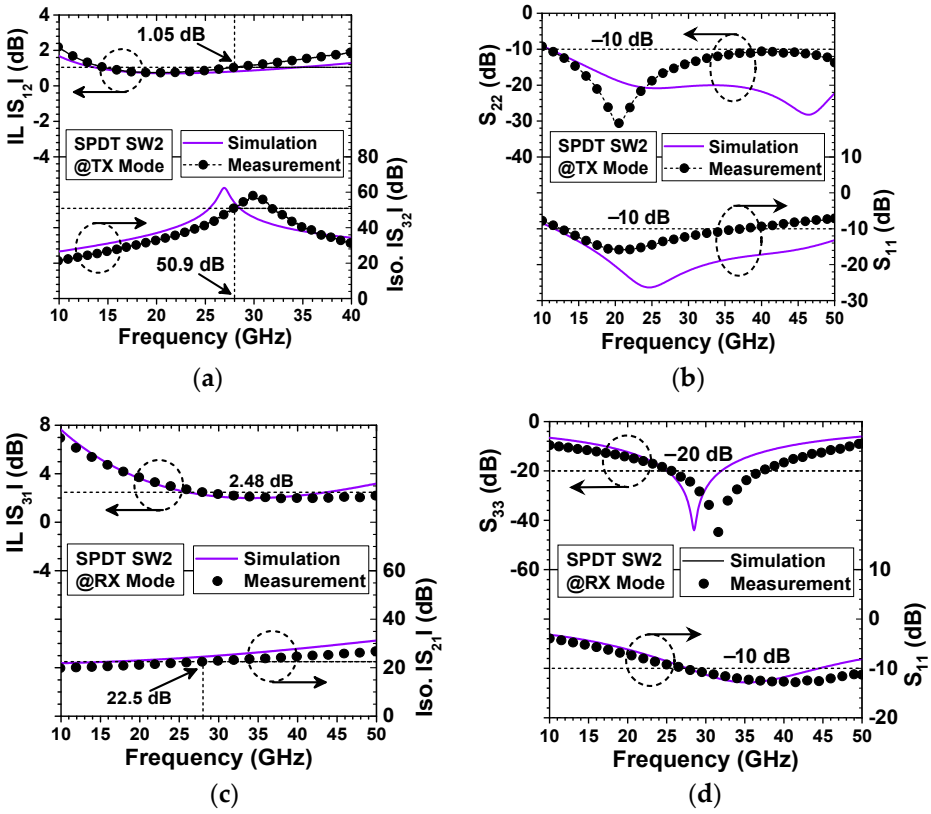

Figure 11. Measured and simulated (**a**) IL and isolation and (**b**) S_{11} and S_{22} of SPDT SW2 in the TX mode. Measured and simulated (**c**) IL and isolation and (**d**) S_{11} and S_{33} of SPDT SW2 in the RX mode.

Figure 11c shows the measured and simulated IL (i.e., $|S_{31}|$) and isolation (i.e., $|S_{21}|$) of SPDT SW2 in the RX mode. SPDT SW2 achieves a measured IL_{min} of 1.93 dB at 40.2 GHz and an IL of 1.93–2.5 dB from 27.7 GHz to over 50 GHz. This result is close to the simulated one, i.e., an IL_{min} of 1.99 dB at 34.2 GHz and an IL of 1.99–2.5 dB for 25.9–43.9 GHz. Moreover, SPDT SW2 achieves a measured isolation of 17.5–21.8 dB for 27.7–50 GHz. This result is close to the simulated one, i.e., isolation of 19.5–26.2 dB for 27.7–50 GHz. Figure 11d shows the measured and simulated S_{11} and S_{33} of SPDT SW2 in the RX mode. SPDT SW2 achieves a measured $S_{11,min}$ of −13 dB at 41.4 GHz and an S_{11} better than −10 dB from 27 GHz to over 50 GHz, corresponding to an f_{10dB} larger than 23 GHz. This result is consistent with the simulated one, i.e., an $S_{11,min}$ of −12.9 dB at 35.3 GHz and an f_{10dB} of 16.9 GHz (27.6–44.5 GHz). Moreover, SPDT SW2 achieves a measured $S_{33,min}$ of −49.2 dB at 31.4 GHz, and an S_{33} better than −10 dB for 11–48.5 GHz, equivalent to an f_{10dB} of

37.5 GHz. This result is consistent with the simulated one, i.e., an $S_{33,min}$ of −44.1 dB at 28.5 GHz and an f_{10dB} of 23.3 GHz (17.1–40.4 GHz).

Figure 12a shows the measured and simulated power gain S_{12} against the P_{in} characteristics of SPDT SW2 at 28 GHz in the TX mode. That is, DTMOS-R M_1 and M_2 are in the off-state and M_3 is in the on-state. SPDT SW2 achieves a measured S_{12} of −1.05 dB at a low P_{in} of 0 dBm and an S_{12} of −2.05 dB at a high P_{in} of 24.6 dBm. The corresponding P_{1dB} is 24.6 dBm. This result is consistent with the simulated one, i.e., an S_{12} of −0.81 dB at a low P_{in} of 0 dBm and an S_{12} of −1.81 dB at a high P_{in} of 24.3 dBm, corresponding to a simulated P_{1dB} of 24.3 dBm. The decent P_{1dB} performance of SPDT SW2 in the TX mode is mainly attributed to the novel SPDT switch topology and the adoption of DTMOS-R switch transistors. This can be explained in more detail as follows. In contrast to the traditional CS switch transistors using a V_{sw1}/V_{sw2} of $0/V_{DD}$ and a body voltage of 0 V, DTMOS-R M_1 and M_2 achieve a better off-state due to higher off-state channel/substrate resistance ($R_{off,ch}/R_{off,sub}$) because of a higher V_{th}, a lower overdrive voltage V_{ov}, and the suppression of I_B. Moreover, DTMOS-R M_3 achieves a better on-state due to lower on-state channel/substrate resistance ($R_{on,ch}/R_{on,sub}$) because of a lower V_{th} and a higher over-drive voltage V_{ov}. In other words, a higher P_{in} is required to conduct the off-state shunt/series M_1/M_2. This leads to a high P_{1dB} in the TX mode. Moreover, the high P_{1dB} of 24.6 dBm is partly due to the prominent (TX-to-RX) isolation of 59.2 dB (see Figure 11a).

Figure 12b shows the measured power gain S_{31} against the P_{in} characteristics of SPDT SW2 at 28 GHz in the RX mode. That is, DTMOS-R M_1 and M_2 (controlled by V_{sw1}) are in the on-state, and M_3 (controlled by V_{sw2}) is in the off-state. The measured result is consistent with the simulated one. SPDT SW2 achieves a measured S_{31} of −2.48 dB at a low P_{in} of 0 dBm, and −3.48 dB at a high P_{in} of 20.2 dBm. The corresponding P_{1dB} is 20.2 dBm. This decent P_{1dB} performance of the SPDT switch in the RX mode is also attributed to the novel SPDT switch topology and the adoption of DTMOS-R switch transistors.

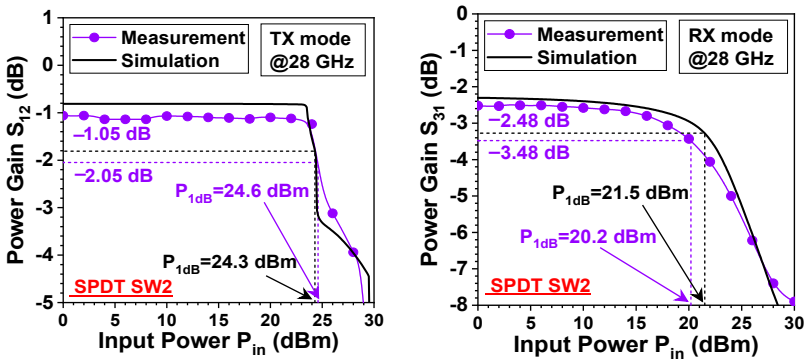

Figure 12. Measured and simulated P_{1dB} of SPDT SW2 in (**a**) the TX mode and (**b**) the RX mode.

A figure-of-merit (FOM) suitable for the evaluation of a wideband, low-IL, high-linearity, and decent-isolation SPDT switch can be defined as follows.

$$FOM[GHz \cdot mW] = \frac{BW[GHz] \cdot Isolation[1] \cdot P_{1dB}[mW]}{IL[1]} \quad (12)$$

in which IL [1] is the insertion loss in magnitude, BW[GHz] is the bandwidth in GHz, Isolation [1] is the isolation in magnitude, and P_{1dB} is the input 1 dB compression point in mW. Table 1 is a summary of SPDT SW1 and SW2, and recently reported state-of-the-art SPDT switches with similar operation frequency using similar CMOS technologies. The operation bandwidth (BW) is a function of the specification of the maximum allowed IL (IL_{max}). As shown, SPDT SW1 achieves BW values of 13.3 and 21.1 GHz for IL_{max} of 2.1 and 2.5 dB, respectively. SPDT SW2 achieves a BW of 22.3 GHz for IL_{max} 2.5 dB. For the same IL_{max} of 2.5 dB, for a fair comparison, SPDT SW1 achieves a BW of 21.1 GHz, close to

that (22.3 GHz) of SPDT SW2. Overall, SPDT SW1 occupies a medium area, and achieves decent reflection coefficients, IL, isolation, bandwidth, and P_{1dB}, and excellent FOM in the RX mode and the best FOM in the TX mode.

Table 1. Summary of the CMOS SPDT SW1 and SW2, and recent reported state-of-the-art CMOS SPDT switches with similar operation frequency.

	Topology	S_{11} (dB)	S_{22}/S_{33} (dB)	IL/IL_{min} (dB)	Isolation (dB)	BW (GHz)	P_{1dB} (dBm)	FOM (GHz.mW)	Area (mm^2)	CMOS Technology
SW1-TX	Asymmetrical and equal λ/4 TL & DTMOS-R	−12.6~−21.9	−12.8~−30.6	<1/0.58	25.6–62.3	17.9 (17–34.9)	28.5	1.55×10^7	0.068	90 nm
SW1-RX		−12.8~−14.7 −12.4~−14.7	−13.5~−30.4 −10.6~−30.4	<2.1/1.83 <2.5/1.83	24.5–27 24.5–27.7	13.3 (25–38.3) 21.1 (22–43.1)	24	1.04×10^5		
SW2-TX	Asymmetrical and equal λ/4 TL and DTMOS-R	−11~−15.9	−13.4~−30.7	<1.2/0.74	25.2–59.2	16.9 (13.6–30.5)	24.6	4.08×10^6	0.068	0.18 µm
SW2-RX		−10.2~−13	−8.9~−49.2	<2.5/1.93	22.5–26.8	22.3 (27.7–50)	20.2	4.09×10^4		
[3]	Symmetrical and MN	<−7.2	<−6.9	<4.3/3.6	>25.7	38 (0–38)	25.6	1.76×10^5	0.392	0.18 µm
[4]	Symmetrical and Shunt-L	<−20	NA	<1.5/NA	18.2	13.5 (25–39.5)	12.55	1.66×10^3	0.009	65 nm
[5]-TX	Asymmetrical and MN	<−14.2	<−14.2	<1.1/0.96	>27	5 (25–30)	31.8	1.52×10^5	0.043	65 nm
[5]-RX		<−15.9	<−15.9	<1.16/0.74	>16.4		5.2	1.01×10^2		
[6]-TX	Asymmetrical and MN and Stacked-MOS	<−15.7	NA	<2.1/1.8	>28.1	5 (20–25)	32.5	1.84×10^5	0.03	65 nm
[6]-RX		<−16	NA	<2/1.5	>22.5		4.7	1.66×10^2		
[7]	Symmetrical and λ/4-L	<−8	NA	<2/NA	>25	20 (50–70)	13.5	6.33×10^3	0.27	90 nm
[8]	Asymmetrical	<−10	NA	<3.4/NA	22	24 GHz only	28.7	1.51×10^5	0.018	90 nm
[9]	Resonance Network	<−10	<−10	<1.3/1	>50	10 (9–19)	5	8.91×10^3	0.034	65 nm
[10]	λ/4 Spiral Inductor	<−10	<−10	<1.5/1.3	>23.7	15 (20–35)	10.8	2.34×10^3	0.028	65 nm
[11]	Center-Tapped L	<−10	<−10	<1.7/1.7	>22	9 (26–35)	9	7.4×10^2	0.03	65 nm
[12]	Traveling Wave	<−10	<−10	<2.7/2.7	>34	60 (DC-60)	NA	NA	0.2	45 nm SOI
[13]	N/PMOS w/i Canceler	<−10	<−10	<1.6	>35	16 (24–40)	19.1	6.08×10^4	0.016	65 nm

5. Conclusions

We propose an asymmetrical CMOS SPDT switch with a low IL, good isolation, and high linearity for a 28 GHz 5G NR. The SPDT switch is designed and implemented in a 90 nm CMOS process with a top metal thickness (TMT) of 3.4 µm (SPDT SW1) and in a 0.18 µm CMOS process with a TMT of 2.34 µm (SPDT SW2). Compared with SPDT SW2, SPDT SW1 exhibits better overall performance (such as a 0.1–0.4 dB enhancement in IL) mainly due to a thicker TMT (i.e., lower transmission loss). The TX path is a π-network consisting of a parallel DTMOS-R M_1, a series λ/8 TL, and a parallel capacitance, C_{ant}, for a low IL (0.58–1 dB over 17–34.9 GHz for SPDT SW1) and a high P_{1dB} (28.5 dBm at 28 GHz for SPDT SW1) in the TX mode and good isolation in the RX mode. The RX path consists of a series impedance (of parallel L_1 and DTMOS-R M_2) and a parallel DTMOS-R M_3 for a high P_{1dB} (24 dBm at 28 GHz for SPDT SW1) in the RX mode and decent isolation (25.6–62.3 dB over 17–34.9 GHz for SPDT SW1) in the TX mode. The prominent performance of SPDT SW1 indicates that it is suitable for a 28 GHz 5G NR.

Author Contributions: Conceptualization, Y.-S.L. and J.-F.C.; methodology, Y.-S.L.; software, C.-Y.H.; validation, Y.-S.L., C.-T.H., C.-Y.H. and J.-F.C.; formal analysis, Y.-S.L.; investigation, Y.-S.L., C.-T.H., C.-Y.H., N.-W.T. and Y.-H.C.; resources, Y.-S.L.; data curation, Y.-S.L.; writing—original draft preparation, Y.-S.L.; writing—review and editing, Y.-S.L.; visualization, Y.-S.L.; supervision, Y.-S.L.; project administration, Y.-S.L.; funding acquisition, Y.-S.L. All authors have read and agreed to the published version of the manuscript.

Funding: This research was funded by the National Science and Technology Council (NSTC) of Taiwan, grant number MOST111-2221-E-260-017.

Acknowledgments: The authors are very grateful for the support from the Taiwan Semiconductor Research Institute (TSRI) for chip fabrication and measurements.

Conflicts of Interest: The authors declare no conflict of interest.

References

1. Kibaroglu, K.; Sayginer, M.; Rebeiz, G.M. A low-cost scalable 32-element 28-GHz phased array transceiver for 5G communication links based on a 2 × 2 beamformer flip-chip unit cell. *IEEE J. Solid State Circuits* **2018**, *53*, 1260–1274. [CrossRef]
2. Sadhu, B.; Tousi, Y.; Hallin, J.; Sahl, S.; Reynolds, S.K.; Renström, Ö.; Sjögren, K.; Haapalahti, O.; Mazor, N.; Bokinge, B.; et al. A 28-GHz 32-element TRX phased-array IC with concurrent dual-polarized operation and orthogonal phase and gain control for 5G communications. *IEEE J. Solid State Circuits* **2017**, *52*, 3373–3391. [CrossRef]
3. Chang, J.F.; Lin, Y.S. High linearity DC-38 GHz CMOS SPDT switch. *Appl. Sci.* **2021**, *11*, 9402. [CrossRef]

4. Lee, W.; Hong, S. Low-loss and small-size 28 GHz CMOS SPDT switches using switched inductor. In Proceedings of the 2018 IEEE Radio Frequency Integrated Circuits Symposium (RFIC), Philadelphia, PA, USA, 10–12 June 2018; pp. 148–151.
5. Lee, K.H.; Choi, S.; Kim, C.Y. A 25-30-GHz asymmetric SPDT switch for 5G applications in 65-nm triple-well CMOS. *IEEE Microw. Wirel. Compon. Lett.* **2019**, *29*, 391–393. [CrossRef]
6. Kim, T.; Lee, H.D.; Park, B.; Jang, S.; Kong, S.; Park, C. Design of a K-band high-linearity asymmetric SPDT CMOS switch using a stacked transistor. *IEEE Microw. Wirel. Compon. Lett.* **2022**, *32*, 1443–1446. [CrossRef]
7. Uzunkol, M.; Rebeiz, G.M. A low-loss 50-70 GHz SPDT switch in 90 nm CMOS. *IEEE J. Solid State Circuits* **2010**, *45*, 2003–2007. [CrossRef]
8. Park, P.; Shin, D.H.; Yue, C.P. High-Linearity CMOS T/R switch design above 20 GHz using asymmetrical topology and AC-floating bias. *IEEE Trans. Microw. Theory Techn.* **2009**, *57*, 948–956. [CrossRef]
9. Fu, X.; Wang, Y.; Li, Z.; Shirane, A.; Okada, K. A 68-dB Isolation 1.0-dB Loss Compact CMOS SPDT RF Switch Utilizing Switched Resonance Network. In Proceedings of the 2020 IEEE/MTT-S International Microwave Symposium (IMS), Los Angeles, CA, USA, 4–6 August 2020; pp. 1315–1318.
10. Meng, X.; Yue, C.P. Compact millimeter-wave SPDT switches and Wilkinson power combiners implemented by LC-based spiral transmission lines. *IEEE Trans. Microw. Theory Tech.* **2021**, *69*, 1305–1315. [CrossRef]
11. Pan, Y.; Li, Z. A Ka-band SPDT switch utilizing center-tapped inductor resonance network. In Proceedings of the 2022 International Conference on Microwave and Millimeter Wave Technology (ICMMT), Harbin, China, 12–15 August 2022; pp. 1–3.
12. Hao, W.; Di, M.; Pan, Z.; Li, X.; Miao, R.; Cahoon, N.; Wang, A. A 60 GHz traveling-wave SPDT switch with HBM and CDM ESD protection in 45 nm SOI CMOS. In Proceedings of the 2022 IEEE 16th International Conference on Solid-State & Integrated Circuit Technology (ICSICT), Nangjing, China, 25–28 October 2022; pp. 1–4.
13. Park, J.; Lee, S.; Hong, S. A 24–40 GHz differential SPDT switch with an NMOS and PMOS alternating structure and leakage-canceling capacitors. *IEEE Trans. Circuits Syst. II Express Briefs* **2023**, *70*, 86–90. [CrossRef]
14. Yeh, M.C.; Tsai, Z.M.; Liu, R.C.; Lin, K.Y.; Chang, Y.T.; Wang, H. Design and analysis for a miniature CMOS SPDT switch using body- floating technique to improve power performance. *IEEE Trans. Microw. Theory Tech.* **2006**, *54*, 31–39.
15. Chang, J.F.; Lin, Y.S. A 13.7-mW 21-29 GHz CMOS LNA with 21.6 dB Gain and 2.74 dB NF for 28 GHz 5G Systems. *IEEE Microw. Wirel. Compon. Lett.* **2022**, *32*, 137–140. [CrossRef]
16. Park, J.; Mercier, P.P. A sub-10-pJ/bit 5-Mb/s magnetic human body communication transceiver. *IEEE J. Solid State Circuits* **2019**, *54*, 3031–3042. [CrossRef]
17. Pozar, D.M. *Microwave Engineering*, 4th ed.; John Wiley & Sons, Inc.: Hobokan, NJ, USA, 2012.
18. King, W.M. Minimizing EMI and noise coupling among circuit regions in circuit boards. In Proceedings of the IEEE International Symposium on Electromagnetic Compatibility (EMC), Hamburg, Germany, 8–12 September 2008; Available online: https://ewh.ieee.org/r6/scv/emc/archive/2008meetings.html (accessed on 9 December 2008).
19. NXP Semiconductors. *High Speed Layout Design Guidelines*; NXP Semiconductors: Eindhoven, The Netherlands, 2006; Available online: https://www.nxp.com/docs/en/application-note/AN2536.pdf (accessed on 1 April 2006).
20. Intel Corporation. *High-Speed Board Layout Guidelines*; Intel Corporation: Santa Clara, CA, USA, 2009; Available online: https://www.intel.com/content/dam/www/programmable/us/en/pdfs/literature/an/an224.pdf (accessed on 1 August 2009).
21. Lin, Y.S.; Lan, K.S. Realization of a compact and high-performance power divider using parallel RC isolation network. *IEEE Trans. Circuits Syst. II Express Briefs* **2021**, *68*, 1368–1372. [CrossRef]