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A Capacitorless LDO Regulator with Fast Feedback Loop and Damping-Factor-Control Frequency Compensation

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Abstract: A fast feedback loop (FFL) based on comparators is proposed in this paper. The FFL improves the transient response characteristics of the output-capacitorless low-dropout (OCL-LDO) regulator. When the load current switches between 1 mA and 100 mA with 1 µs edge time, the overshoot and undershoot are 33 mV and 37 mV, respectively, and recovery time is 1.2 µs and 1.6 µs, respectively. A damping-factor-control (DFC) frequency compensation circuit is used to ensure the stability of the OCL-LDO, and the simulation results show that the phase margin exceeds 50 degree in the entire load variation range. This design is based on 180 nm process, and the area of the chip is 0.068 mm^2 (without pads). A band-gap reference circuit is also designed in this work; its output voltage is 1.2 V and its temperature coefficient is 7.96 ppm/°C. The input voltage range of the proposed OCL-LDO is 2.5 V to 5 V with a linear regulation rate of 0.128 mV/V and a load regulation rate of 0.0017 mV/mA. In addition, the load range of the proposed OCL-LDO is 0 mA to 100 mA, and the minimum required external capacitance is 0 F. The power supply rejection ratio (PSRR) is −46 dB @ 1 kHz.

Keywords: transient response; OCL-LDO; damping-factor control; fast feedback loop

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1. Introduction

Low-dropout (LDO) voltage regulators play an important role in system-on-chip (SoC) design, due to its wide output voltage, low noise, high power supply rejection ratio, and fast load response [1–3]. In the traditional LDO structure, an external output off-chip capacitor (C_L) usually in the µF range is needed to stabilize the output voltage. Usually, C_L requires extra pins, and it is not easy to integrate with other circuit modules due to the large on-chip area required. Thus, it is difficult to meet the current high-integration design requirements [4–6]. OCL-LDO has attracted more and more attention because it does not require additional large capacitors and is easy to integrate with other circuit modules.

Because OCL-LDO cannot compensate the loop through the zero point introduced by external ESR resistor and capacitor, it is necessary to design a special frequency compensation module. OCL-LDO has many frequency compensation methods, some commonly used methods are introduced in references [7–12]. The damping-factor-control (DFC) method redistributes the zero and pole points of the system by adding a damping control unit in the circuit. This method is effective for circuits with large capacitance nodes in the system, and can also improve the transient characteristics of the circuit [13–16]. In addition, the transient enhancement loop is very important for the OCL-LDO because of its small load capacitance. Reference [11] proposed a weighted current feedback (WCF) technique that can improve gain and loop stability. When the current changes from 0 to 50 mA, its recovery time is 250 ns, but it requires a capacitor of 0.47 µF. Reference [15] proposed an LDO with an input range of 8 V to 24 V. Through DFC technology, it can maintain the stability of the loop without external large capacitors. However, its overshoot voltage is 118.8 mV, and its undershoot voltage is about 140 mV.

This paper is organized as follows. Section 2 shows the main circuit structure. Section 3 analyzes the frequency compensation. Section 4 summarizes the simulation results. Section 5 is the conclusion of this paper.

2. Circuit Implementation

In this work, an OCL-LDO with fast feedback loop is proposed. Figure 1 shows a simplified block diagram of the proposed OCL-LDO. The OCL-LDO includes a fast feedback loop [17–19], a reference circuit, an error amplifier for comparing the difference between the feedback and reference voltage, and a DFC provides frequency compensation [20–22]. A detailed circuit of the error amplifier and DFC is shown in Figure 2.

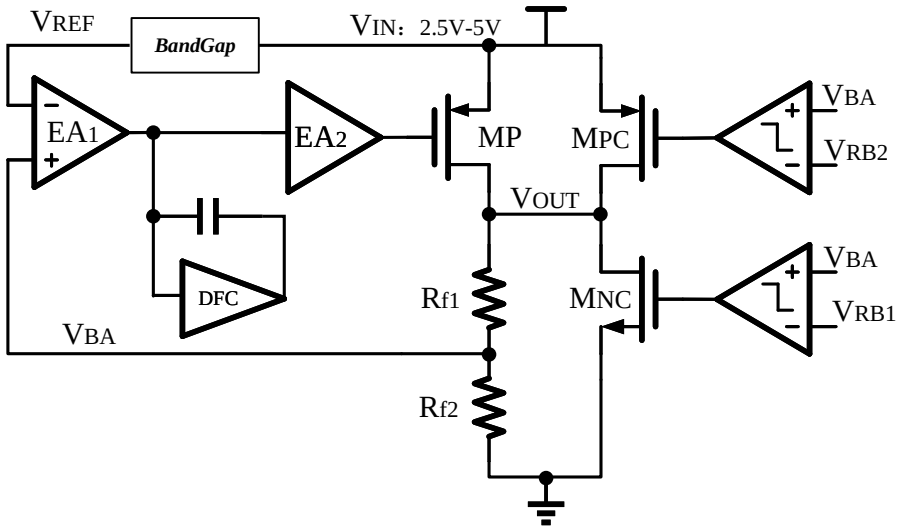

Figure 1. The proposed OCL-LDO regulator.

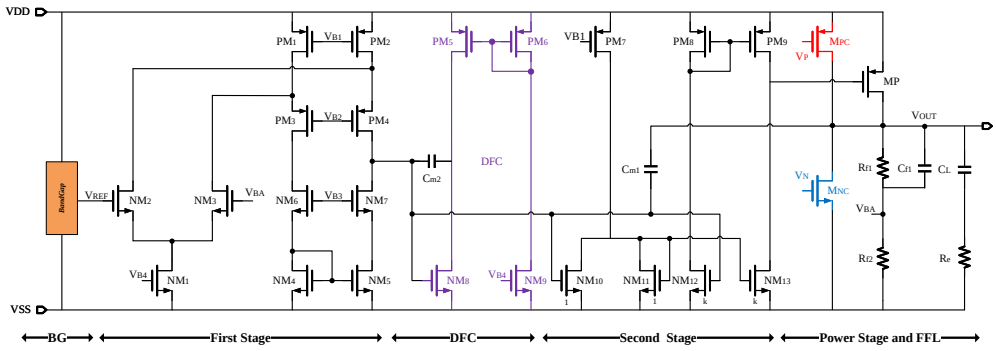

Figure 2. Proposed OCL-LDO with DFC.

2.1. Reference Circuit

As shown in Figure 3, the reference circuit includes start up, band gap, and reference. The band-gap circuit is implemented with a conventional self-biasing circuit [23–25]. EN is the enable signal, which is mainly used to control the opening and closing of the band-gap reference circuit. When EN is VSS, the PM_5 tube is turned on and the NM_2 tube is turned off. The voltage of V_2 is pulled up to VDD, and then the entire band-gap reference circuit is turned off. When the EN signal is VDD, the PM_5 tube is turned off and the NM_2 tube is turned on. The Reference circuit operates normally. A start-up module is also added to the design of the reference circuit, which can accelerate the band-gap reference module to enter the normal working state and prevent the band-gap reference circuit from entering a deadlock state. When the power supply voltage is turned on, the voltage of V_{REF} is low. Because V_{REF} is low, the PM_4 tube is turned on and the NM_1 tube is turned off. The gate

voltage V_1 of the NM_3 tube is pulled up by the PM_4 tube, and then the NM_3 tube is turned on. Because the EN signal is high at this time, the NM_2 tube is turned on. So, voltage V_2 is pulled low and the band-gap reference circuit starts working. When the output of the band-gap reference circuit is stable, the output voltage V_{REF} is about 1.2 V. The PM_4 tube is closed and the NM_1 tube is open. Voltage V_1 is pulled low, NM_3 is turned off, and then, the start-up circuit is turned off. Through the above analysis, it can be found that the start-up circuit is only operating at the initial moment. The simulation results of reference circuit are shown in Figure 4. According to the simulation results, it can be determined that the startup time of the entire reference circuit is 7.2 µs.

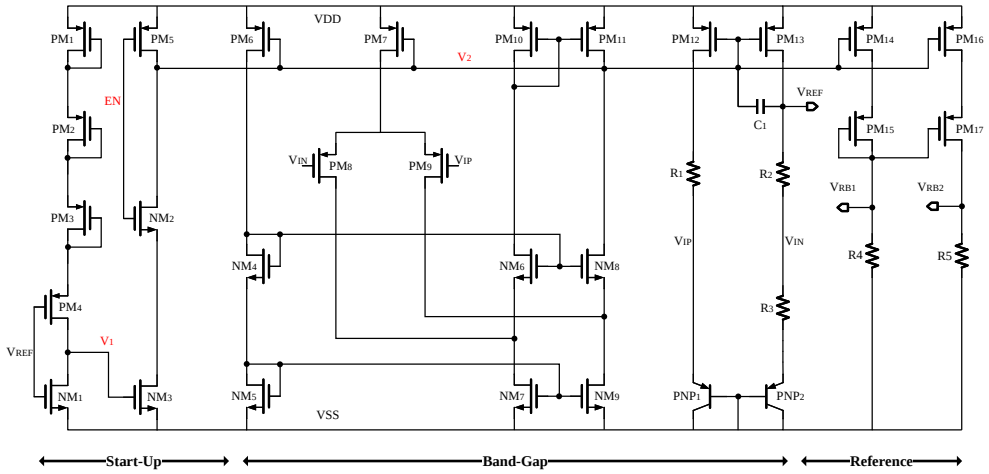

Figure 3. Reference circuit.

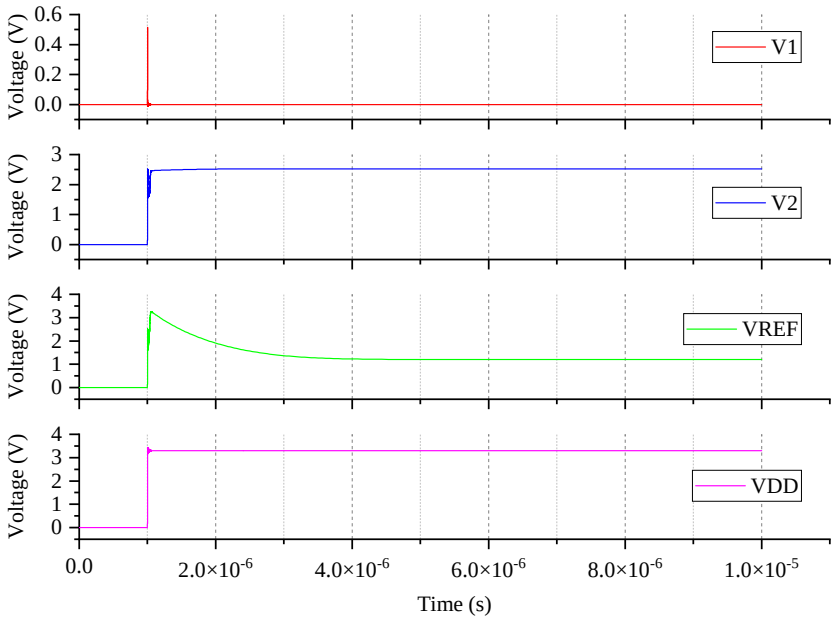

Figure 4. Transient simulation results of the reference circuit.

In order to ensure that the currents of PM_{12} and PM_{13} are consistent, the resistor R1 is added. Figure 5 shows the simulation results of the reference circuit at different temperatures and voltages. According to Figure 5, we can know that the temperature coefficient of the band-gap reference circuit is 7.96 ppm/°C. When the input power supply voltage changes from 2 V to 5 V, the output voltage V_{REF} is 1.204 ± 0.002 V. In order to keep the voltage of V_{RB1} and V_{RB2} constant, R_4 and R_5 need to use resistors with negative temperature coefficients.

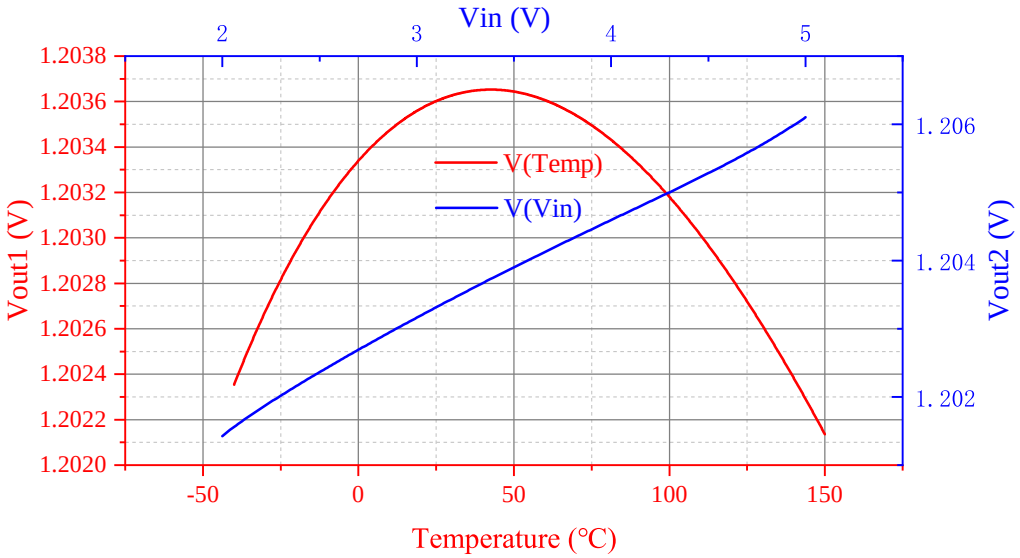

Figure 5. Simulation results of the reference circuit at different temperatures.

Taking into account the deviation made by the craft factory, Figure 6 shows the simulation results of the phase margin and gain at three different process angles where the three process angles are FF (−40 °C), TT (27 °C), and SS (80 °C). According to the simulation results in Figure 6, it can be seen that under the three different process angles, the gain of the reference circuit is about 37 dB and the phase margin is greater than 60 degrees.

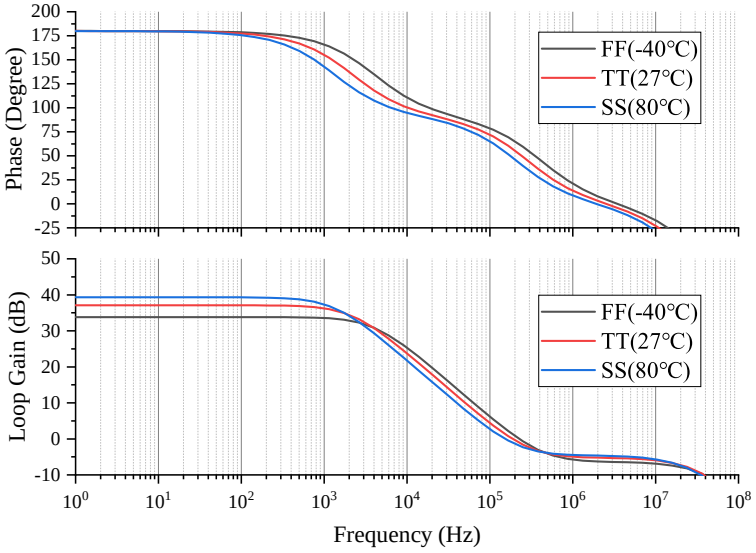

Figure 6. Gain and phase margin of reference circuit under different process angles.

2.2. Error Amplifier and DFC

This OCL-LDO adopts a three-stage structure [26–28]. Figure 2 shows the circuit implementation of the proposed OCL-LDO. In the first stage, a folded cascode structure is used for high gain. In the second stage, the drain terminals of NM_{10} and NM_{11} are connected to the same current source, so the gate voltage of NM_{11} will change opposite to the gate voltage of NM_{10}. This voltage difference is translated into a 2k-times current difference through NM_{12} and NM_{13}. With this design, both the gain of the second stage and the driving ability can be improved. In this work, the value of k is 10, and the total gain of the OCL-LDO is 109 dB. C_{m1}, C_{m2}, C_{f1}, and DFC are used to compensate the phase margin of the loop [29–32].

2.3. Fast Feedback Loop

As shown in Figure 1, when the output voltage is within the normal range, M_{NC} and M_{PC} are turned off. The following is an analysis of the working state of the FFL loop when the load current I_L changes sharply. In Figure 7a, when the output voltage V_{OUT} suddenly becomes low due to the load suddenly becoming high, the comparator controls M_{PC} to turn on. Then, the output voltage V_{OUT} is pulled up through the conduction of the M_{PC} tube. In Figure 7b, when the output voltage V_{OUT} suddenly becomes high due to the load suddenly becoming low, the comparator controls M_{NC} to turn on. Then, the output voltage V_{OUT} is pulled down through the conduction of the M_{NC} tube. In order to improve the comparison speed of the comparator, this work proposes a comparator structure with positive feedback. The detailed circuit is shown in Figure 8. When V_{IP} is greater than V_{IN}, the voltage V_1 will become less than voltage V_2. This also means that the gate voltage of NM_5 is greater than the gate voltage of NM_4, so NM_5 will flow more charge than NM_4.This results in a greater voltage difference between V_1 and V_2 than before. In short, NM_4 and NM_5 form a positive feedback structure. Likewise, PM_3 and PM_7 also form a positive feedback structure. These two positive feedback structures enable the comparator to obtain comparison results quickly. As can be seen from Figure 9, the comparison time of the comparator is 79 ns.

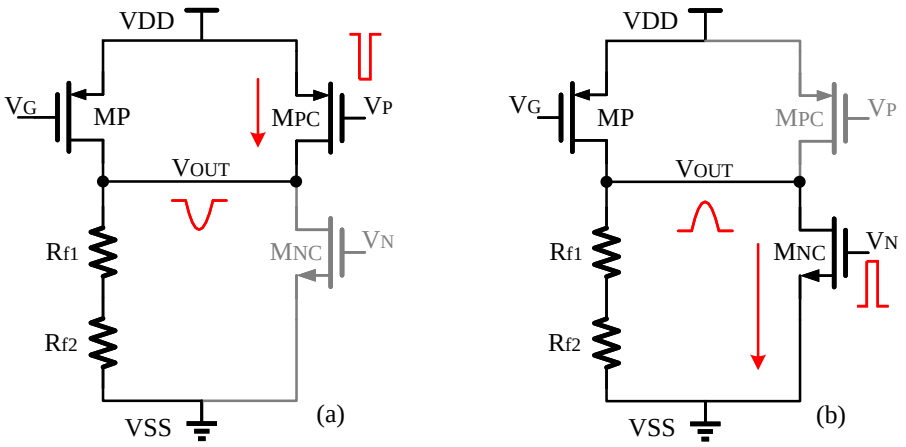

Figure 7. Response of the FFL loop when the output changes. (**a**) Load current I_L suddenly becomes larger, (**b**) Load current I_L suddenly becomes smaller.

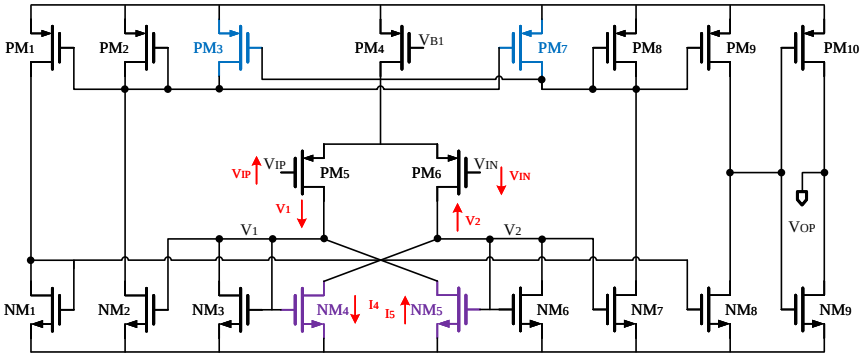

Figure 8. Comparator schematic.

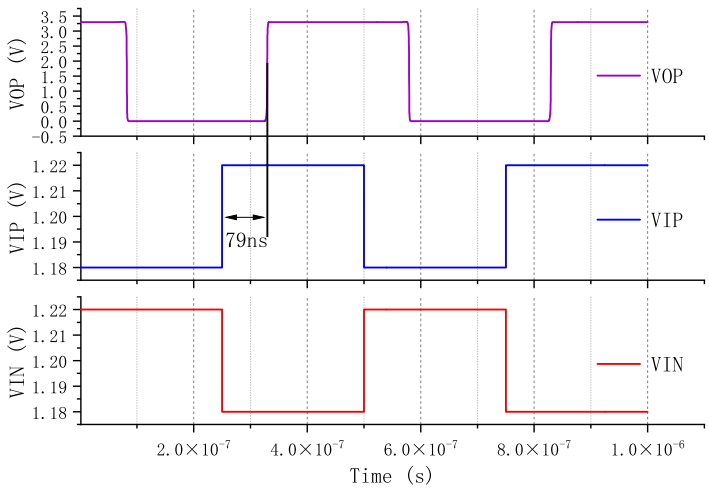

Figure 9. Comparator simulation results.

3. Frequency Compensation

Reference [10] has already mentioned that the DFC method can compensate the phase margin of the OCL-LDO. The DFC module designed in this work requires fewer tubes and reference voltages than reference [10]. The small-signal block diagram of the proposed OCL-LDO main circuit is given in Figure 10. According to the given small signal model, the loop gain of OCL-LDO under different load current and load capacitance is analyzed. When $C_L \neq 0$ and $I_L = 0$, the loop gain is Equation (1). When $C_L \neq 0$ and $I_L \neq 0$, the loop gain is Equation (2). When $C_L = 0$, the loop gain is Equation (3).

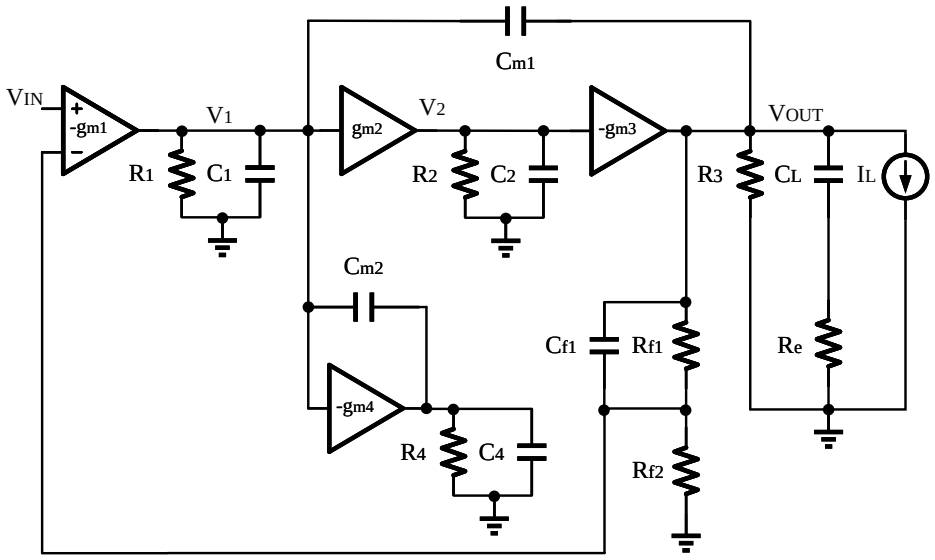

Figure 10. Small-signal model of the proposed OCL-LDO.

$$L_{O(cap)}(s)_{I_L=0} = \frac{L_0(1+\frac{s}{z_e})(1+\frac{s}{z_f})}{(1+\frac{s}{p_1})(1+\frac{C_L C_p g_{m4}}{C_{m1} g_{m2} g_{m3}} s + \frac{C_p C_L}{g_{m2} g_{m3}} s^2)(1+\frac{s}{p_f})} = \frac{L_0(1+\frac{s}{z_e})(1+\frac{s}{z_f})}{(1+\frac{s}{p_1})(1+\frac{2\beta}{p_c} s + (\frac{1}{p_c})^2 s^2)(1+\frac{s}{p_f})} \quad (1)$$

$$L_{O(cap)}(s)_{I_L \neq 0} = \frac{L_0(1+\frac{s}{z_f})}{(1+\frac{s}{p_1})(1+\frac{s}{p_2})(1+\frac{s}{p_f})} \quad (2)$$

$$L_{O(capfree)(s)} = \frac{L_0(1+\frac{s}{z_f})}{(1+\frac{s}{p_1})(1+\frac{s}{p_f})} \quad (3)$$

$$L_O = (\frac{R_{f2}}{R_{f1}+R_{f2}}) g_{m1} g_{m2} g_{m3} R_1 R_2 R_3$$

$$p_1 = \frac{1}{C_{m1} g_{m2} g_{m3} R_1 R_2 R_3}, p_2 = \frac{g_{m2} g_{m3} R_e}{C_p}$$
$$p_f = \frac{1}{C_{f1}(R_{f1}//R_{f2})}, z_f = \frac{1}{C_{f1} R_{f1}}, z_e = \frac{1}{C_L R_e}$$
$$\beta = \frac{1}{2}\sqrt{\frac{C_p C_L}{g_{m2} g_{m3}}}(\frac{g_{m4}}{C_{m1}}), p_c = \sqrt{\frac{g_{m2} g_{m3}}{C_p C_L}}$$

where C_p is the gate capacitance of the power tube; g_{m4} is the transconductance of the DFC; β is the damping factor; p_c is the complex poles; L_O is the loop gain of the proposed OCL-LDO; p_1 is the main pole; p_2 is the pole introduced by the power tube; z_f and p_f are the zero and pole points introduced by the DFC structure, respectively; g_{m1}, g_{m2}, g_{m3} are the transconductances of the LDO; R_1, R_2, and R_3 are the output resistances of the LDO; C_L is the output load capacitance; R_e is the ESR resistance; and C_{m1}, C_{m2}, and C_{f1} are the compensation capacitors.

According to Equation (1) , when $C_L \neq 0$ and $I_L = 0$, z_f complements the main pole, z_e complements a pole of p_c, and the p_f pole is designed outside the unity gain bandwidth. The specific zero-pole distribution is shown in Figure 11a. According to Equation (2), when $C_L \neq 0$ and $I_L \neq 0$, z_f is used to compensate the main pole, and the p_f pole is designed outside the unity gain bandwidth. The specific zero-pole distribution is shown in Figure 11b. According to Equation (3), when $C_L = 0$, z_f is used to compensate the dominant pole, the subdominant pole is p_f, and the composite pole is located outside the unity gain bandwidth. The specific zero-pole distribution is shown in Figure 11c. It can be seen from the above analysis that OCL-LDO can maintain stability under different load capacitances. Figure 12 shows the simulation results when the load capacitance is 0 F. Figure 13 shows the simulation results when the load capacitance is 100 pF. Figure 14 shows the simulation results when the load capacitance is 1 µF. It can be seen that stability is maintained under all load conditions. Furthermore, in all cases, the minimum phase margin of the loop is greater than 50 degrees.

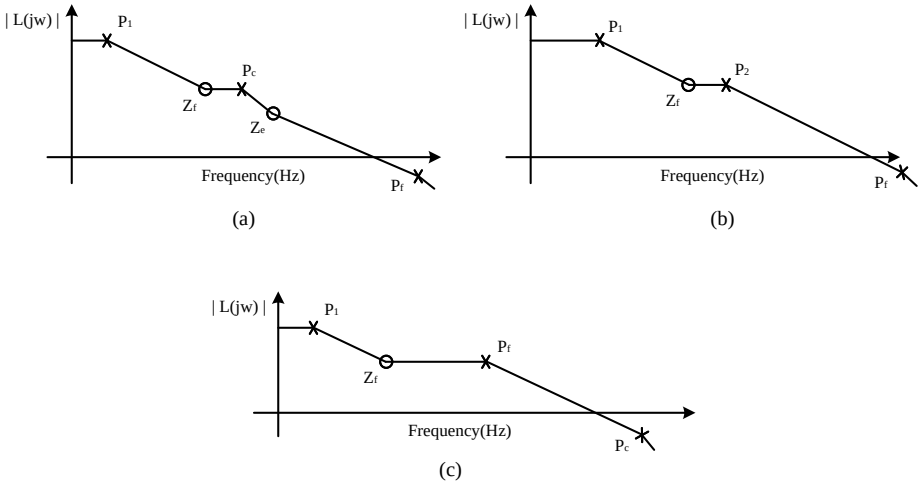

Figure 11. Distribution of zeros and poles at different load capacitances and load currents. (**a**): $C_L \neq 0$ and $I_L = 0$, (**b**): $C_L \neq 0$ and $I_L \neq 0$, (**c**): $C_L = 0$.

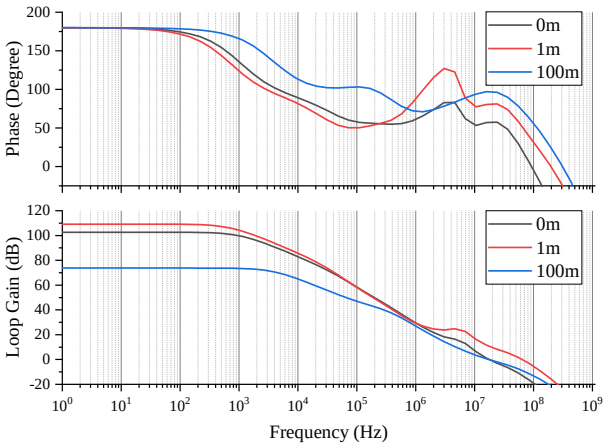

Figure 12. Stability simulation results (C_L = 0 F).

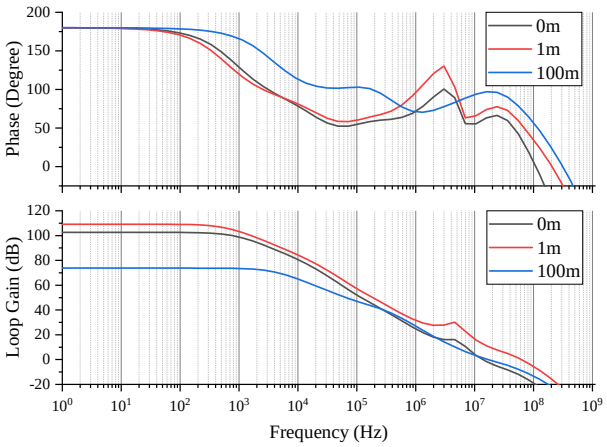

Figure 13. Stability simulation results (C_L = 100 pF).

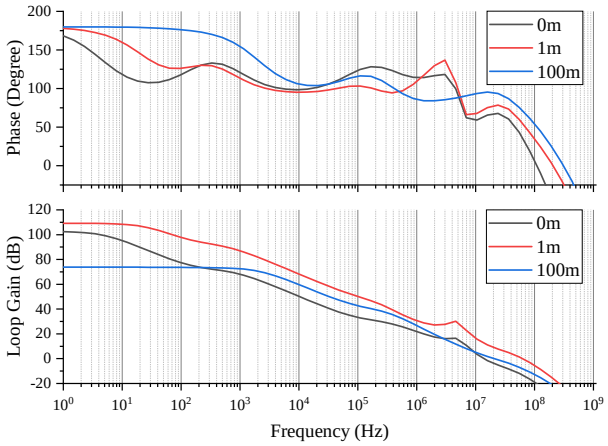

Figure 14. Stability simulation results (C_L = 1 µF).

4. Simulation Results

Figure 15 shows the overall layout of the chip. The proposed OCL-LDO was implemented in 180 nm process with an active area of 216 µm × 315 µm (without pads). The power consumption of the whole chip is 136 µA, and the power consumption of the OCL-LDO core is 76 µA. The peak current efficiency achieved was 99.89%.

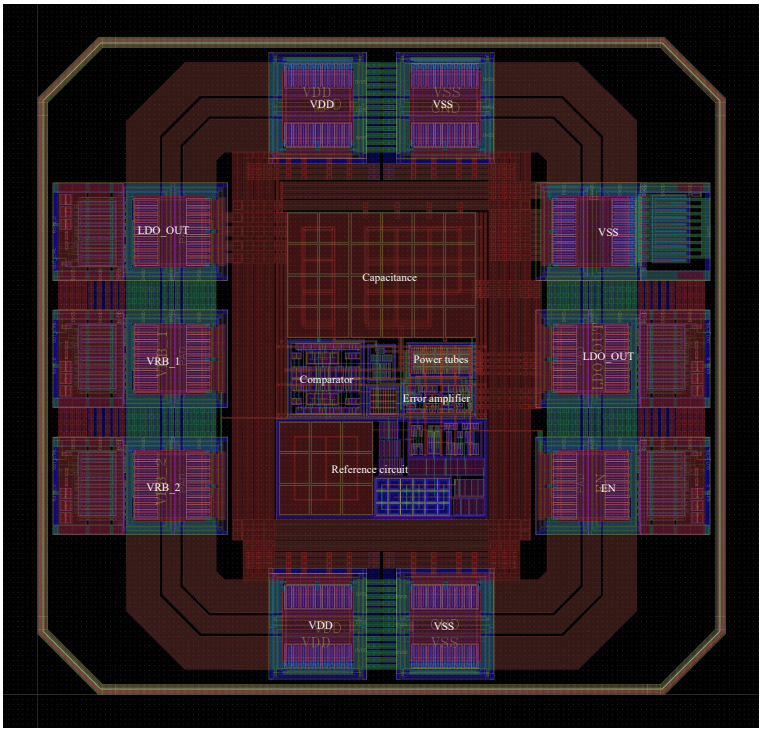

Figure 15. Layout of the chip.

Figure 16 shows the line regulation rate of OCL-LDO. When the load is 1 mA and the input voltage V_{IN} changes from 2.5 V to 5 V, the variation of output voltage is 0.32 mV. Therefore, the line regulation rate of OLC-LDO is 0.128 mV/V. Figure 17 shows the load regulation of OCL-LDO. When the load changes from 0 to 100 mA, the variation of output voltage is 0.17 mV. Therefore, the load regulation rate of OCL-LDO is 0.0017 mV/mA.

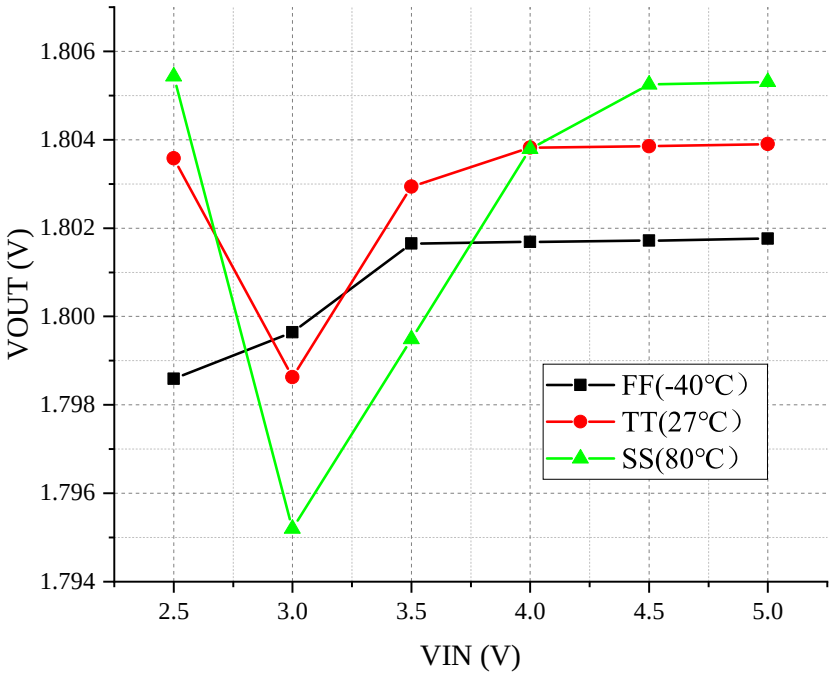

Figure 16. Line regulation rate of OCL-LDO.

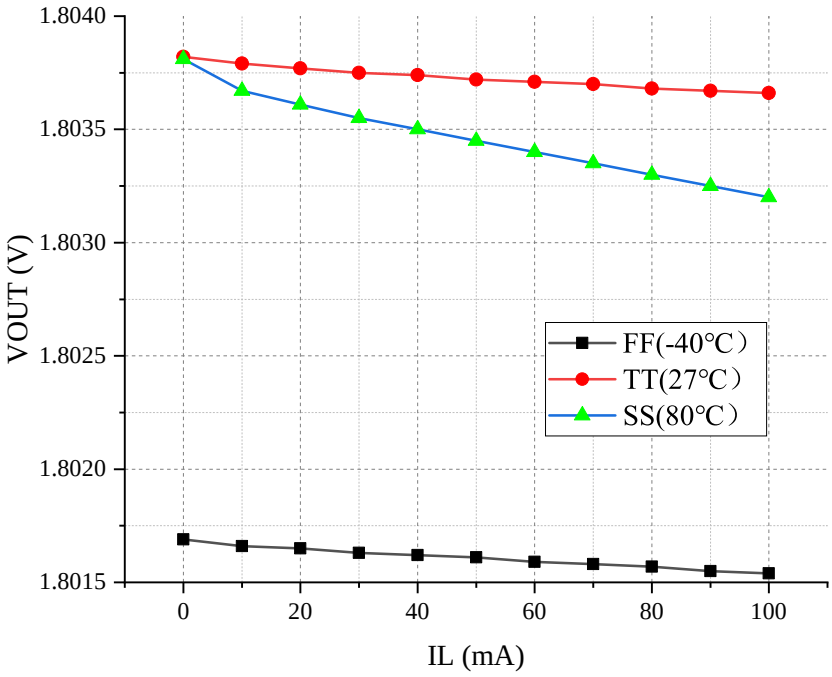

Figure 17. Load regulation of OCL-LDO.

Figure 18 shows the measured load transient responses of the OCL-LDO regulator. When I_L changes from 1 mA to 100 mA with an edge time of 1 µs, the undershoot is 37 mV and the overshoot is 33 mV. The recovery time for the overshoot voltage is 1.2 µs and the recovery time for the undershoot voltage is 1.6 µs. When the output load I_L changes from 0 to 100 mA with an edge time of 100 ps, the undershoot is 1.7 V and the overshoot is 1.4V. The recovery time for the overshoot voltage is 0.7 µs, and the recovery time for the undershoot voltage is 2.5 µs. It can be seen that when the load changes drastically, thanks to the proposed FFL fast feedback loop, the transient response time of the proposed OCL-LDO does not increase significantly. There is even smaller recovery time of the output overshoots.

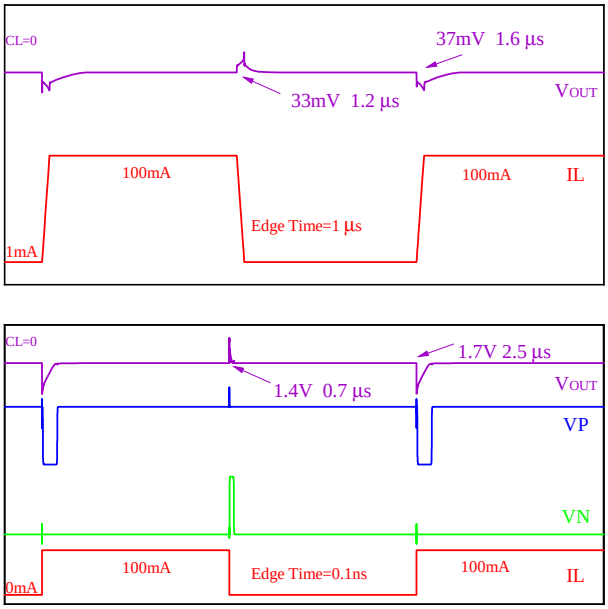

Figure 18. Transient responses of the OCL-LDO.

A performance comparison between the proposed OCL-LDO regulator and other reported LDO regulators is shown in Table 1. Compared with others works, the proposed circuit is stable with or without a large external capacitor. Due to the high gain of the proposed OCL-LDO, its load regulation and line regulation are better than other works. Its gain is 109 dB, load regulation is 0.0017 mV/mA, and line regulation is 0.128 mV/V. The change of the output voltage of the proposed circuit is small, and its undershoot voltage and overshoot voltage are 37 mV and 33 mV, respectively, and the recovery time is 1.6 µs. To compare various regulators implemented in different technologies, a comparison method based on FOM is adopted. Its calculation method is Equation (4) [6,12].

Table 1. Comparison with some advanced LDOs.

Reference	**[30]**	**[17]**	**[11]**	**[31]**	**[29]**	**[27]**	**This Work**
Year	2022	2023	2014	2020	2012	2019	**2023**
Technology (nm)	350	500	65	180	350	180	**180**
Chip size (mm^2)	0.077	0.29	0.013	0.15	0.4	0.18	**0.068**
V_{IN} (V)	2.7∼3.3	5.2–20	0.75∼1.2	70	1.2∼1.5	3.3	**2.5–5**
V_{OUT} (V)	2.5	5	0.6	66	1	2.8	**1.8**
IQ (µA)	66	244	15.9–478	288	45	32	**76**
I_{OUT} (max)(mA)	100	100	50	100	50	100	**100**
I_{OUT} (min)(mA)	0.01	0.22	0	0	1	0	**0**
Line regulation (mV/V)	0.8	0.88	4	90	N/A	5.7	**0.128**
Load regulation (mV/mA)	0.06	0.22	0.18	1.7	N/A	0.028	**0.0017**
C_T (min)(pF)	14	5	474.1	6	41	1,000,100	**9**
(on-chip capacitance) (pF)	14	5	4.1	6	41	100	**9**
ΔV_{OUT} (mV)	255	70	113	2480	70	640	**37**
PSRR (dB)	−41 (10 kHz)	−49 (100 kHz)	−51 (1 kHz)	N/A	N/A	N/A	**−46 (1 kHz)**
Setting time (µs)	0.7	2	0.25	1.63	4	52	**1.6 (99%)**
Edge time Δt (µs)	0.4	1	0.1	0.3	1	0.1	**1**
Edge time ratio K	4	10	1	3	10	1	**10**
FOM (V×pF/A)	9.43	8.5	102.4	128.56	51.7	204,820.5	**2.531**

$$FOM = K(\frac{\Delta V_{OUT} C_T \times I_Q}{\Delta {I_{OUT}}^2}) \quad (4)$$

where K is the edge time ratio and is defined as:

$$K = \frac{\Delta t \ used \ in \ the \ measurement}{the \ smallest \ \Delta t \ among \ the \ designs \ for \ comparison} \quad (5)$$

From Table 1, the proposed OCL-LDO regulator design achieves a comparable or better FOM with the other reported LDO regulators.

5. Conclusions

OCL-LDOs are attracting more and more attention because of their convenience for integration with other circuit modules. However, OCL-LDOs usually have poor transient characteristics. This work proposes a comparator-based transient enhanced OCL-LDO. Due to the fast response speed of the comparator, the transient characteristics of the OCL-LDO can be greatly improved. The overshoot and undershoot voltages of the proposed OCL-LDO are 33 mV and 37 mV, respectively, and the recovery time are 1.2 µs and 1.6 µs, respectively. Through the DFC frequency compensation technology, it can be ensured that the output of the OCL-LDO remains stable within the load variation range of 0 mA to 100 mA. The phase margin of the proposed OCL-LDO can be greater than 50 degrees under different current loads and capacitive loads. The proposed OCL-LDO integrates a band-gap reference, which can make its output temperature invariant and more reliable for integration with other modules.

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