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Design Technique of K-Band CMOS Phase Shifter with L-C-L T-Type Low Pass Structure

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Abstract: In this study, we designed a 5-bit K-band CMOS switch type phase shifter. In order to minimize phase and gain errors, a design technique for bits constituting the phase shifter was proposed. The proposed design technique has been achieved by adjusting the resonant frequencies of inductance and capacitance in the L-C-L T-type low pass filter structure. Through this, a method of optimizing the phase shifter with the T-type low pass filter structure was presented. The K-band 5-bit phase shifter was designed with a 65 nm CMOS process to verify the feasibility of the proposed design technique. The core size was 0.78 × 0.21 mm^2. At the frequency ranges of 22.0 to 23.0 GHz, the insertion loss and RMS phase and gain errors were measured to be 7.44 ± 2.0 dB, 2.6°, and 1.2 dB, respectively.

Keywords: CMOS; gain error; phase error; phase shifter

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1. Introduction

Recently, research and development of various RF circuits for array antenna systems has become active as the utilization of beamforming systems including 5G mobile communication has increased [1–3]. In particular, in the beamforming system, sophisticated phase variation is recognized as an essential technology. Therefore, various structures of phase shifters have already been introduced [4–6], and research to improve the performance of phase shifters is still actively underway.

In particular, passive-type phase shifters are widely used in beamforming systems because they allow bidirectional signal flow and have a relatively simple structure [7,8]. For such passive-type phase shifters, resolution, insertion loss, and phase and gain errors are major performance indicators. Because a phase shifter consists of several bits and operates in pass and shift modes for each bit, the phase shifter is characterized by having various operating states compared to other RF circuits [4,9,10]. As such, since the phase shifter operates in various states, it is important to minimize the phase and gain errors for each state of the phase shifter when considering the performance of the entire beamforming system. Therefore, various optimization techniques have been introduced to minimize the phase and gain errors for each state [7,10,11]. Most of these optimization techniques are based on mathematical analysis.

In this study, for the beamforming system in the flexible access common spectrum (FACS) millimeter-wave band [12], a 5-bit K-band complementary metal-oxide-semiconductor (CMOS) phase shifter was designed using the L-C-L T-type low pass structure. In order to minimize the root mean square (RMS) phase and gain errors of the phase shifter, a design technique was proposed that utilizes the resonances of the inductance and capacitance constituting each bit. In particular, the proposed design technique provides a method for

graphically understanding the process of minimizing phase and gain error using phase and gain graphs according to the frequency of shift and pass modes. Based on this, the proposed design technique provides a method of obtaining the initial values of the inductors and capacitors constituting the phase shifter through impedance analysis using the equivalent circuits of the phase shifter. In addition, for further improvement of phase and gain errors, the 180° bit is assumed to be mounted on a differential amplifier located on a signal path passing through the phase shifter, and accordingly, the 180° bit was not included in the phase shifter of this study.

2. Proposed Design Technique of the T-Type Phase Shifter

In this study, the designed phase shifter consists of a total of five bits, excluding the 180° bit. When the 180° bit is implemented in a phase shifter, a large chip area is generally required compared to other bits. In addition, the 180° bit has a large insertion loss compared to other bits, and generally has a narrow bandwidth. On the other hand, it is relatively easy to configure the 180° bit in a typical differential amplifier structure rather than a phase shifter [12–14]. In this case, problems related to area, insertion loss, and bandwidth resulting from the 180° bit can be solved. As a representative example, the 180° phase shift function can be mounted on power amplifiers and low-noise amplifiers of differential structures [12–14]. Therefore, the 180° bit was not included in the phase shifter of this study.

Figure 1 shows the schematic of the unit-bit used in this study. All of five bits, from 5.625° bit to 90° bit, are designed to have the same structure of L-C-L T-type low pass filter structure. In Figure 1, R_{M1} is the parasitic resistance of the ON state M_1. R_{M2} and C_{M2} are parasitic components in ON and OFF states of M_2, respectively. In the pass and shift modes of each bit, M_1 operates in ON and OFF states, respectively, and M_2 operates in the opposite state to M_1.

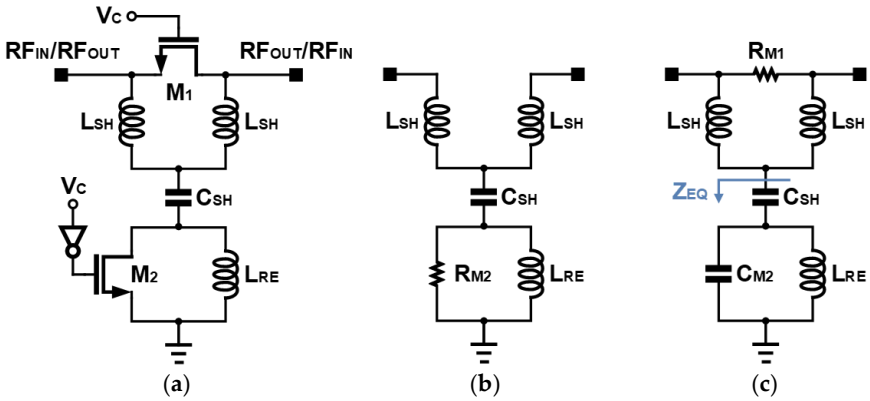

Figure 1. T-type structure: (**a**) schematic of the used T-type structure, and equivalent circuits for the (**b**) shift and (**c**) pass modes.

In this study, for convenience of analysis, it is assumed that the terminal impedance is 50 Ω, and the resistance of the transistor is negligibly small when the transistor is in the ON state. In addition, when the transistor was in the OFF state, it was modeled as a drain-source parasitic capacitance. Such assumptions and simplifications are intended to obtain initial values of inductors and capacitors constituting the phase shifter. Therefore, in the final design stage should be accompanied by an optimization process through electromagnetic (EM) simulation, etc.

2.1. Analysis of the Operation of the Phase Shifter

In the shift mode, for the convenience of intuitive analysis, it is assumed that the impedance of R_{M2} is negligible compared to the impedances of L_{RE} and C_{SH}. Therefore, the equivalent circuit of the shift mode shown in Figure 1b may be considered as the T-network of L_{SH}-C_{SH}-L_{SH}. At this time, for convenience of analysis, the parasitic capacitance of M_1 in

the OFF state in shift mode was ignored because it plays an incidental role in the analysis of this study. If the parasitic capacitance of M_1 is considered, there is an effect of decreasing the required L_{SH} value compared to the case not considered [15]. In this study, optimization was carried out in consideration of the parasitic capacitance of M_1 in the final design stage of the phase shifter.

In the case of the pass mode, the equivalent circuits according to frequency are shown in detail in Figure 2. The Z_{EQ} of Figure 1c in the pass mode is calculated as follows:

$$Z_{EQ} = \frac{1 - \omega^2 L_{RE}(C_{SH} + C_{M2})}{j\omega C_{SH}(1 - \omega^2 L_{RE} C_{M2})} \tag{1}$$

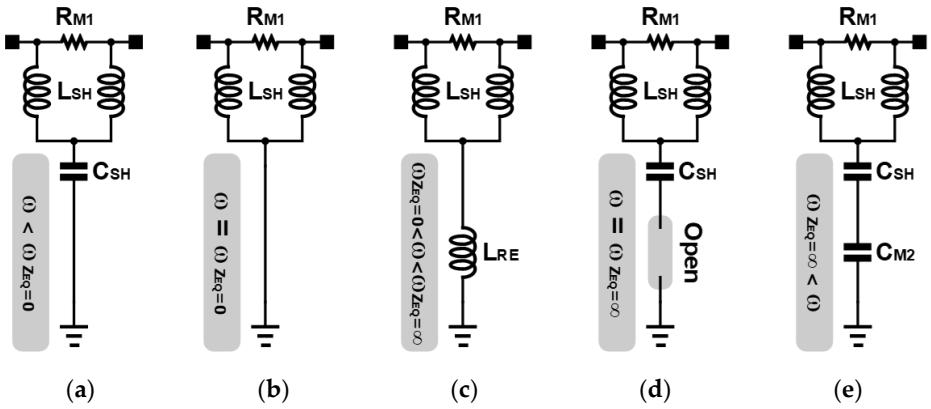

Figure 2. Equivalent circuits for pass mode according to frequency: (**a**) $\omega < \omega_{ZEQ\,=\,0}$, (**b**) $\omega = \omega_{ZEQ\,=\,0}$, (**c**) $\omega_{ZEQ\,=\,0} < \omega < \omega_{ZEQ\,=\,\infty}$, (**d**) $\omega = \omega_{ZEQ\,=\,\infty}$, and (**e**) $\omega_{ZEQ\,=\,\infty} < \omega$.

In addition, the values of ω satisfying $Z_{EQ} = 0$ and $Z_{EQ} = \infty$ are calculated as follows:

$$\begin{aligned} \omega_{Z_{EQ}=0} &= \frac{1}{\sqrt{L_{RE}(C_{SH}+C_{M2})}}, \\ \omega_{Z_{EQ}=\infty} &= \frac{1}{\sqrt{L_{RE}C_{M2}}} \end{aligned} \tag{2}$$

The Z_{EQ} values calculated in Equation (2) are utilized in the minimization technique of phase and gain errors described in Sections 2.2 and 2.3.

2.2. Design Technique for Securing the Required Phase

A phase of each bit of a phase shifter is defined as a phase difference between shift and pass modes. Therefore, in order to improve the phase accuracy of each bit, the phases of shift and pass modes were first calculated. In this study, the phases in shift and pass modes were calculated as follows:

$$\phi_{S21,Shift} = \tan^{-1}\left(-\frac{2\omega L_{SH} - \omega^3 L_{SH}^2 C_{SH}}{Z_0(1 - \omega^2 L_{SH} C_{SH})}\right) \tag{3}$$

$$\phi_{S21,Pass} = \tan^{-1}\left(\frac{\omega Z_{EQ} R_{M1}^2 L_{SH}(2Z_{EQ}+\omega L_{SH}) - \omega^2 Z_0 R_{M1} L_{SH}^2 (2Z_{EQ} - \omega L_{SH})}{\{\omega^4 L_{SH}^4 - 4\omega^2 Z_{EQ} L_{SH}^2 (Z_{EQ}+\omega L_{SH})\}(R_{M1}+Z_0) - Z_{EQ} Z_0 R_{M1}^2 (Z_{EQ}+\omega L_{SH})}\right) \tag{4}$$

$$\phi_{S21,Pass}\big|_{Z_{EQ}=\infty} = \tan^{-1}\left(\frac{-2\omega R_{M1}^2 L_{SH}}{4\omega^2 L_{SH}^2 (R_{M1} + Z_0) + Z_0 R_{M1}^2}\right) \tag{5}$$

where $\phi_{S21,Shift}$ and $\phi_{S21,Pass}$ are phases of the shift and pass modes, respectively. In general, the phase in pass mode has a very small value. For each bit, the difference in phases calculated from Equations (3) and (4) becomes the phase of the corresponding bit. In this

case, it is assumed that the termination impedance Z_0 is 50 Ω. For convenience, ω_P was defined as follows:

$$\omega_P = \frac{1}{\sqrt{L_{SH}C_{SH}}} \tag{6}$$

Here, ω_P represents the frequency at which the phase of the output signal compared to the input signal changes to 90°, assuming that R_{M2} is sufficiently small in the shift mode of Figure 1b and the impedance by L_{RE} is ignored. In this study, in order to make the phase of the pass mode close to zero, Z_{EQ} is designed to be ∞ at the operating frequency. At this time, when the value of ω_P is adjusted through L_{SH} and C_{SH}, the slope of Equation (3) is also adjusted. Accordingly, as shown in Figure 3a, a desired phase in the shift mode can be secured at a given operating frequency. In Figure 3a, ω_{P90} and ω_{P45} are shown as examples. Here, ω_{P90} and ω_{P45} are ω_P values for phase shift of 90° and 45° at a given operating frequency, respectively. As a result, through this process, values of $\omega_{ZEQ=\infty}$ and ω_P are set.

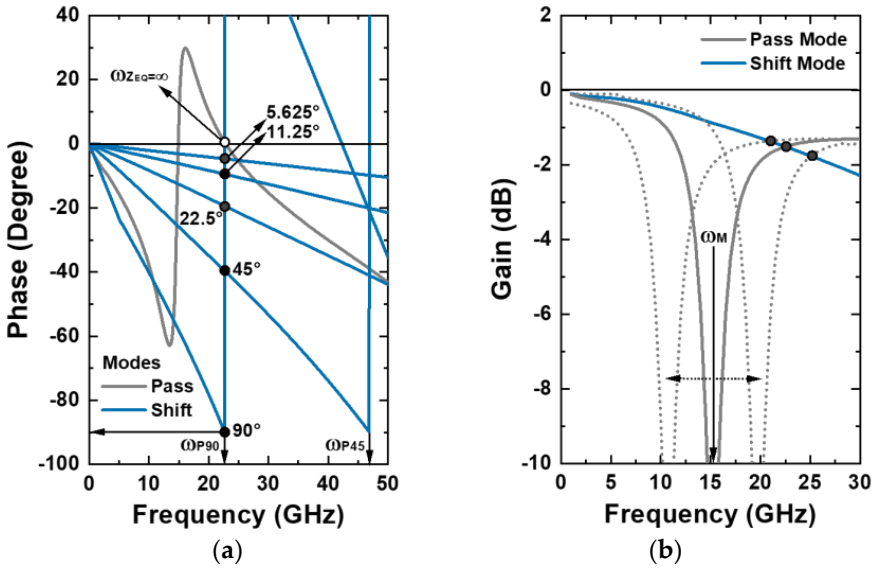

Figure 3. Conceptual diagrams for securing required (**a**) phase and (**b**) gain.

2.3. Design Technique for Minimizing Gain Error

As a next step, a design was performed to minimize the gain error between shift and pass modes based on the previously determined values of $\omega_{ZEQ=\infty}$ and ω_P. Figure 3b shows a conceptual diagram for minimizing the gain error. As can be seen in Figure 3b, the gain in shift mode decreases as the frequency increases. On the other hand, in the case of pass mode, as can be predicted from Figure 2, the gain increases as the frequency increases in the region after the frequency satisfying $\omega_{ZEQ=0}$. Therefore, when the frequency satisfying $\omega_{ZEQ=0}$ is adjusted, the gain of shift and pass modes may be set equally at the operating frequency. In Figure 3b, ω_M is defined as a frequency satisfying $\omega_{ZEQ=0}$.

Here, in order to maintain the minimized phase error previously described, the values of $\omega_{ZEQ=\infty}$ and ω_P determined in Section 2.2 must be maintained. Therefore, in order to maintain the values of $\omega_{ZEQ=\infty}$ and ω_P, the gain error can be minimized by adjusting the L_{RE}, C_{M2}, and C_{SH} while maintaining the ratio of L_{SH} to C_{SH} and the ratio of L_{RE} to C_{M2}.

In conclusion, the design process of the proposed phase shifter can be summarized step by step as follows.

- Step 1: In the pass mode, the $L_{RE}C_{M2}$ value is set so that $\omega_{ZEQ=\infty}$, the frequency at which Z_{EQ} becomes infinite, becomes the desired operating frequency. This process allows the phase in the pass mode to become zero.
- Step 2: In the shift mode, the frequency of the ω_P determined by $L_{SH}C_{SH}$ is adjusted to secure the desired phase difference at the desired operating frequency.

- Step 3: In the pass mode, ω_M, the frequency at which Z_{EQ} becomes zero, is adjusted so that gains in shift and pass modes are the same at the desired operating frequency. In this case, the value of $L_{RE}(C_{SH} + C_{M2})$ is used to adjust the ω_M.
- Step 4: Finally, the initial values of the inductors and capacitors constituting the unit-bit are set with L_{RE}, L_{SH}, C_{SH}, and C_{M2} values satisfying the previous steps 1, 2, and 3.

3. Design Results of the Designed Phase Shifter

To verify the feasibility of the proposed design technique, a K-band phase shifter with L-C-L T-type low-pass filter structure using 65 nm RFCMOS process which provides eight metal layers.

Figure 4 shows the simulated phases for the shift and pass modes in the 45° and 90° bits. In this study, the values of ω_P for 45° and 90° bits were designed to be 41.5 GHz and 23.4 GHz, respectively. Here, ω_{P45} and ω_{P90} present the values of ω_P for 45° and 90° bits, respectively. As shown in Figure 4, simulation results of high-accuracy phase shift were obtained for both 45° and 90° bits.

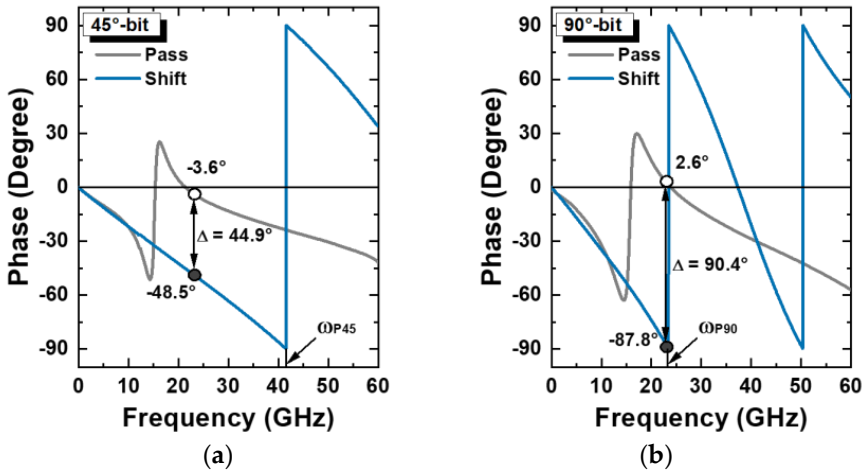

Figure 4. Simulated phases for shift and pass modes for (**a**) 45° and (**b**) 90° bits.

In addition, as shown in Figure 5, the values of ω_M for 45° and 90° bits were designed to be 15.2 GHz and 16.5 GHz, respectively. Here, ω_{M45} and ω_{M90} present the values of ω_M for 45° and 90° bits, respectively. As can be seen in Figure 5, the proposed design technique minimizes the gain error at a given operating frequency.

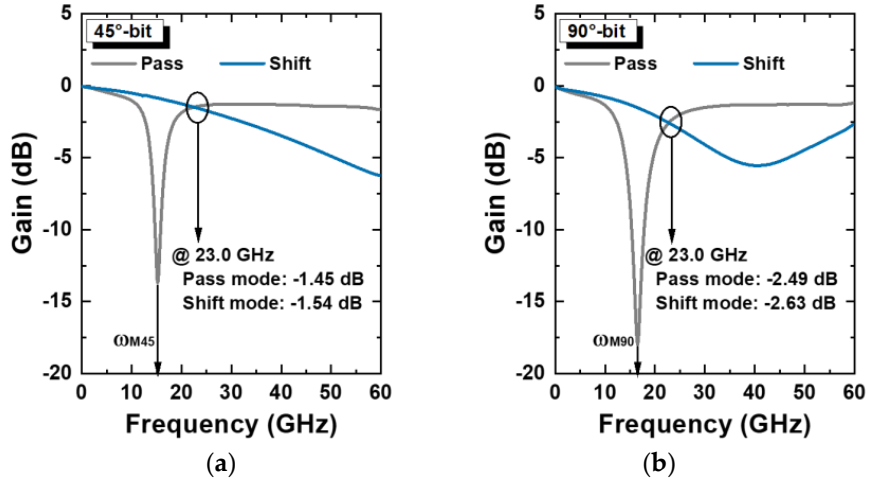

Figure 5. Simulated gains for shift and pass modes for (**a**) 45° and (**b**) 90° bits.

In Table 1, the design parameters of the designed phase shifter were shown. The values of all active and passive devices were finally optimized using EM simulation after all bits were connected.

Table 1. Size of the used transistors, inductors, and capacitors.

Bits	90°	45°	22.5°	11.25°	5.625°
M_1 (μm) [(1)]	48	180	360	384	384
M_2 (μm) [(1)]	36	28	78	54	128
C_{SH} (fF)	143.8	88.54	101.0	47.3	34.2
L_{SH} (pH)	138.0	72.2	10.0	33.0	10.5
L_{RE} (pH)	274.6	566.4	495.8	782.7	483.4

[(1)] Total gate width.

Figure 6 shows the configuration of the designed phase shifter, and each bit is designed with the schematic of the unit-bit of Figure 1. C_{90} with 56.3 fF is additionally used for matching between bits. Although 180° bit is not mounted on the designed phase shifter of this study, the 180° bit can be easily implemented by connecting two 90° bits designed in this study if a 180° bit is required.

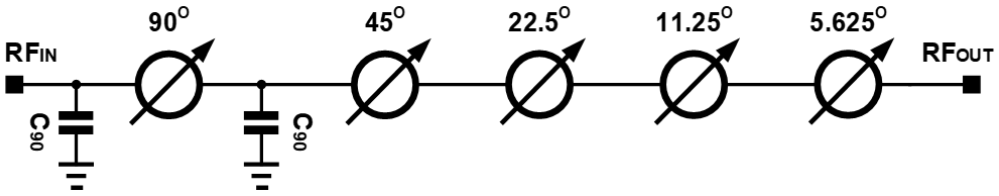

Figure 6. Overall structure of the designed phase shifter.

Figure 7 shows the simulated phase and gain characteristics. The effect of all passive devices, including interconnection lines and pads were considered through EM simulations. Decoupling capacitors are positioned between the pads for applying the control voltage V_C for each bit to stabilize the V_C. In this study, 1.0 V was used as V_C for simulation and measurement.

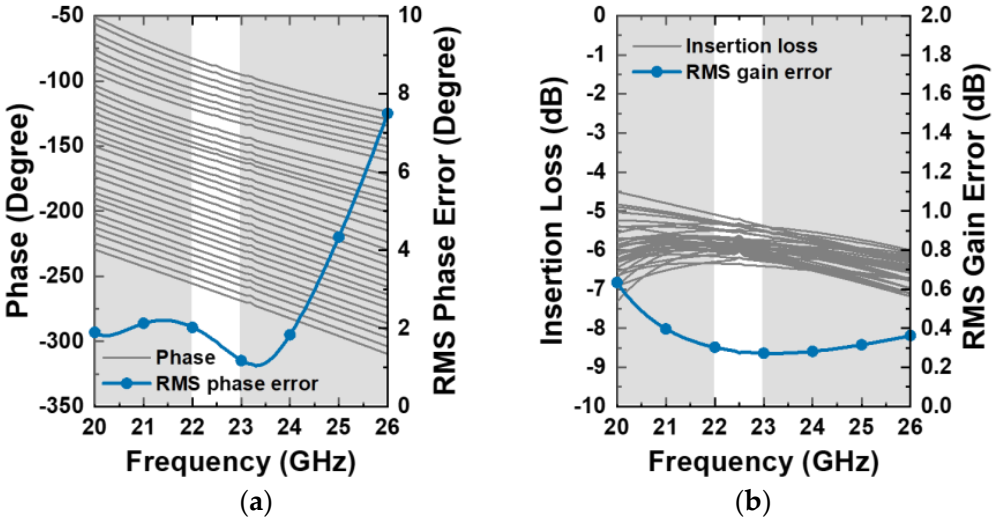

Figure 7. Simulated results: (**a**) phase and RMS phase error and (**b**) insertion loss and RMS gain error.

Figure 8 shows a photograph of the designed phase shifter with chip and core sizes of 960 × 400 μm^2 and 780 × 210 μm^2, respectively. Considering that the 180° bit is mounted on the amplifier of the differential structure, the 180° bit is not mounted on the phase shifter of this study, so it is designed in a compact size. We used bonding wire for V_C pads for dc

voltages, and RF input and output signals were measured through on-wafer probing to minimize measurement error.

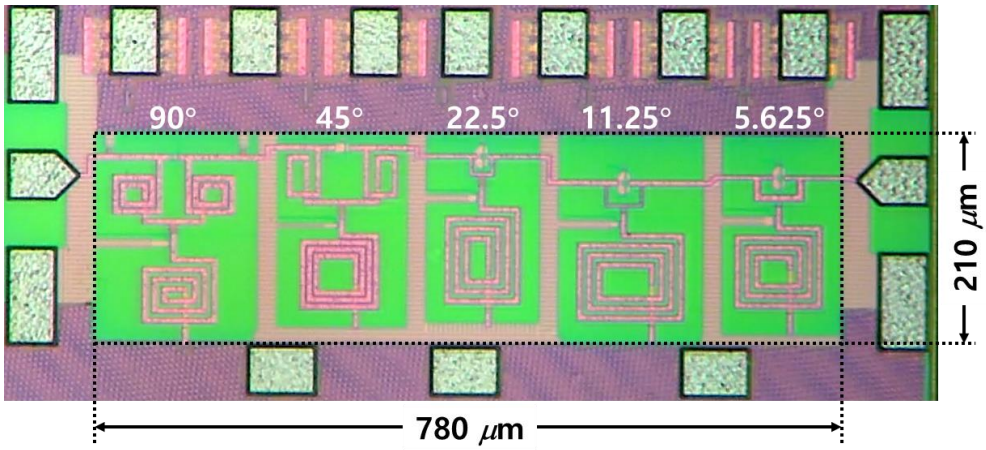

Figure 8. Chip photograph of the designed K-band CMOS phase shifter.

Figure 9 shows the measured phase and gain characteristics. In the frequency range of 22.0 GHz to 23.0 GHz, insertion loss, RMS phase error, and RMS gain error were measured as 7.44 ± 2.0 dB, <2.6°, and <1.2 dB, respectively. Compared to the simulation results, in the measurement results, insertion loss increased and RMS phase and gain errors were somewhat degraded. The main reason expected is that the accuracy of EM simulation in the design process of the 90° bit seems to have deteriorated. If the EM simulation accuracy for the 90° bit is improved, it is expected that RMS phase and gain errors can be improved. Accordingly, it is also expected that the measurement results of the phase shifter with a wider operating frequency range can be obtained.

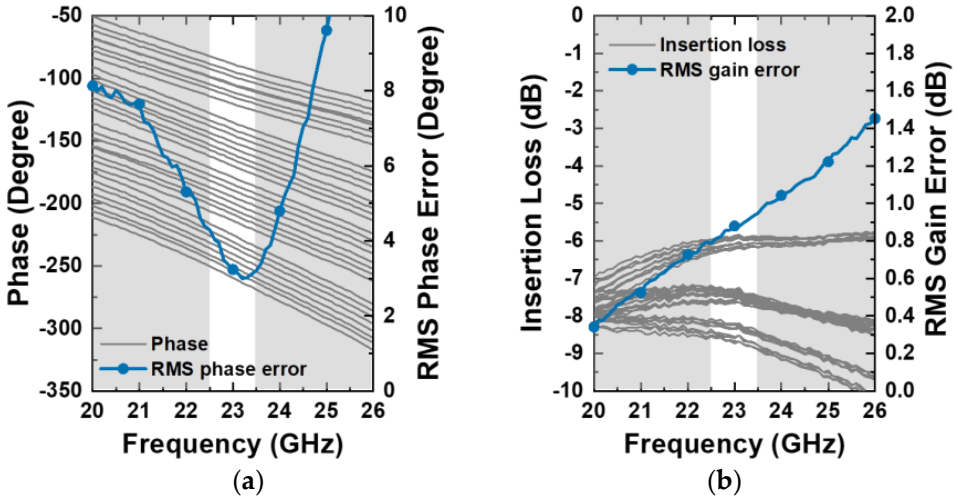

Figure 9. Measurement results: (**a**) phase and RMS phase error and (**b**) insertion loss and RMS gain error.

Table 2 shows the performance of the CMOS phase shifters available in the literature. As shown in Table 2, although the measurement results of the designed phase shifter deteriorated compared to the simulation results, the measurement results of the improved RMS phase error were obtained. In addition, the designed phase shifter has no 180° bit, resulting in the measurement results of competitive insertion loss. Thanks to the absence of the 180° bit, the proposed phase shifter has a compact core size when compared to previous 5-bit phase shifters.

Table 2. Performance comparison of CMOS phase shifter.

Ref.	Tech. (nm)	Freq. (GHz)	Total Phase (°)/bits	Insertion Loss (dB)	RMS Phase Error (°)	RMS Gain Error (dB)	Core Size (mm^2)	Topology
[16]	65	27.5–28.35	360/4	<7.6	<9.0	N/A	0.23	STPS
[17]	28	29–37	360/4	12.8 ± 2.5 (@ 33 GHz)	8.8 (1)	N/A	0.08	STPS
[18]	65	27–42	360/5	<14.5	<3.8	<2.1	0.395	STPS
[19]	65	57–64	360/5	14.3 ± 2	<9.5	<1.1	0.094	RTPS & STPS
[20]	90	57–64	360/5	14.6 ± 3	<10	<1.8	0.34	STPS
[21]	180	26–30	360/5	<17.4	<3.3	<0.85	0.84 (2)	STPS
This work	65	22.0–23.0	180/5	7.44 ± 2.0	<2.6	<1.2	0.16	STPS

(1) Specific value at the center frequency, (2) Chip area.

4. Conclusions

In this study, a K-band CMOS phase shifter with L-C-L T-type low pass structure was designed. To reduce the RMS phase and gain errors, a design technique using resonances in the L-C-L T-type low pass structure was proposed. First, the phase was determined through optimization of two resonance frequencies for each bit. Based on the two determined resonance frequencies, the design parameters of each bit were set so that the gains of shift and pass modes became the same. To verify the feasibility of the proposed design technique, we designed the K-band 5-bit phase shifter using a 65 nm RFCMOS process. At the frequency ranges of 22.0 GHz and 23.0 GHz, the measured insertion loss, RMS phase error, and RMS gain error were 7.44 ± 2.0 dB, 2.6°, and 1.2 dB, respectively.

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