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Effect of Non-Ideal Cross-Sectional Shape on the Performance of Nanosheet-Based FETs

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Abstract: In this article, the effects of non-ideal cross-sectional shapes of stacked nanosheet FET (NSFET) and nanosheet FET with inter-bridge channel (TreeFET) are studied through calibrated 3D TCAD simulations. The impact of non-ideal cross-sectional shapes on the electrical characteristics due to insufficient/excessive etch processes are investigated in terms of inner spacer (IS), nanosheet (NS) channel, and inter-bridge (IB) channel. Simulation results show that the geometry and material of the IS have significant effects on the performance of the NSFET. Compared with the rectangular inner spacer (RIS), the low-k crescent inner spacer (CIS) enhances the gate control capability while the high-k CIS degrades the drain-induced barrier lowering ($DIBL$) and reduces the gate capacitance (C_{gg}). The tapered NS channel improves short-channel effects (SCEs), but sacrifices the driving current. For the TreeFET, considering the fin angle and concave arc, the IB channel can degrade the gate control capability, and SCEs degradation is severe compared to the ideal structure. Therefore, the non-ideal cross-sectional shapes have a significant impact on NSFET-based structure. This research provides development guidelines for process and structure optimization in advanced transistor technology nodes.

Keywords: gate-all-around (GAA); inner spacer (IS); nanosheet (NS); inter-bridge (IB); cross-sectional shape; TCAD

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1. Introduction

Recently, gate-all-around (GAA) field-effect transistors have been proposed and widely studied to improve the short-channel effects (SCEs) that arise due to the continuous scaling down of the MOSFETs. Among them, stacked nanosheet field-effect transistors (NSFETs) are considered very promising candidates thanks to their excellent gate control capability, superior current drive capabilities, variable channel widths, and FinFET-compatible processes [1–6].

However, continuous scaling down leads to many non-ideal effects, such as self-heating effects (SHEs) [7–9] and higher leakage currents [10,11]. Moreover, the manufacturing process of NSFET is highly complex and presents numerous engineering challenges at each step. Currently, foundries struggle to increase the yield of advanced process nodes, indicating the presence of many non-ideal factors [12,13]. Among those factors, non-ideal cross-sectional shapes resulting from insufficient or excessive etch can significantly impact the NSFET performance and lead to yield issues [14–17].

First, the non-ideal cross-sectional shape of the inner spacer (IS) due to insufficient etch can significantly impact the NSFET performance. The primary function of the IS is to isolate the gate region from the source-drain extension regions. The indentation of SiGe defines the gate length and high-k metal gate (HKMG) placement [18]. It was shown that the dimension of the IS significantly affects NSFET's characteristics, leading to many studies on optimizing the size and structure of the IS [19–23]. However, most published papers on

IS optimization are based on the ideal cross-sectional shape of the IS. There is little analysis based on the non-ideal cross-sectional shape of the IS formed by actual NSFET processes.

Second, the non-ideal channel cross-sectional shape due to excessive etch also severely impacts the performance of NSFETs. In the channel release, it is important to reduce the non-uniform etch front along the nanosheet width and maximize the effective channel width [15]. When the nanosheet (NS) width and the spacing distance between the NS channels of NSFET are large enough, the effect of non-ideal etching on the channel cross-sectional shape can be ignored. Rectangular channel cross-sectional shapes with rounded corners can be found in the papers on NSFET TCAD simulation [24–27]. However, when the distance between the channels and the NS width are scaled down, the etching selectivity will also cause the edge of the NS to be etched when removing the SiGe sacrificial layers, which leads to both ends of the NS being thinner than its middle [28]. In this case, the influence of the non-ideal channel cross-sectional shape cannot be ignored.

Third, the non-ideal etching has a more complex influence on the channel cross-sectional shapes of NSFET-based advanced structures, such as the TreeFET, which combines the stacked NS channel and the fin-like inter-bridge (IB) channel [29–32]. The TreeFET channel geometry can be achieved by partially removing the SiGe sacrificial layers between the stacked NS channels during the channel release [29]. The presence of IB aggravates the influence of the non-ideal etching on cross-sectional shapes. The width of the top stacked sheet is smaller than that of the bottom stacked sheet due to the fin angle in the vertical direction during the fin formation process. Therefore, the width of IB from top to bottom is not uniform when the IB is formed by the subsequent isotropic etching step. In addition, the IB can be wider near the NS due to the insufficient etching during the channel release. Therefore, the edges of IB are not straight lines but concave arcs. The impact of these non-ideal channel cross-sectional shapes caused by non-ideal etching on the TreeFET performance are also worthy of in-depth analysis.

In summary, the non-ideal cross-sectional shapes of the IS, NS, and IB are formed due to the limited etching selectivity. However, in previous TCAD simulations, the cross-sectional shapes are often idealized [19–21]. The non-ideal cross-sectional shape has a significant impact on the characteristics of the devices. Therefore, it is necessary to analyze the effects of the IS, NS, and IB cross-sectional shapes formed by non-ideal etching selectivity in the actual process on the device's performance. This work comprehensively analyzes this non-ideal effect based on calibrated TCAD simulations. The rest of this article is organized as follows. In Section 2, we mainly introduce the device structure and electrical parameters in the simulation. The simulation setting is also discussed. In Section 3, we analyze the influence of non-ideal cross-sectional shapes on device performance. Finally, the conclusions are given in Section 4.

2. Device Structure and Simulation Methodology

2.1. Device Structure

The 3-D schematic and 2-D cross-sectional views along and across the channel of the conventional 7-nm NSFET with punch through stopper (PTS) doping scheme, which is referred to in [19], are shown in Figure 1. The gate length (L_g) and inner spacer length (L_{sp}) are 12 and 5 nm, respectively. The S/D length is set to 13 nm. The vertical channel space (N_{ch}) and channel thickness (t_{ch}) are 10 and 5 nm, respectively. The doping concentrations of the channel and S/D region are 1×10^{16} cm^{-3} and 1×10^{20} cm^{-3}, respectively. Moreover, in order to reduce I_{OFF}, the doping concentration of the PTS structure is 5×10^{18} cm^{-3}. An effective-oxide-thickness (EOT) of 0.7 nm (0.45 nm SiO_2 and 1.5 nm HfO_2) is achieved. The source and drain contact resistance of NSFET is 1×10^{-9} $\Omega \cdot$cm^2. All the relevant physical parameters of the device are listed in Table 1.

Table 1. Device parameters.

Parameters	Values
Gate length, L_g	12 nm
Spacer length, L_{sp}	5 nm
Source/Drain length, L_{sd}	13 nm
Contact gate pitch, CGP	48 nm
Channel width, W_{ch}	20–50 nm
Channel thickness, t_{ch}	5 nm
Vertical channel space, N_{ch}	10 nm
Equivalent oxide thickness, *EOT*	0.7 nm
Channel doping, $N_{channel}$	1×10^{16} cm^{-3}
Source/Drain doping, N_{SD}	1×10^{20} cm^{-3}
PTS doping, N_{bulk}	5×10^{18} cm^{-3}
Contact resistance	1×10^{-9} Ω·cm^2

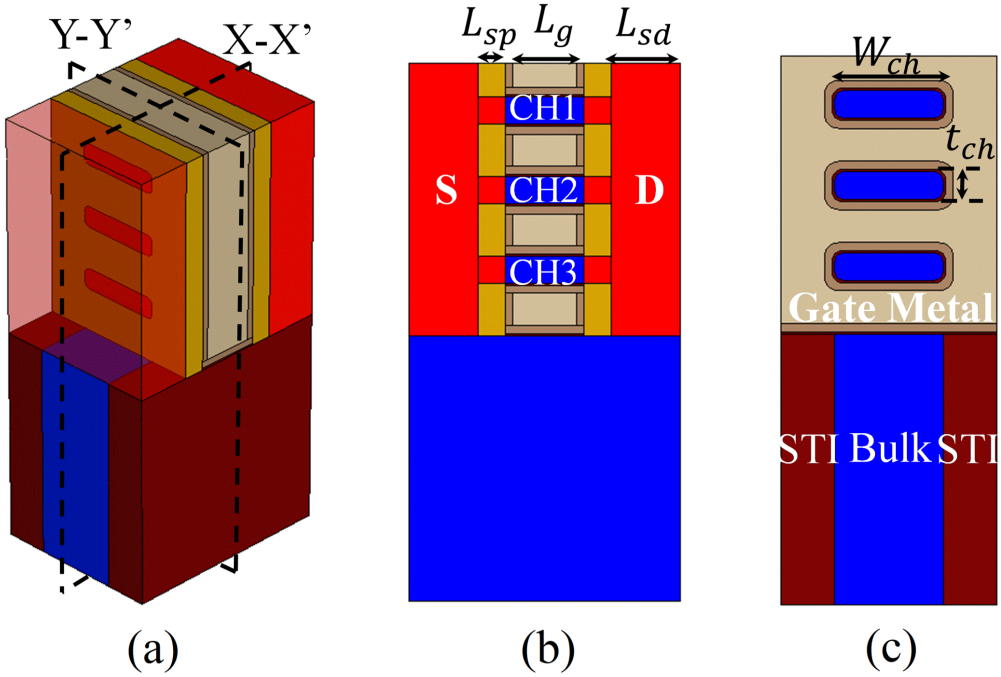

Figure 1. (**a**) 3-D view, (**b**) X-X′ view, and (**c**) Y-Y′ view of the conventional 7-nm NSFET with PTS doping scheme.

2.2. Simulation Settings

To ensure the accuracy of the following simulations, the physical parameters of NSFET are calibrated using the experimental data in [2]. According to the cross-sectional shapes given in [2], a similar structure was designed. In this calibration work, the channel had a rectangular cross-sectional shape with rounded corners, and the crescent inner spacer was also designed. The channel width is set to 50 nm to minimize the influence of the non-ideal channel cross-sectional shape on the NSFET performance. Figure 2 shows good calibration with the experimental data in the saturation regime. Here, we adjusted the channel doping concentration and the gate metal work function to control the OFF-state current (I_{OFF}) in the subthreshold region. Then, we adjusted the high-field saturation model parameters to make the simulation results match the experimental data in the saturation region.

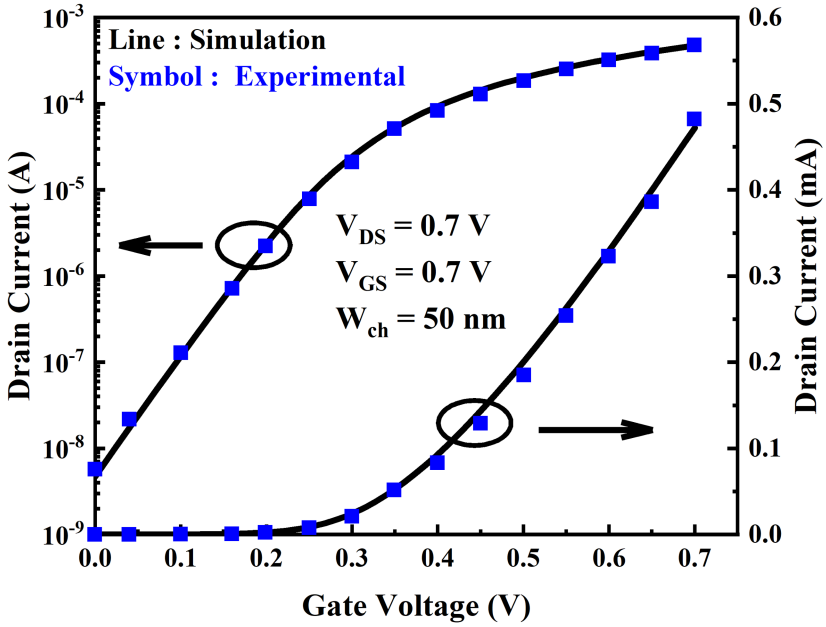

Figure 2. The calibration of I_d–V_g curve of the NSFET (W_{ch} = 50 nm) with experimental data from [2] in the saturation regime.

In addition, the density gradient quantization model is used to consider the quantum confinement effect of the nanosheets. The recombination models include Shockley–Read–Hall (SRH) and Auger models. In order to calculate the effective bandgap width, which determines the intrinsic density, the Bandgap Narrowing Slotboom Model was used. As the thickness of the nanosheet channel is only a few nanometers (N_{ch} = 5 nm), the mobility cannot be expressed with a typical field-dependent interface model. Thus, the thin-layer mobility and Lombardi models are applied to reflect the phonon and surface roughness scattering. The Doping Dependence model is specified to reflect the carrier-impurity scattering. The high field saturation model is also included to describe the carrier velocity saturation effect at high electric fields.

Finally, due to the different mobilities of the NS with (100) surface orientation and IB with (110) surface orientation, the parameter sets of the mobility model related to the surface orientation in TreeFET are adjusted [29–32]. After adjustment, the electron mobility and hole mobility of (110) are 0.9× and 1.3× of (100) [29], respectively. For areas that cause hybrid orientation, different sets of parameters are selected for simulation based on their spatial location, according to the nearest interface direction.

3. Results and Discussion

In this section, the effects of different cross-sectional shapes on the device characteristics are investigated. The Sentaurus TCAD is used to simulate the electrical characteristics of devices. I–V curves of all structures and significant electrical parameters are obtained. Here, the On-state current (I_{ON}) is calculated at V_{GS} = V_{DS} = 0.7 V, while the OFF-state current (I_{OFF}) is calculated at V_{GS} = 0 V and V_{DS} = 0.7 V [2]. The total gate capacitance (C_{gg} = $I_G \times \partial$ t/∂ V_{GS}, and the I_G is the gate displacement current under a time-dependent gate voltage) is calculated at V_G = 0.7 V and V_S = V_B = V_D = 0 V. A critical parameter that represents SCE is the drain-induced barrier lowering (DIBL), which can be calculated from the following equation [33,34]:

$$DIBL = \frac{V_{tlin} - V_{tsat}}{V_{Dsat} - V_{Dlin}} \quad (1)$$

The DIBL effect is related to the threshold voltage definition. Here, the threshold voltage (V_{th}) is extracted by the constant current method. The V_{tsat} is the threshold voltage

calculated in the saturation region (V_{tsat} = V_{GS} when the V_{DS} = V_{Dsat} = 0.7 V and the I_{DS} = 100 nA × W_{eff}/L_g), and V_{tlin} is the threshold voltage calculated in the linear region (V_{tlin} = V_{GS} when the V_{DS} = V_{Dlin} = 0.05 V and the I_{DS} = 100 nA × W_{eff}/L_g).

3.1. Inner Spacer

In previous TCAD simulations, the traditional rectangular inner spacer (RIS) is common [19–21], as shown in Figure 3a,b. However, a crescent inner spacer (CIS) can be formed due to the insufficient etching selectivity in the actual process [14–17], as shown in Figure 3c,d. To investigate how the non-ideal inner spacer cross-sectional shape impacts the performance of NSFET, the electrical characteristics of NSFET with RIS and CIS are simulated at different L_g. In this work, we change the L_g from 8 to 16 nm (meanwhile, the L_{sp} is changed from 7 to 3 nm), keeping the total length of the L_g plus the L_{sp} fixed.

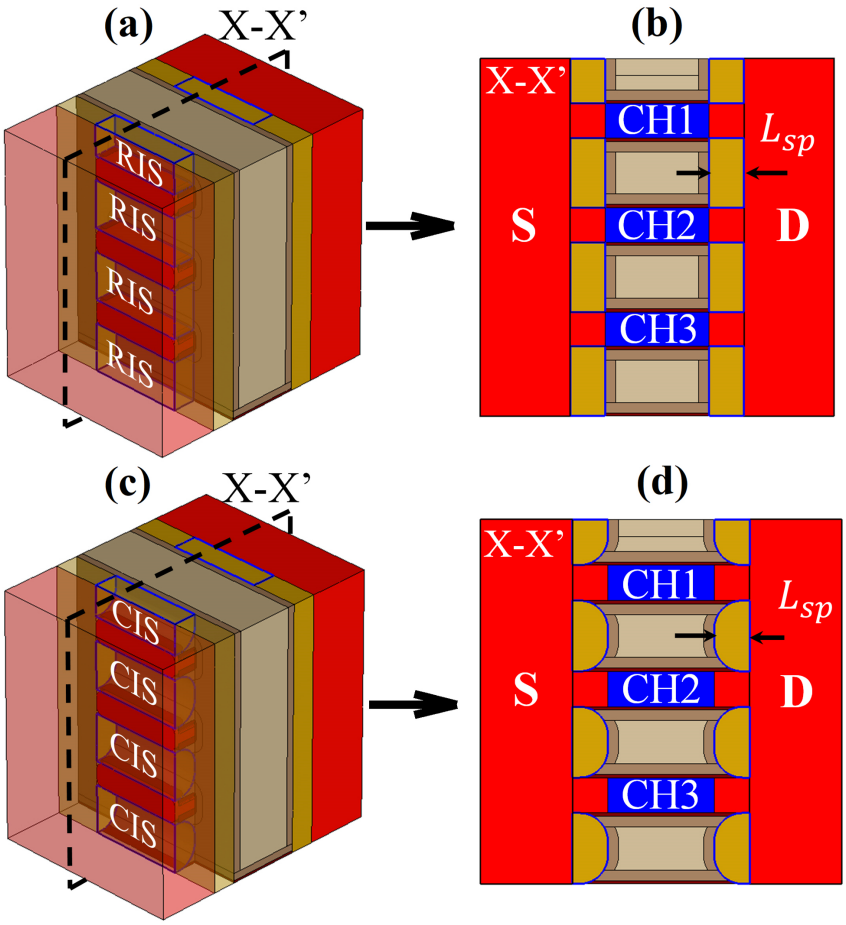

Figure 3. (**a**) 3-D structure, and (**b**) X-X′ view of the NSFET with Rectangular Inner Spacer (RIS). (**c**) 3-D structure, and (**d**) X-X′ view of the NSFET with Crescent Inner Spacer (CIS).

The comparison of the NSFET with a CIS and the NSFET with a RIS is analyzed under varying L_g, as shown in Figure 4. From Figure 4a, it is observed that the NSFET with a CIS has a higher I_{ON}/I_{OFF} ratio than NSFET with a RIS. The increased trend slows down with L_g increasing, showing improvements of 11.1%, 4.5%, and 2.4%, respectively. The I_{ON}/I_{OFF} ratio increases for NSFET with a CIS compared to NSFET with a RIS because the CIS improves the I_{ON} and decreases the I_{OFF}. Since the total length of the L_g plus the L_{sp} is fixed, the smaller is the L_g, the weaker is the gate control capability, leading to a significant difference in the impact of CIS on NSFETs under varying L_g. Figure 4b,c show that the subthreshold swing (SS) and drain-induced barrier lowering (DIBL) of the NSFET with a CIS are improved compared to the NSFET with a RIS. These results are consistent

with the short-channel effects improvement due to the CIS increasing the effective gate length [6]. It also can be seen that the CIS has a more significant effect on the SS and DIBL with the smaller L_g. The reason for the trend of SS is that the CIS has a more significant improvement in I_{ON}, with the L_g decreasing. For the trend of DIBL, the reason is that the CIS has a more significant enhancement in the gate control capability with the smaller L_g. As shown in Figure 4d, the NSFET with a CIS has a larger C_{gg} than the NSFET with a RIS. The phenomenon occurs because the CIS causes the high-k dielectric and gate to extend towards the junction region, increasing the outer-fringing field at the junction [Figure 5]. Then, the parasitic capacitance increases [22,23]. However, the C_{gg} variation caused by CIS increases due to the enhancement in the increased trend of the gate fringing electric field, with L_g increasing. Therefore, the non-ideal cross-sectional shape of the inner spacer has a significant impact on NSFET.

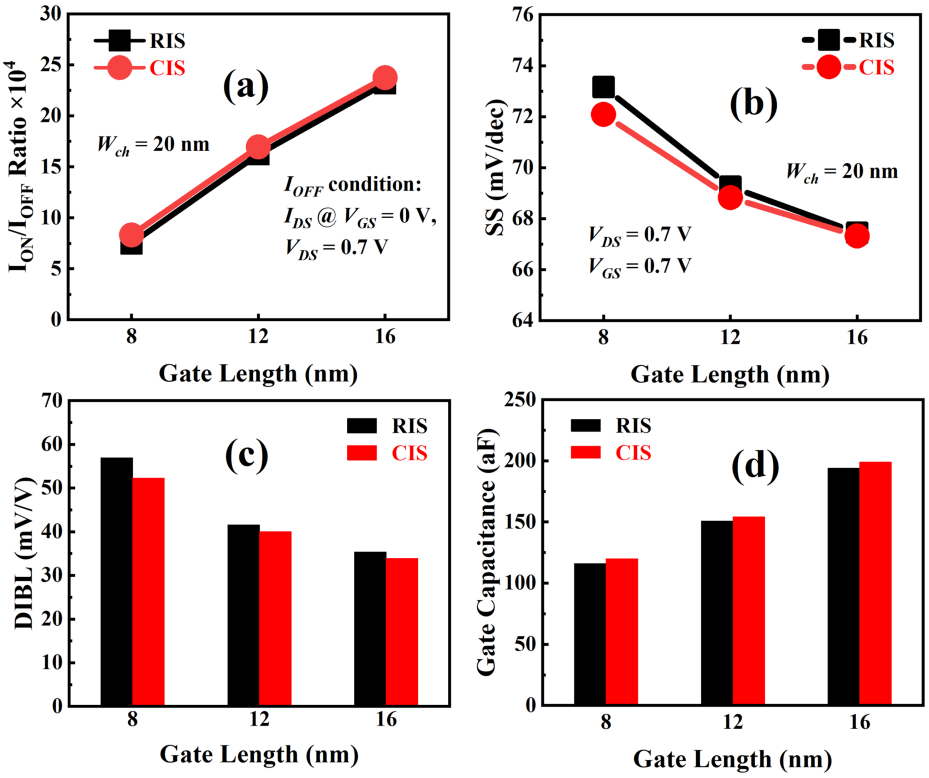

Figure 4. Trend of (**a**) I_{ON}/I_{OFF} ratio, (**b**) SS, (**c**) DIBL, and (**d**) C_{gg} of NSFET with a rectangular inner spacer compared with the NSFET with a crescent inner spacer under different L_g.

Moreover, many studies have demonstrated that the inner spacer material impacts the electrical characteristics of the NSFET [19,20]. We also studied the performance difference between CIS and RIS of various materials. Figure 6 displays the relevant simulation results. The NSFET with a CIS exhibits a higher I_{ON}/I_{OFF} ratio, smaller SS and DIBL, and larger C_{gg} for both SiO_2 and Si_3N_4. The results for HfO_2 are not quite the same as SiO_2 and Si_3N_4. The NSFET with a CIS has a degraded DIBL and smaller C_{gg}. This is because the coverage of HfO_2 layer of CIS is smaller than RIS, showing a lower outer fringing electric field. Therefore, the material also affects the effect of CIS on NSFET.

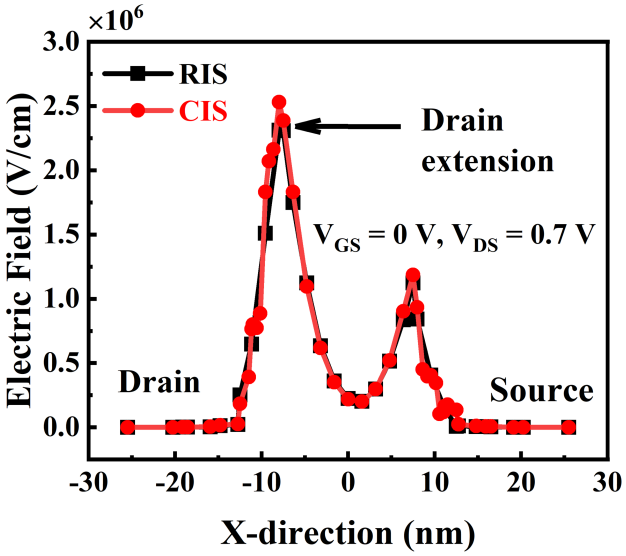

Figure 5. Electric field along the x-direction according to the cross-sectional shape of inner spacer when the V_{GS} = 0 V, the V_{DS} = 0.7, and the L_g = 12 nm.

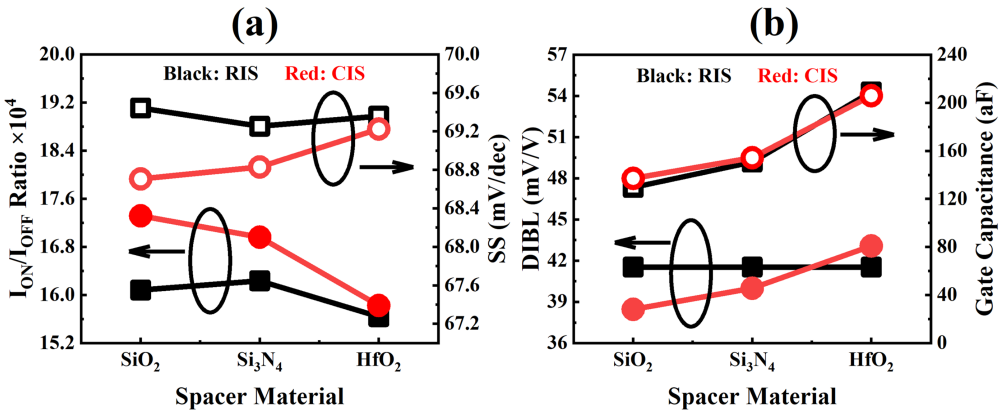

Figure 6. Comparison of (**a**) I_{ON}/I_{OFF} ratio and SS, (**b**) DIBL and C_{gg} between NSFET with a rectangular inner spacer and NSFET with a crescent inner spacer of different materials.

3.2. Stacked NS Channel

In the channel release process, the excessive etch can cause the loss of Si and form a tapered channel cross-sectional shape [28]. Figure 7a,b show the 3-D structure and X-X view of a 7-nm node NSFET with a tapered stacked NS channel cross-sectional shape, designed following the experimental work in [28]. Here, the rounding corner is introduced to reduce the corner effect of the device in the simulation. The parameter g is defined as the channel thickness (t_{ch}), and the parameter e represents the thickness of Si at the end of the channel. The ideal channel cross-sectional shape is indicated by e/g = 1.0. Figure 7c illustrates the I_{ON} and the I_{OFF} at varying e/g ratios when W_{ch} = 20 nm. It is shown that the non-ideal channel cross-sectional shape has a significant impact on NSFETs. As the e/g changes from 1.0 to 0.2, the I_{ON} and the I_{OFF} decrease from 193.8 to 132.8 µA and 1.22 to 0.3 nA, respectively, resulting in a reduction of 31.5% and 75.3%, respectively. This phenomenon occurs because the smaller is the e/g ratio, the larger is the loss of Si at the edge of the channel. Therefore, the device current decreases with a smaller e/g ratio due to the reduction in conduction area. In addition, the I_{OFF} due to SCEs is also reduced, resulting in a significant degradation in I_{OFF} than I_{ON}.

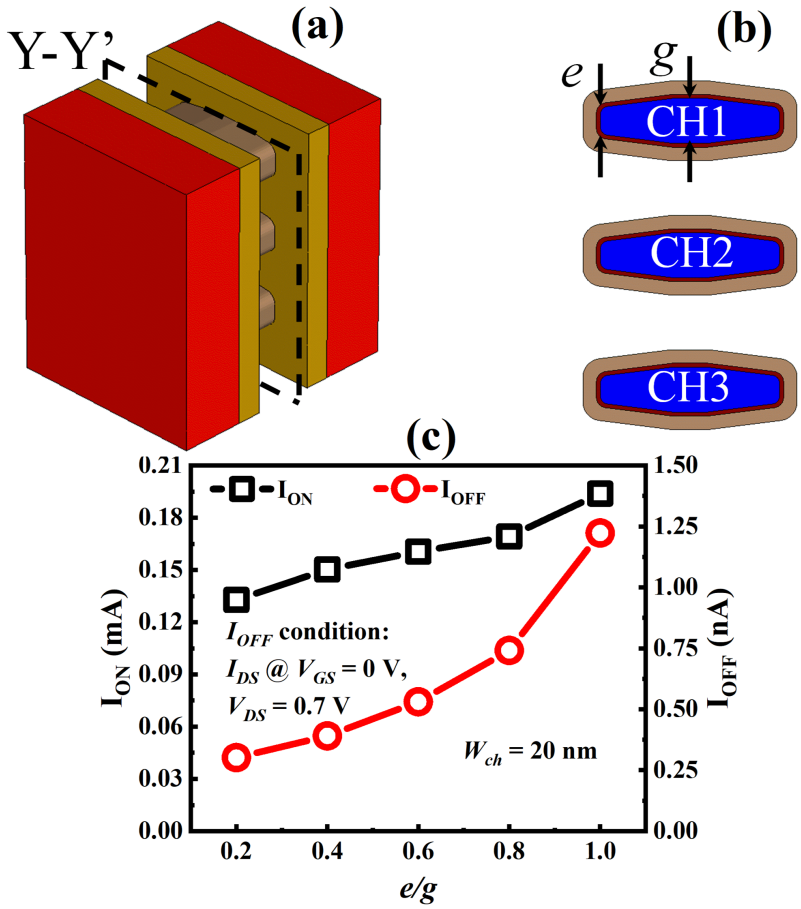

Figure 7. (**a**) 3-D structure, and (**b**) Y-Y′ view of the NSFET with a tapered channel cross-sectional shape. (**c**) drain current of NSFETs at varying e/g ratios when W_{ch} = 20 nm.

The non-ideal cross-sectional shapes are mainly formed in the initial stage of the etching process and do not vary with the etching time [16]. Therefore, the channel width (W_{ch}) also impacts the effect of the non-ideal channel cross-sectional shape on NSFET. Figure 8 shows the electrical characteristics of NSFETs with different e/g ratios at varying W_{ch} from 20 to 40 nm. Since the effective channel width (W_{eff}) is insensitive with the e/g ratio varying when the W_{ch} is large enough, the effect of the non-ideal channel cross-sectional shape on NSFETs becomes insignificant with the W_{ch} increasing. Figure 8a plots the I_{ON}/I_{OFF} ratio variation with NS width. It can be seen that the NSFET with a smaller e/g ratio provides a larger I_{ON}/I_{OFF} ratio at a fixed channel width. For example, the I_{ON}/I_{OFF} ratio with an e/g ratio of 0.2 is 177.7% higher than that of conventional NS when W_{ch} = 20 nm. This increased trend for I_{ON}/I_{OFF} can be explained by the fact that the I_{OFF} decreases faster than the I_{ON}, with the e/g falling. As the W_{ch} increases, the I_{ON}/I_{OFF} ratio with an e/g ratio of 0.2 decreases by 68.5% at W_{ch} = 40 nm compared with that at W_{ch} = 20 nm. This reduction in drain current can be explained by the trend of SS with W_{ch} varying, as shown in Figure 8b. As the W_{ch} increases, the I_{ON} increases slightly due to the increase in SS, while the I_{OFF} increases due to the enlargement in the conduction area. The SS and DIBL are improved with a smaller e/g ratio, as shown in Figure 8b. These improvements are because the short-channel effects (SCEs) can be alleviated by reducing the channel width [35]. Figure 8c shows that the threshold voltage (V_{th}) of the tapered NS is increased by 16.6% over that of the conventional NS due to the lower I_{ON}. The conduction area increases with W_{ch} increasing. So, the increase of W_{ch} would result in a reduction in the threshold voltage. Figure 8d indicates that the NSFET with conventional stacked NS channels presents a larger maximum transconductance ($g_{m,max}$) value than the tapered NS channel. This is because the former has a larger W_{eff}. Therefore, the tapered NS improves

the SCEs but sacrifices the driving current, resulting in an improvement in I_{ON}/I_{OFF} ratio, SS, and DIBL, but a degradation in V_{th} and $g_{m,max}$.

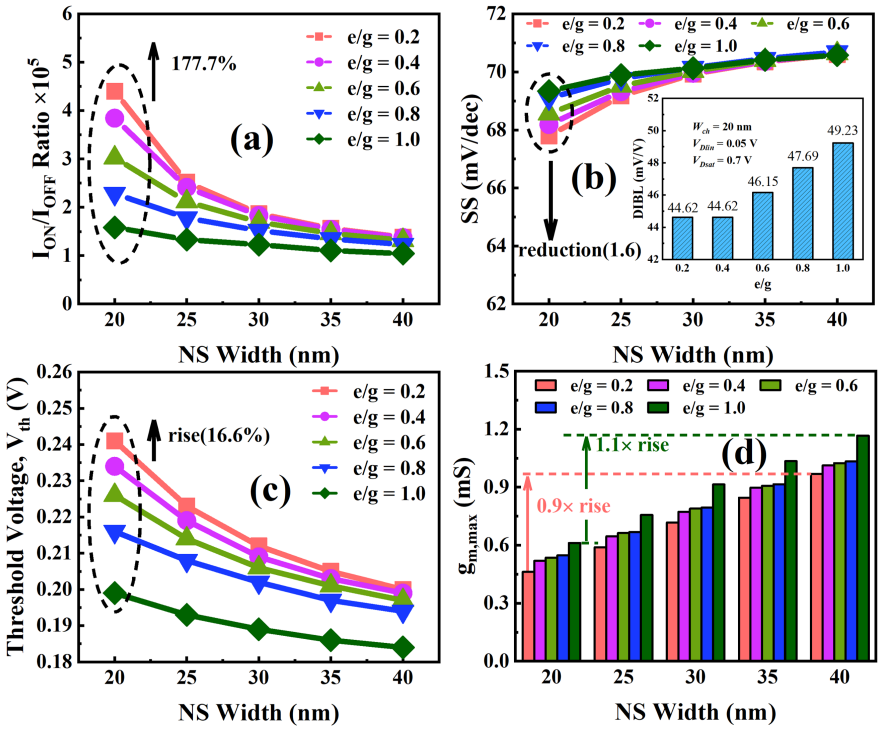

Figure 8. Trend of (**a**) I_{ON}/I_{OFF} ratio, (**b**) SS, (**c**) DIBL and, (**d**) $g_{m,max}$ of NSFETs with different e/g ratios considering different NS width (W_{ch}).

3.3. Fin-Shaped IB Channel

The TreeFET structure is proposed to balance the electron and hole mobilities for CMOS devices [31]. It also enhances the device current compared to NSFET [29–32]. However, the presence of the IB significantly impacts TreeFET performance due to the insufficient etching selectivity. In order to investigate how the non-ideal cross-sectional shapes impact the TreeFET performance, we designed similar cross-sectional shapes based on the cross-sectional shapes given by the existing experimental results in [31], as illustrated in Figure 8. The 3-D scheme and the ideal Y-Y′ view of the TreeFET are depicted in Figure 9a,b. The height of IB (HIB) is 20 nm, and the width of IB (WIB) is 5 nm. The rest of the relevant parameters are consistent with the NSFETs listed in Table 1.

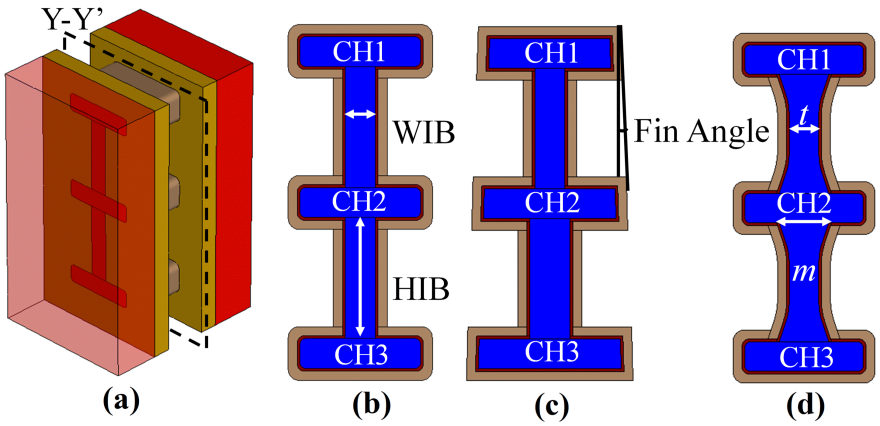

Figure 9. (**a**) 3-D view, and (**b**) ideal Y-Y′ view of TreeFET. (**c**) Y-Y′ view of TreeFET considering fin angle. (**d**) Y-Y′ view of TreeFET with concave arc IB

Two factors will result in a non-ideal channel cross-sectional shape of the TreeFET. The first factor is that the fin angle can cause the W_{ch} and WIB at the bottom to be wider than that at the top, as shown in Figure 9c. Here, the top width of CH1 for all schemes is fixed at 20 nm, while the rest widths of channels vary with the fin angle from 0° to 4°. A fin angle of 0° represents the conventional cross-sectional shape. The second factor is that the insufficient etch can form a concave arc IB during the channel release, as shown in Figure 9d. In this case, the IB can be wider near the NS. Here, the parameter m is defined as the width of IB at the intersection, whereas the parameter t represents the ideal width of IB. The t/m = 1.0 is the ideal cross-sectional shape. To accurately analyze the effect of the corresponding factor on TreeFET performance, in this work, we discussed the two factors separately.

Figure 10 shows the influence of the above two factors on TreeFET performance at different WIB. As expected, the I_{ON}/I_{OFF} ratio, SS, and DIBL all deteriorate with WIB increasing. The two non-ideal factors have a more significant impact on electrical characteristics as the WIB increases. These results are because the gate control capability degrades with WIB increasing [3].

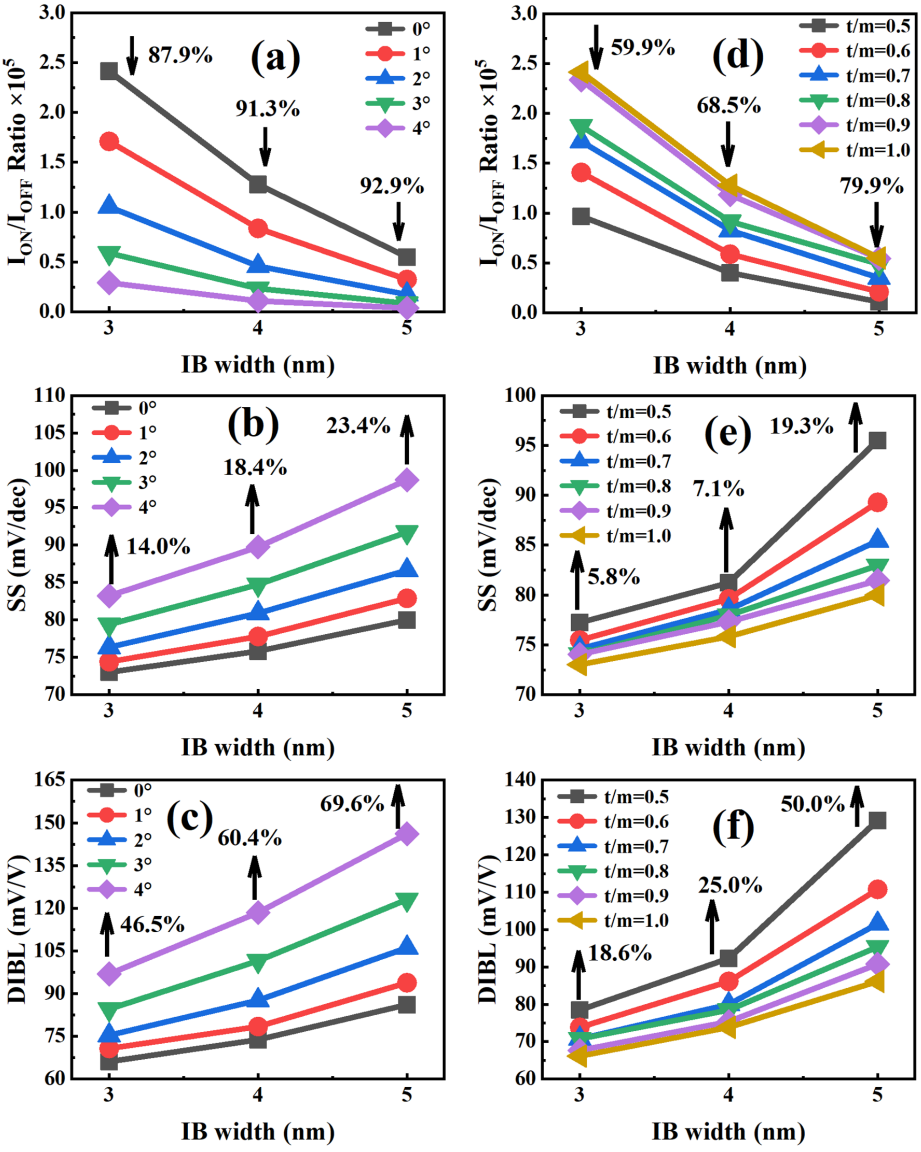

Figure 10. The influence of fin angle on (**a**) I_{ON}/I_{OFF} ratio, (**b**) SS and (**c**) DIBL at varying IB width. The effect of concave arc IB on (**d**) I_{ON}/I_{OFF} ratio, (**e**) SS and (**f**) DIBL at different IB width.

As the fin angle increases, the W_{ch} and WIB increase, increasing the device current. However, the I_{OFF} rises faster than the I_{ON}. So, the I_{ON}/I_{OFF} ratio decreases as the fin angle changes from 0° to 4°, reaching 92.9% at WIB = 5 nm, as shown in Figure 10a. The larger W_{ch} can degrade the electrostatic control behavior [6]. Also, the larger WIB reduces the gate control capability due to the smaller area-volume ratio of the channel region [3]. As shown in Figure 10b,c, these two cooperative phenomena eventually lead to the SS and DIBL all deteriorating as the fin angle varies from 0° to 4°, with the degradation reaching 23.4% and 69.6%, respectively, at WIB = 5 nm. Therefore, due to the rapid decrease in gate control capability, the fin angle increases from 0° to 4°, SCEs degradation is severe compared to the conventional TreeFET.

The smaller t/m is, the wider is the IB near NS, causing the current conduction area to increase. In this case, both I_{ON} and I_{OFF} increase, but I_{OFF} rises dramatically, leading to a 79.9% decrease in the I_{ON}/I_{OFF} ratio at WIB = 5 nm, as shown in Figure 10d. As t/m decreases, SS and DIBL degrade by 19.3% and 50.0%, respectively, at WIB = 5 nm, as illustrated in Figure 10e,f. This is because the gate is further away from the intersection due to the wider IB near the NS, which reduces the gate control capability [30]. Therefore, the concave arc IB also causes a severe degradation in gate control capability. For the TreeFET with a concave arc IB, the I_{ON}/I_{OFF} ratio, SS, and DIBL all deteriorate compared to the conventional TreeFET.

4. Conclusions

In this article, the effects of non-ideal cross-sectional shapes of the inner spacer (IS), nanosheet (NS), and inter-bridge (IB) are investigated. The results show that the geometry and material of the inner spacer have significant effects on the performance of the NSFET. Compared with the rectangular inner spacer (RIS), the low-k crescent inner spacer (CIS) enhances the gate control capability while the high-k CIS degrades the drain-induced barrier lowering ($DIBL$) and reduces the gate capacitance (C_{gg}). When the e/g = 0.2 and W_{ch} = 20 nm, the tapered NS shows the best on/off current ratio (I_{ON}/I_{OFF}) with 177.7% improvement while increasing the threshold voltage by 16.6% over the rectangular NS. The TreeFET considering the fin angle and concave arc IB can degrade the gate control capability, and the SCEs degradation is severe compared to the ideal structure. When WIB = 5 nm, the degradation of I_{ON}/I_{OFF}, SS, and $DIBL$ can reach 92.9%, 23.4%, and 69.6%, respectively, with fin angle increasing; The degradation of I_{ON}/I_{OFF}, SS, and $DIBL$ can reach 79.9%, 19.3%, and 50.0%, respectively, with the t/m increasing. Moreover, the relevant parameters of each structure are well investigated, and the results show that the non-ideal cross-sectional shapes significantly impact device performance under smaller gate length (L_g), narrower NS width (W_{ch}), and wider IB width (WIB). To reduce the effect of non-ideal cross-sectional shapes on performance, geometry parameters including L_g, W_{ch}, and WIB should be set reasonably. Therefore, the detailed TCAD simulation results show that the non-ideal cross-sectional shapes should be considered to accurately determine the device's electrical performance.

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