electronics

MDPI

Article

Impacts of Floating Poly on Electrostatic Discharge Protection of Power-Managed High-Voltage Laterally Diffused Metal Oxide Semiconductor Components

Xing-Chen Mai, Shen-Li Chen *, Hung-Wei Chen and Yi-Mu Lee

Department of Electronic Engineering, National United University, Miaoli City 36063, Taiwan; jonshon0000@gmail.com (X.-C.M.); hwchen@nuu.edu.tw (H.-W.C.); ymlee@nuu.edu.tw (Y.-M.L.)
* Correspondence: jackchen@nuu.edu.tw; Tel.: +886-37-382525

Abstract: This study used a TSMC 0.18 μm 50 V process to build a high-voltage n-LDMOS structure. In the reference device, the number of floating poly (poly-2) turns was 7, and the width and spacing of each turn was 1 μm. The experiment was realized in three steps, i.e., fixing the number of laps by occupying the width of the structure, adjusting the width of each turn, and adjusting the distance between turns. The first step was fixed to occupy the width of the structure chart to adjust the number of turns. The number of turns increased from 7 to 9 and then decreased to 5 and 3 turns. The reduction in the number of turns resulted in a greater reduction in maximum electric field and an increase in breakdown voltage. A comparison of the 3-turn set with the reference set showed a 42% reduction in maximum electric field, from 4.17×10^3 to 2.46×10^3 (V/cm), and an increase in breakdown voltage (V_{BK}) from 30.2 V to 35.84 V. The second step was to adjust the width of each turn from 1 to 1.4, 1.2, 0.8, and 0.6 μm. This increase in width reduced the maximum electric field, resulting in a greater increase in V_{BK}. When the width was increased to 1.4 μm, the maximum field decreased from 1.95×10^3 V/cm to 1.4×10^3 V/cm and the V_{BK} increased from 30.2 V to 85.6 V, an increase of 183%. The third step was to adjust the per-turn spacing of the reference group from 1 to 1.4, 1.2, 0.8, and 0.6 μm. When the spacing was reduced to 0.6 μm, the maximum electric field decreased by 33% from 1.95×10^3 to 1.32×10^3 V/cm and the V_{BK} increased by 345% from 30.2 to 134.4 V.

Keywords: breakdown voltage; electric field; floating poly; lattice temperature; n-LDMOS

check for updates

Citation: Mai, X.-C.; Chen, S.-L.; Chen, H.-W.; Lee, Y.-M. Impacts of Floating Poly on Electrostatic Discharge Protection of Power-Managed High-Voltage Laterally Diffused Metal Oxide Semiconductor Components. *Electronics* **2023**, *12*, 2803. https://doi.org/10.3390/electronics12132803

Academic Editor: Yahya M. Meziani

Received: 12 May 2023
Revised: 21 June 2023
Accepted: 22 June 2023
Published: 25 June 2023

Copyright: © 2023 by the authors. Licensee MDPI, Basel, Switzerland. This article is an open access article distributed under the terms and conditions of the Creative Commons Attribution (CC BY) license (https://creativecommons.org/licenses/by/4.0/).

1. Introduction

In a rapidly evolving world, the demand for smaller chip sizes and higher performance is increasing. However, the protection circuitry of the chip can pose a serious problem. In order to reduce the chip size, the gate length is reduced and the gate oxide layer is thinned, which makes it easy for the current to break through. Therefore, the protection components need a higher breakdown voltage to protect the components they need to protect. In addition, today's electronic products are expected to have higher performance and faster transmission speed but this also increases the internal temperature and electric field values of the components. These values, which increase with demand, can be fatal to the components. Therefore, an attempt was made to design a protection element that would increase the breakdown voltage and reduce the electric field value. Electrostatic discharge (ESD) [1–7] can occur because of excessive transient currents, which can be caused by the switching on and off of a power supply, the incomplete grounding of a machine, or human contact with an integrated circuit (IC) through human grounding (i.e., the Human Body Model). Notably, ESD can also irreversibly damage an IC. To effectively prevent ESD, specific components for power supplies and protective components for automotive electronics can be designed, and such components require advanced and improved ESD protection.

In the present study, Silvaco T-CAD Atlas software 5.34.0.R [8–11] was used to perform n-LDMOS modulation simulations. The plate effect [12–17] was employed to arrange a floating poly [17–19] on the oxide layer (STI). The design was intended to take advantage of the field-saka effect to increase the breakdown voltage (VBK) while reducing the maximum electric field. In the first part, how the concentration of the field plate affects the protection ability was determined by increasing the number of turns by fixing the width of the floating poly (poly-2) on the structure picture. The second part increased and decreased the width of each turn of the floating poly on the structural drawing, so that the effect of increasing or decreasing the width on the protection ability can be determined. In the third part, the spacing between the turns of the floating poly on the structure diagram was adjusted to determine the effect on the protection capability if the turns are separated with no change in conditions. Three types of modulation were used to determine whether the plate effect substantially changed the components by lowering their electric fields and increasing their V_{BK}.

2. Device Structure

2.1. The Reference Device

Figure 1 presents the structure of the reference group of components used in the present study. As indicated in the structural and layout views, the current flows from the inner drain side to the source side and bulk side, and because the ESD discharge events are all two-pin events, we connected the bulk side, source side, and gate side and grounded them to form a grounded-gate n-channel metal oxide semiconductor. In the structure, the high-voltage n-well, high-voltage p-well, and N^+ formed a parasitic bipolar junction transistor (BJT) in the internal circuit, and we used this BJT as a discharge current path for discharging ESD currents. This component for the I/O PAD was designed to protect the internal component circuit when an ESD event occurs and to promptly discharge the ESD current to prevent damage to the main circuit. The high-voltage n-well forms a resistance in the drift region such that the components can operate in a high-voltage environment. The DPW (Deep P Well) forms a double RESURF structure in the component to reduce the maximum electric field and on-state resistance of the component. STI (shallow trench isolation) prevents current leakage between adjacent semiconductor device components. RPO (Resist Protect Oxide) is used to block the formation of silicide on the nitride. It is used to avoid ESD currents from flowing over the nitride surface and posing any threat to the gate oxide. Next, a poly-2 was used to create a field plate effect above the drift region to distribute the internal electric field evenly, thereby reducing the peak electric field in the drift region and increasing the breakdown voltage. The N-type buried layer structure (NBL layer) forms an equivalent reverse diode with the p-sub below it to prevent the excessive leakage of current to the p-sub and to prevent component failure.

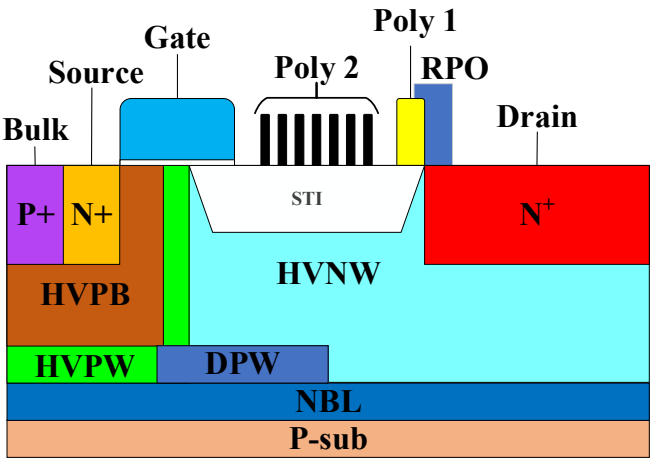


Figure 1. Cross-sectional view of the high voltage nLDMOS reference device.

2.2. Field-Plate Effect

In the reference group, we used a floating poly to create a field plate effect in the component. This approach was employed to control the magnitude of the surface electric field by applying a bias to the field plate. When we applied a positive bias to the field plate, the depletion zone extended along the surface toward the edge of the field plate, which reduced the concentration effect of the original electric field and further increased the V_{BK}.

Two common field plate structures were used. The first was a field plate connected to an electrode (i.e., the contact field plate; Figure 2). The second was a floating field plate placed independently above the STI (Figure 3).

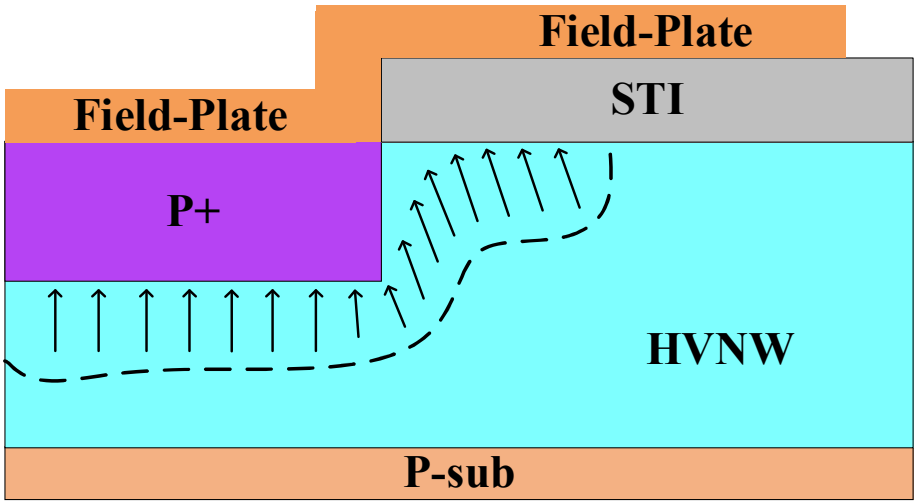


Figure 2. Field plate structure with a continuous field plate.

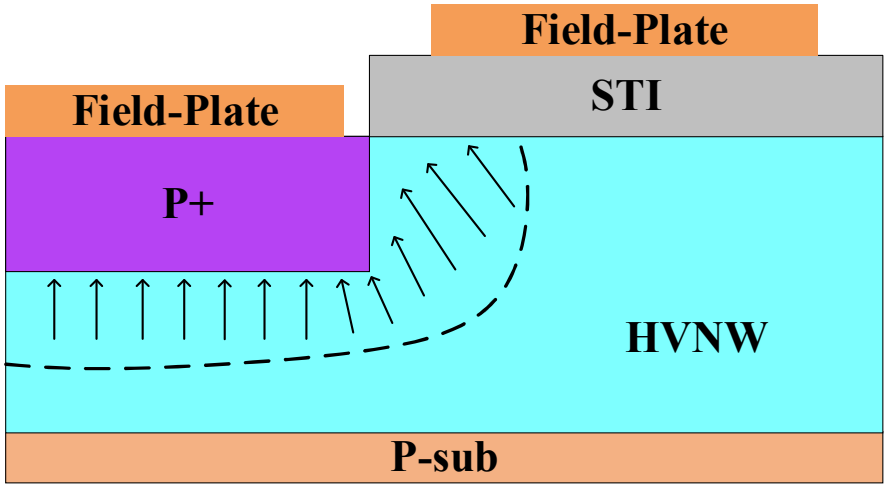


Figure 3. Field plate structure with a floating field plate.

2.3. Device Modulation Engineering

2.3.1. Fixed Area of Turns

We fixed the area occupied by the floating poly and the distance between turns to analyze the effect of the number of turns on the maximum field and V_{BK}. Because the reference group (Ref) was a 7-turn floating poly, we increased the number of turns to 9 (S1_9R) and reduced the number of turns to 5 (S1_5R) and 3 (S1_3R) to fix the area occupied by the floating poly such that the width of each group of turns was different. The width was 0.77 µm for 9R [Figure 4a], 1 µm for Ref (Figure 1), 1.4 µm for 5R [Figure 4b], and 2.33 µm for 3R [Figure 4c].

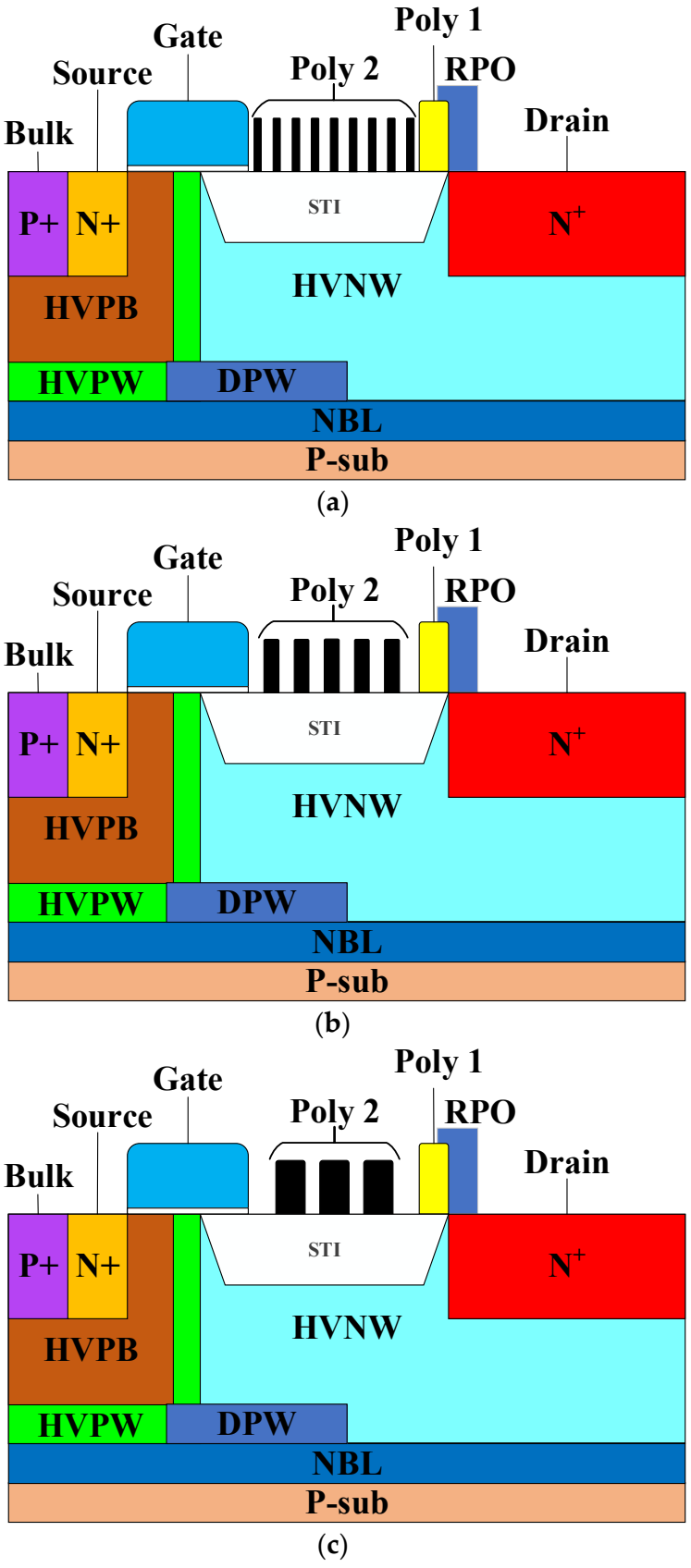


Figure 4. Cross-sectional views of the high-voltage nLDMOS (**a**) S1_9R, (**b**) S1_5R, and (**c**) S1_3R devices.

2.3.2. Adjust Width of Each Turn

In this section, the width of each turn of the floating poly was adjusted, and the width of each turn of the reference group was 1 µm. During testing, the width of each turn was increased to 1.2 (S2_1.2) and 1.4 (S2_1.4) microns, while the width of the structure diagram occupied by each turn was increased to 8.4 and 9.8 microns, respectively. Figure 5a presents the structure formed when the width was increased to 1.4 µm. We also reduced the width to 0.8 (S2_0.8) and 0.6 (S2_0.6) µm to reduce the area occupied to 5.6 and 4.2 µm, respectively. Figure 5b presents the structure formed when the width was reduced to 0.6 µm. This experiment was performed to clarify how the area occupied by the floating poly affected the electric field value and V_{BK}.

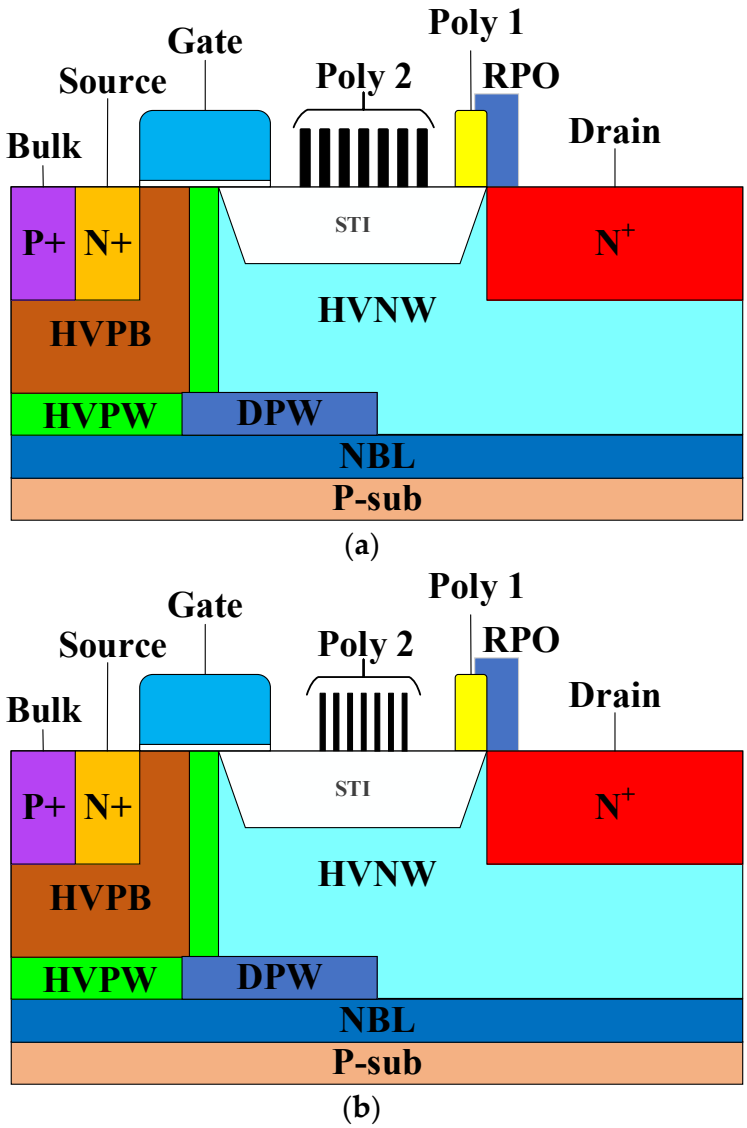


Figure 5. Cross-sectional views of the high-voltage nLDMOS (**a**) S2_1.4 and (**b**) S2_0.6 devices.

2.3.3. Adjusting the Spacing between Turns

In this section, the spacing of each turn of the floating poly was adjusted, and the spacing of each turn of the reference group was 1 µm. In the experiment, the spacing of each turn was increased to 1.2 (S3_1.2) and 1.4 (S3_1.4) µm and reduced to 0.8 (S3_0.8) and 0.6 (S3_0.6) µm. Figure 6a,b present the structure formed when the spacing was increased to 1.4 and 0.6 µm, respectively. This experiment was performed to clarify how increasing or decreasing the pitch of each turn of the floating poly affected the electric field value and V_{BK}.

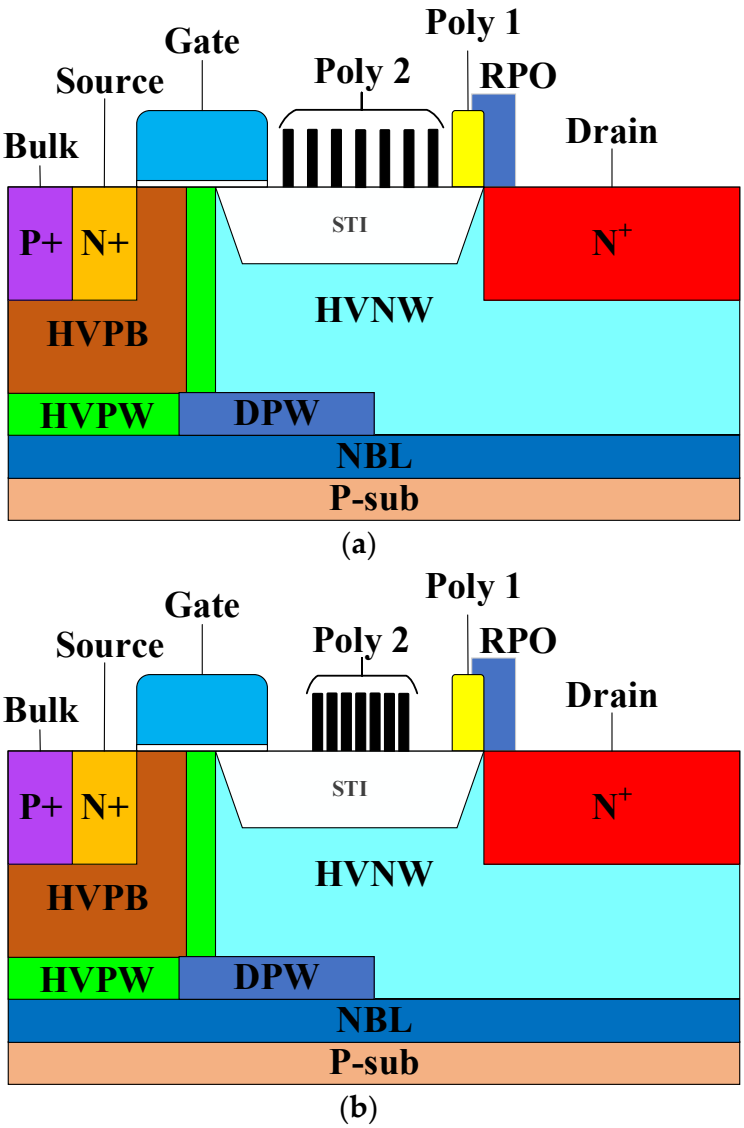


Figure 6. Cross-sectional views of the high-voltage nLDMOS (**a**) S3_1.4 and (**b**) S3_0.6 devices.

3. Results and Discussion

3.1. Fixed Area of Turns

Group 1 samples (S1) pertain to the adjustment of the number of turns of the fixed area; previous studies have focused on directly reducing or increasing the number of turns and have reported that a greater number of turns results in a stronger field plate effect. However, this finding indicates the presence of two variables, and whether the stronger field plate effect was due to an increase in the occupied area or the number of turns is unclear. Therefore, in the present experiment, the area occupied by the sum of the turns was fixed to exclude the effect of changing the area occupied and to clarify the effect of changing the number of turns on ESD capability. Table 1 presents the data for the S1 injection current 1×10^{-4} (A). The table reveals that the trigger voltage (V_{t1}) tended to increase when the number of turns was reduced; this occurred because we used the field plate effect to reduce the strength of the electric field in the channel, which made it more difficult for components to conduct electricity and caused V_{t1} to increase. Figure 7 presents the V_{t1} and V_{BK} trends of the S1 samples. S1_3R (i.e., fewest number of turns) had the highest V_{t1} of 146.6 V, and S1_9R had the lowest V_{t1} of 50.8 V. When the V_{t1} increased, the V_{BK} also increased, with the highest and lowest V_{BK} of 69.9 and 30.2 V being achieved with S1_3R and S1_9R,

respectively. The lattice temperature floated at 725 K, indicating that changing the number of turns did not cause the lattice temperature to change.

Table 1. Device data of the S1 samples with the injection current 1E-4A.

S1_Samples	V_{t1} (V)	I_{t2} (A)	Star EF (V/cm)	Lattice Temp (K)	Breakdown (V)
S1_3R	146.6	1.36	2.46×10^3	725	66.9
S1_5R	92.3	1.43	4.02×10^3	726	55.2
S1_7R	61.2	1.47	4.17×10^3	725	42.8
S1_9R	50.8	1.54	7.46×10^3	725	30.2

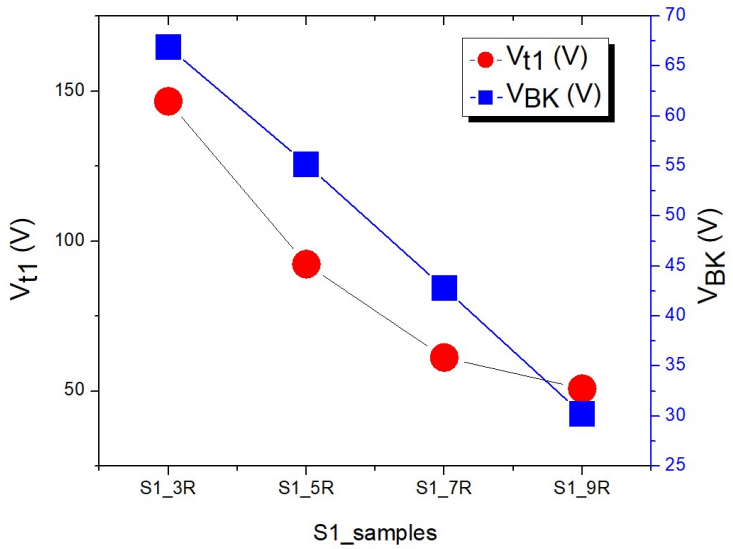


Figure 7. S1 trend graphs of V_{t1} and V_{bk} values.

In this work, an accurate measurement of the maximum electric field value of the metal oxide semiconductor could not be obtained because of the field plate effect. Therefore, we obtained a sample at the center of the channel under the STI layer and placed a star marker at 22.8 on the *X*-axis to compare the field strengths. Figure 8 presents the trend for the S1 star point EF between the groups, and the results revealed that the lowest star point EF value of 2.46×10^3 V/cm was obtained when the number of turns was reduced to three (S1_3R). Relative to the 3-turn star point EF, the 5-turn (S1_5R) star point EF increased slightly to 4.02×10^3 (V/cm). When the number of turns was increased to nine (S1_9R), the highest star point EF of 7.46×10^3 V/cm was obtained. These simulation data reveal that when the occupied area was fixed, reducing the number of turns reduced the field value.

3.2. Adjust Width of Each Turn

Group 2 samples (S2) pertain to the width adjustments for each turn. In contrast to the previous section, where the area occupied was fixed, the number of turns was fixed in S2 to clarify how increasing the occupied area affected the ESD components. Table 2 presents the data for the S2 injection current 1E-4A. The table reveals that the V_{t1} increased when the turn width was increased. This likely occurred because an increase in the area occupied created a stronger field plate effect, which made it more difficult for the components to conduct electricity and caused the V_{t1} to increase. The V_{t1} was 89.8 V at the widest width of 1.4 µm (S2_1.4). The V_{t1} of the reference group was 57.94 V when the width was 1 µm (S2_ref); this value differed from that of the reference group in the previous section. This could have occurred because increasing the width to 1.4 µm caused overlapping with the poly-1 layer to the right. Thus, shifting the floating poly to the left by 1 µm caused the value of the reference group to deviate. When the width decreased to 0.6 µm (S2_0.6), the V_{t1} also decreased to 31.4 V. The V_{BK} also changed when the V_{t1} changed. When the width

was 1.4 μm (S2_1.4), the V_{BK} was 85.5 V, and the V_{t1} of the reference group (S2_ref) was 30.2 V. At the narrowest width of 0.6 μm (S2_0.6), the V_{t1} decreased to only 8.7 V. Figure 9 presents V_{t1} and V_{BK} trends of the S2 for each device when the lattice temperature was maintained at 725 K. Furthermore, the lattice temperature was not affected by adjustments to the width of the aforementioned section.

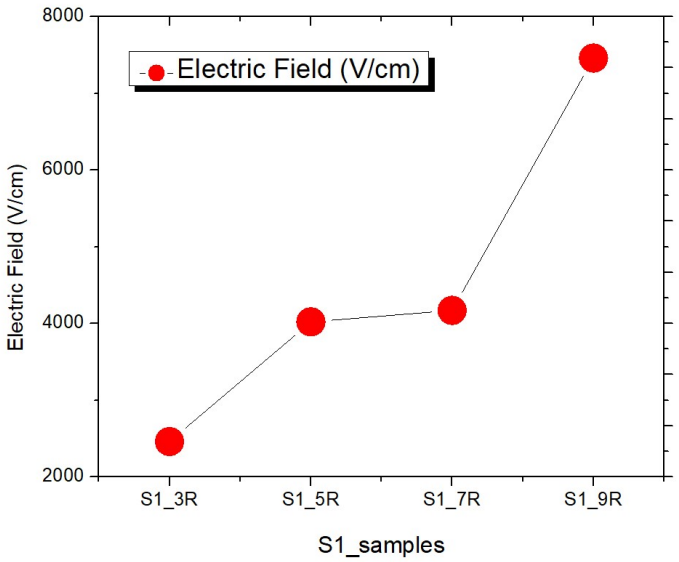


Figure 8. S1 star point EF trend between related devices.

Table 2. Device data of the S2 samples with the injection current 1E-4A.

S2_Samples	V_{t1} (V)	I_{t2} (A)	Star EF (V/cm)	Lattice Temp (K)	Breakdown (V)
S2_0.6	31.4	1.45	4.12×10^3	725	8.7
S2_0.8	40.3	1.46	2.48×10^3	725	29.3
S2_ref	57.94	1.4	1.95×10^3	725	30.2
S2_1.2	61.24	1.53	1.8×10^3	725	40.5
S2_1.4	89.8	1.55	1.4×10^3	725	85.5

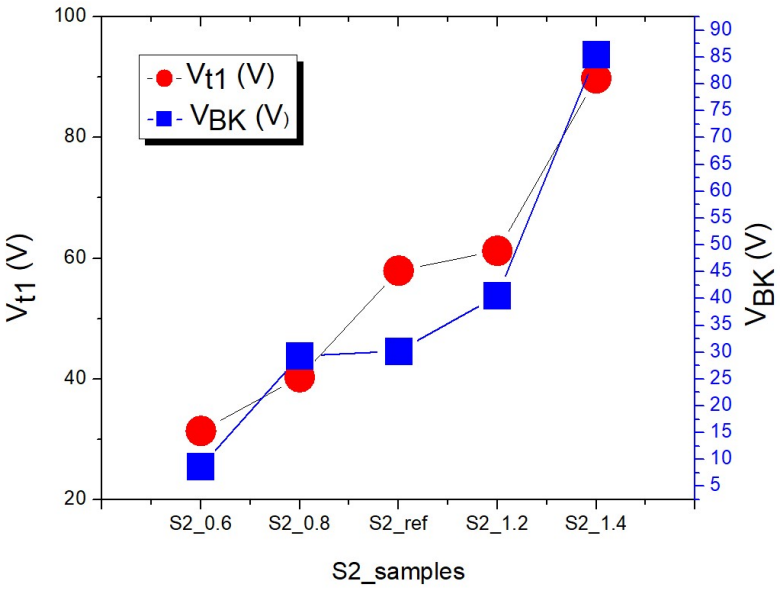


Figure 9. S2 trend graphs of V_{t1} and V_{bk} values.

The collected data indicated that the electric field started to weaken when the width increased and the star point EF of the reference group (S2_ref) was 1.95 × 10^3 V/cm. After the width was reduced, the star point EF was 4.12 × 10^3 V/cm at the smallest width of 0.6 µm (S2_0.6). The star point EF was 2.48 × 10^3 V/cm for S2_0.8. The star point EF of S2_1.2 was 1.8 × 10^3 V/cm at the widest width of 1.2 µm (S2_1.2). The star point EF at the widest width of 1.4 µm (S2_1.4) was 1.4 × 10^3 V/cm. Figure 10 presents the star point EF comparison of S2 samples.

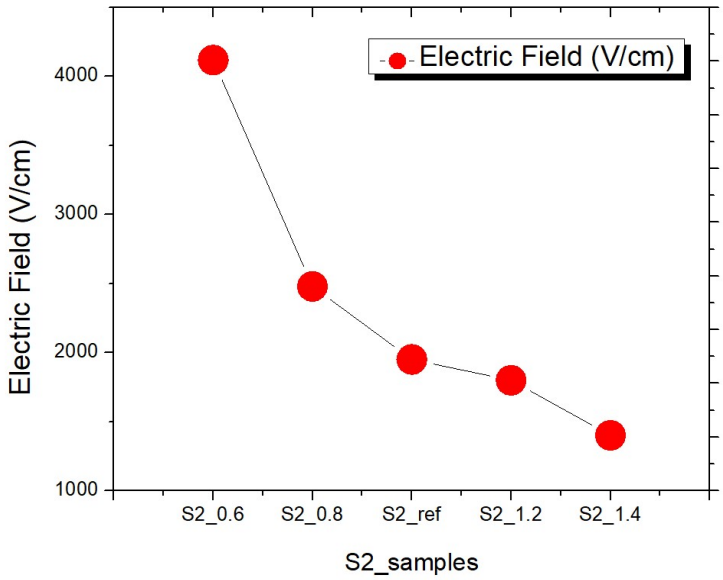


Figure 10. S3 Star point EF trend between these related devices.

3.3. Adjusting the Spacing between Turns

This subsection group pertains to adjustments of the spacing between turns and the width of each turn after the width of each turn was fixed. Table 3 presents the data for the S3 samples with the injection current 1E-4A. By observing the V_{t1}, we determined whether reducing the spacing would lead to an increase in the V_{t1}. Figure 11 presents a comparison of the trends between the V_{t1} and V_{BK} of the groups in S3. When the spacing was reduced to 0.6 µm (S3_0.6), the V_{t1} increased to 158.4 V. When the spacing was 1 µm (S3_ref), the V_{t1} was 57.94 V, which is identical to the V_{t1} in the reference group (discussed in the previous subsection) when the spacing and width were both 1 µm. When the spacing was increased to 1.4 µm (S3_1.4), the V_{t1} decreased to 31.4 V. The V_{BK} and V_{t1} followed the same trend; that is, with a minimum spacing of 0.6 µm (S3_0.6), the V_{BK} was 134.4 V [reference group (S3_ref) V_{BK} = 30.2 V], and with a maximum spacing of 1.4 µm (S3_1.4), the V_{BK} was 8.7 V. Similar to the findings for the V_{t1}, the V_{BK} increased and decreased when the spacing was reduced and increased, respectively, with the lowest value being 8.7 V. The lattice temperature was not affected by changes in the floating poly; this finding is supported by those of the previous subsections.

Table 3. Device data of the S3 samples with the injection current 1E-4A.

S3_Samples	V_{t1} (V)	I_{t2} (A)	Star EF (V/cm)	Lattice Temp (K)	Breakdown (V)
S3_0.6	158.4	1	1.54 × 10^3	725	134.4
S3_0.8	72.14	1	1.65 × 10^3	725	55.8
S3_ref	57.94	1.4	1.95 × 10^3	725	30.2
S3_1.2	41.3	1.42	2.65 × 10^3	725	19.6
S3_1.4	31.4	1.50	3.42 × 10^3	724	8.7

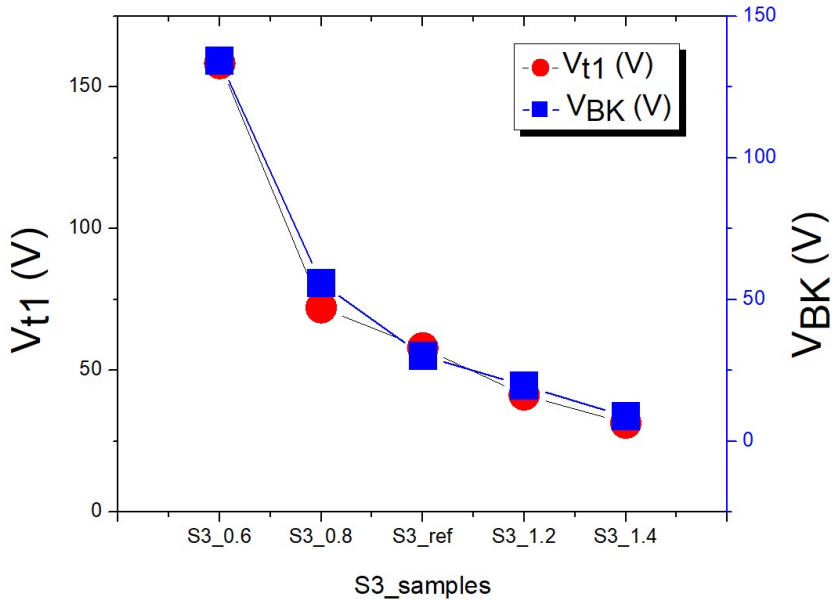


Figure 11. S3 trend graphs of V_{t1} and V_{bk} values.

With respect to the electric field values, the reference group (S3_ref) produced a 1.95×10^3-V/cm electric field, which corresponds to the values reported in the previous subsection, and reducing the pitch caused the electric field to weaken. With a pitch of 0.6 µm (S3_0.6), the star point EF was 1.54×10^3 V/cm. With a spacing of 0.8 µm (S3_0.8), the star point EF was 1.65×10^3 V/cm. When the spacing was increased, the electric field increased in strength. With a spacing of 1.2 µm (S3_1.2), the star point EF was 2.56×10^3 V/cm. With a spacing of 1.4 µm (S3_1.4), the star point EF was 3.42×10^3 V/cm. Figure 12 presents the star point EF comparison of the S3 samples, which reveals that an increase in the spacing reduced the field effect, resulting in higher field values and lower V_{BK} values.

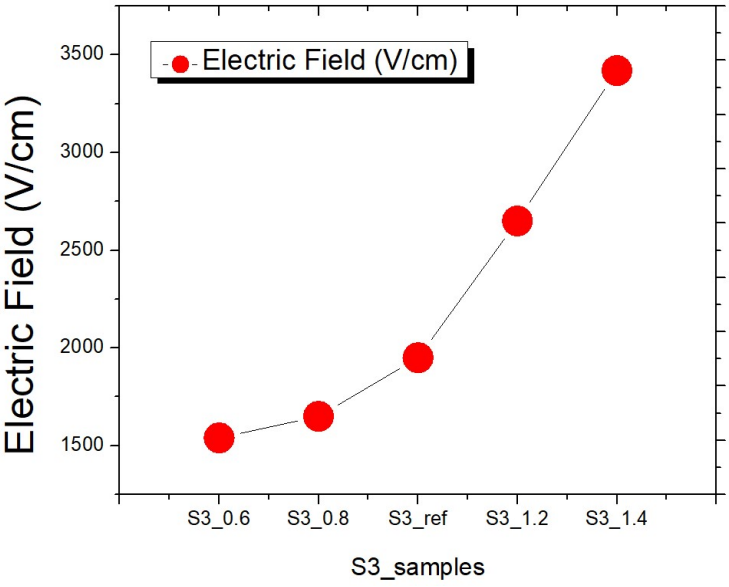


Figure 12. S3 star point EF trend between related devices.

3.4. Comparison of Electric Field Values by Different Groups

This work intended to reduce the electric field in the channel by adjusting it with a floating poly. It is generally accepted that the higher the number of turns, the more significant the reduction of the field. The conditions can be subdivided into the total area

occupied by the floating poly, the number of turns, or the width and spacing of the turns, all of which may affect the protection capacity. In S1 (fixed area of turns), we fixed the occupied area, increased the number of turns, and organized the EF field distribution to produce Figure 13. However, it can also be seen that the width of the circles increased as the number decreased.

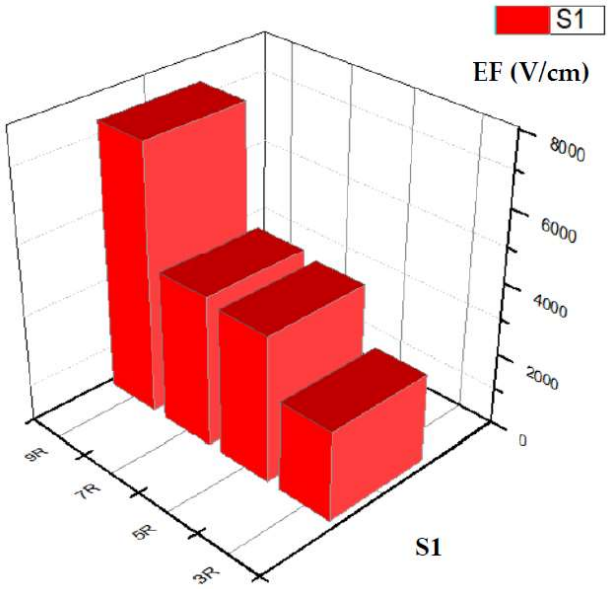


Figure 13. S1 electric field (EF) values in the channel.

Therefore, we have fixed the number of turns for S2 and S3 to investigate the effect of width and pitch on the protection capability. The EF field values for S2 (width adjustment) and S3 (pitch adjustment) are plotted in Figure 14, which shows that the wider the width, the lower the field, and the greater the pitch, the higher the field. Therefore, the higher the width of the protection element and the lower the spacing, the greater the reduction in the electric field (EF) value.

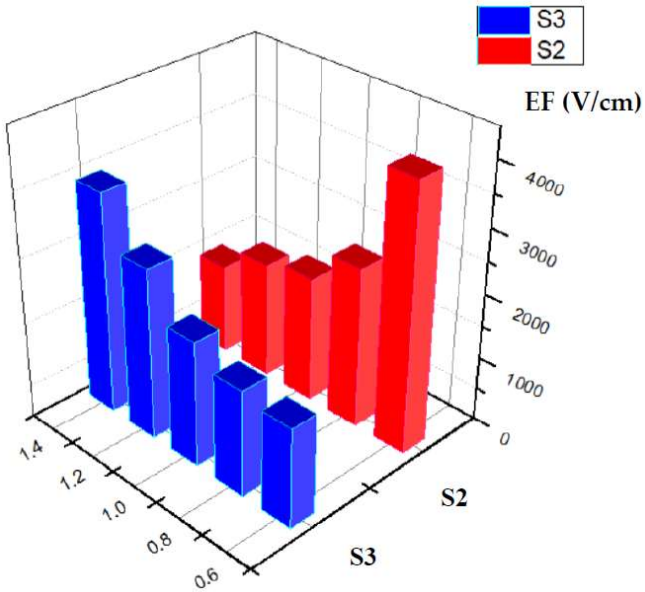


Figure 14. S2 and S3 electric field (EF) values in the channel.

4. Conclusions

The focus of this study was on floating aggregation. In the S1 group, we fixed the occupied area and adjusted the number of turns to analyze how changing the number

of turns with a fixed overall occupied area affects the ESD protection capability of the component. It was found that with the maximum number of turns of nine (S1_9R), the VBK was 30.2 V and the field at the channel center (star point EF) was 7.46 $\times$ 10^3 (V/cm). With the minimum number of turns of three (S1_3R), the VBK was 66.9 V and the star point EF was 2.46 $\times$ 10^3 (V/cm). The VBK increased by 121% and the field decreased by 33%. The best results for ESD protection elements were obtained when the number of turns was three (S1_3R) and the turn width was high. In the S2 group, the number of turns was fixed and the width of each turn was varied to clarify how the variation in width affects the area occupied on the component. When the width was 1.0 microns (S2_ref), VBK was 30.2 V and the star point EF was 1.95 $\times$ 10^3 (V/cm). At a width of 0.6 μm (S2_0.6), the VBK was 8.7 V and the star point EF was 4.12$\times$ 10^3 (V/cm). The VBK was 71% lower and the electric field 111% higher than the reference group. When the width was increased to 1.4 μm (S2_1.4), the VBK of the reference group increases by 283% to 85.5 V and the field value decreases by 29% to 1.4$\times$ 10^3 (V/cm). Therefore, increasing the width of each turn increases the strength of the field effect and enhances the ESD protection of the components. In the S3 group, the number of turns and width were fixed and the spacing between each turn was adjusted to determine how the distance between the field plates affects the ESD capability of the components. When the spacing was reduced to 0.6 microns (S3_0.6), the VBK of 134.4 V increased by 445% and the star point EF of 1.54$\times$ 10^3 (V/cm) decreased by 33%. When we increased the spacing to 1.4 microns (S3_1.4), the VBK of 8.7 V decreased by 72% and the star point EF of 3.42 $\times$ 10^3 (V/cm) increased by 75%. Thus, the further apart the field plate effect is, the weaker it becomes.

In summary, the field plate effect increases the level of floating aggregates. When the area occupied by each turn is reduced, the width of each turn increases and when the spacing between turns is reduced, the field plate effect is enhanced. These findings suggest that reducing the value of the electric field in the channel or increasing the VBK can lead to components exhibiting better anti-static properties.

Author Contributions: X.-C.M. performed the chip layout, implementation, the experimental works, and the manuscript writing; S.-L.C. contributed to the research idea, data verification and the paper revision; H.-W.C. performed the data analysis; Y.-M.L. contributed to evaluation of the DUTs. All authors have read and agreed to the published version of the manuscript.

Funding: This research received no external funding.

Data Availability Statement: Data is contained within the article.

Conflicts of Interest: The authors declare no conflict of interest.

References

1. Liu, J.; Liu, Y.; Han, A.; Nie, Y.Q.; Huang, Q.; Liu, Z. A Novel Voltage Divider Trigger SCR with Low Leakage Current for Low-Voltage ESD Application. *IEEE Trans. Electron Devices* **2022**, *69*, 2534–2542. [CrossRef]
2. Do, K.-I.; Song, B.-B.; Koo, Y.-S. A Gate-Grounded NMOS-Based Dual-Directional ESD Protection with High Holding Voltage for 12V Application. *IEEE Trans. Device Mater. Reliab.* **2020**, *20*, 716–722. [CrossRef]
3. Lai, D.-W.; Sque, S.; Peters, W.; Smedes, T. Gate-Lifted nMOS ESD Protection Device Triggered by a p-n-p in Series with a Diode. *IEEE Trans. Electron Devices* **2019**, *66*, 1642–1647. [CrossRef]
4. Lee, J.-H.; Prabhu, M.; Natarajan, M.I. Engineering ESD Robust LDMOS SCR Devices in FinFET Technology. *IEEE Electron Device Lett.* **2018**, *39*, 1011–1013. [CrossRef]
5. Huang, C.-Y.; Chiu, F.-C.; Ou, C.-M.; Chen, Q.-K.; Huang, Y.-J.; Tseng, J.-C. ESD and Latchup Optimization of an Embedded-Floating-pMOS SCR-Incorporated BJT. *IEEE Trans. Electron Devices* **2016**, *63*, 3036–3043.
6. Lin, C.-Y.; Chang, P.-H.; Chang, R.-K. Improving ESD Robustness of pMOS Device with Embedded SCR in 28-nm High- k/Metal Gate CMOS Process. *IEEE Trans. Electron Devices* **2015**, *62*, 1349–1352. [CrossRef]
7. Wu, C.-H.; Lee, J.-H.; Lien, C. A Novel Drain Design for ESD Improvement of UHV-LDMOS. *IEEE Trans. Electron Devices* **2015**, *62*, 4135–4138. [CrossRef]
8. Hasan, T.; Zafar, S.; Ozbay, E.U.; Kashif, A. Analysis of HfO_2 and ZrO_2 as High-K Dielectric for CMOS Nano Devices. In Proceedings of the 2022 9th International Conference on Electrical and Electronics Engineering (ICEEE), Alanya, Turkey, 29–31 March 2022; pp. 99–103.

9. Khadir, A.; Kouzou, A.K.; Abdelhafidi, M. Effect of Anti-Reflective Coating on CIGS Solar Cells Performance. In Proceedings of the 2020 17th International Multi-Conference on Systems, Signals & Devices (SSD), Monastir, Tunisia, 20–23 July 2020; pp. 621–625.
10. Dutta, R.; Tamang, T.; Paul, P.; Paitya, N. Comparative Study of AlGaN/GaN, InAlN/GaN and AlGaAs/GaAs based High Electron Mobilty Transistors Using Silvaco for High-Frequency Applications. In Proceedings of the 2020 4th International Conference on Trends in Electronics and Informatics (ICOEI) (48184), Tirunelveli, India, 16–18 April 2020; pp. 137–142.
11. Li, S.; Tian, Y.; Wei, J.; Liu, S.; Sun, W. Electrical parameters shifts of 1.2 kV 4H-SiC MOSFET under cosmic radiations. In Proceedings of the 2017 IEEE 24th International Symposium on the Physical and Failure Analysis of Integrated Circuits (IPFA), Chengdu, China, 4–7 July 2017; pp. 1–4.
12. Wang, R.; Qiao, M.; Wang, Y.; Li, Z.; Zhang, B. Novel High-Tolerance Termination With Resistive Field Plate for 600 V Super-Junction Vertical Double-Diffused MOSFET. *IEEE Electron Device Lett.* **2022**, *43*, 1093–1096. [CrossRef]
13. Duan, B.; Xue, S.; Huang, X.; Yang, Y. Novel Si/SiC Heterojunction Lateral Double-Diffused Metal Oxide Semiconductor With SIPOS Field Plate by Simulation Study. *IEEE J. Electron Devices Soc.* **2021**, *9*, 114–120. [CrossRef]
14. Zhen, Z.; Feng, C.; Wang, Q.; Niu, D.; Wang, X.; Tan, M. Single Event Burnout Hardening of Enhancement Mode HEMTs With Double Field Plates. *IEEE Trans. Nucl. Sci.* **2021**, *68*, 2358–2366. [CrossRef]
15. Kilpi, O.-P.; Andrić, S.; Svensson, J.; Ram, M.S.; Lind, E.; Wernersson, L.-E. Increased Breakdown Voltage in Vertical Heterostructure III-V Nanowire MOSFETs With a Field Plate. *IEEE Electron Device Lett.* **2021**, *42*, 1596–1598. [CrossRef]
16. Liu, H.; Xue, Z.; Li, S.; Li, Q.; He, D.; Xia, T.; Guo, J. Characteristics of partial discharge in oil-paper insulated needle plate electrode model under composite AC-DC voltage. *CSEE J. Power Energy Syst.* **2020**, *6*, 848–857.
17. Zhang, W.; Ye, L.; Fang, D.; Qiao, M.; Xiao, K.; He, B.; Li, Z.; Zhang, B. Model and Experiments of Small-Size Vertical Devices With Field Plate. *IEEE Trans. Electron Devices* **2019**, *66*, 1416–1421. [CrossRef]
18. Jiang, W.; Scott, R.; Deen, M.J. Improved Noise Performance of CMOS Poly Gate Single-Photon Avalanche Diodes. *IEEE Photonics J.* **2022**, *14*, 6802208. [CrossRef]
19. Melde, T.; Trentzsch, M.; Duenkel, S.; Richter, R.; Otto, M.; Giesler, H.; Weisbuch, F.; Weddeler, N.; Beyer, S. Novel embedded single poly floating gate flash demonstrated in 22 nm FDSOI technology. In Proceedings of the 2021 IEEE International Memory Workshop (IMW), Dresden, Germany, 16–19 May 2021; pp. 1–4.

Disclaimer/Publisher's Note: The statements, opinions and data contained in all publications are solely those of the individual author(s) and contributor(s) and not of MDPI and/or the editor(s). MDPI and/or the editor(s) disclaim responsibility for any injury to people or property resulting from any ideas, methods, instructions or products referred to in the content.