



Communication A Novel 4H–SiC/Si Heterojunction IGBT Achieving Low Turn–Off Loss

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Abstract: In this paper, a novel silicon carbide (SiC) insulated gate bipolar transistor (IGBT) with a 4H–SiC/Si heterojunction in the buffer layer (HBL) is proposed to improve the turn–off characteristic. Compared with the conventional 4H–SiC IGBT, the polysilicon region is integrated in the buffer layer to form a natural potential well, which can help to store excess carriers in the turn–off process. The simulation results indicate that the turn–off time (t_{off}) was reduced from 325 ns to 232 ns, and the turn–off loss (E_{off}) was decreased from 2.619 mJ to 1.375 mJ, while a similar on–state ability was maintained. This means that reductions of 28.6% in t_{off} and 47.5% in E_{off} were achieved. The E_{off} of the two devices at different forward voltages (V_F) was compared by changing the carrier lifetime. As a result, a better trade–off between E_{off} and V_F was also achieved by the proposed HBL–IGBT. Moreover, the heterojunction of the HBL–IGBT can be formed with the plasma–activated direct bonding technology, which is compatible with the conventional fabrication process.

Keywords: silicon carbide; IGBT; forward voltage drop; turn-off loss; heterojunction

1. Introduction

In recent years, with the development of science and technology, people are paying more attention to environmental issues. The concepts of green energy and carbon neutrality not only promote the development of power electronic technology, but also improve the performance requirements of power electronic devices [1]. However, silicon has approached its theoretical limits. Therefore, third-generation semiconductor materials represented by SiC and GaN are being considered to meet the demands of future high-voltage and high-power devices, and are expected to replace silicon (Si) devices in the high-voltage field, such as photovoltaic (PV) power generation, multi-electric aircraft, electric transmission, and hybrid electric vehicles [2]. GaN materials are mainly used in low-voltage and high-frequency-power devices such as radio frequency devices. Thus, SiC materials have more extensive applications in the high-voltage field. SiC materials have been used in the design of various power devices such as IGBTs (insulated gate bipolar transistors, IGBTs), MOSFETs (metal-oxide-semiconductor field-effect transistors, MOSFETs), BJTs (bipolar junction transistors, BJTs), and JBSs (junction barrier Schottky diodes, JBSs), due to their excellent physical properties including a wider bandgap, higher electron saturation rate, higher critical breakdown electric field and better thermal conductivity [3–6]. However, there are still many problems to be explored and solved. For example, some SiC devices are affected by barrier height inhomogeneities and low mobility caused by interface states [7,8]. On the one hand, some researchers propose to improve the performance of SiC devices by improving SiC materials [9]. On the other hand, some researchers propose to improve device parameters to obtain a better performance. Among the various power devices, SiC



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Copyright: © 2023 by the authors. Licensee MDPI, Basel, Switzerland. This article is an open access article distributed under the terms and conditions of the Creative Commons Attribution (CC BY) license (https:// creativecommons.org/licenses/by/ 4.0/). IGBTs are valued for their excellent trade–off performance between the I-V characteristic, blocking characteristic and dynamic characteristic. SiC IGBTs benefit from the advantages of MOSFETs and BJTs to achieve a strong blocking ability and low on–resistance (R_{on}). Thus, SiC IGBTs are suitable for application in smart grids and green energy generation for high–voltage application requirements [10–16].

Since Edward Van Brunt et al. fabricated the 27 kV SiC IGBT [17], one of the biggest obstacles for practical application has been the improvement of the dynamic performance [18]. The main problem of the switching characteristic is that excess carriers exiting in part of the drift region and the buffer layer suppress the extension of the depletion layer. Therefore, most researchers propose some novel structures introducing a conduction method to extract excess carriers [19–22], which effectively decreases t_{off} and E_{off} . However, there exists another way to extract excess carriers by enhancing the recombination rate, which has been discussed less.

In this paper, a novel SiC IGBT structure with a SiC/Si heterojunction in the buffer layer is proposed using the Synopsys Sentaurus Technology Aided Design (TCAD) simulation software [23]. In this structure, the carrier in silicon carbide is more inclined to flow into polysilicon, because the band gap of polysilicon is much smaller than that of silicon carbide. Meanwhile, the recombination rate is improved because of the smaller bandgap and higher carrier concentration in polysilicon. As a result, enhanced recombination and storage of excess carriers can be achieved within the polysilicon (polySi) region to effectively improve the turn-off characteristic while maintaining a similar on-state characteristic.

2. Device Structure and Working Mechanism

Figure 1 shows the schematic structures of a conventional IGBT (C–IGBT) and the proposed IGBT with a SiC/Si heterojunction in the buffer layer (HBL–IGBT). The parameters of both structures are provided in Table 1. The main structure parameters are the same, except for the heterojunction in the buffer layer. It is noted that three ion implantation operations are used to form a retrograde P–well, which can receive a better channel electron mobility to improve the forward voltage drop and suppress the depletion of the P–well/N–drift junction to obtain a better blocking characteristic. The electron lifetime of SiC is set to 2.5 μ s, and the hole lifetime of SiC is set to 0.5 μ s. The channel length is set to 1 μ m, causing a channel electron mobility of 46 cm²/(V×s) and a hole mobility of 7 cm²/(V×s).



Figure 1. Schematic structures of (a) C–IGBT and (b) HBL–IGBT.

Parameters	C-IGBT	HBL–IGBT
Cell pitch (µm)	15	15
Active area (mm ²)	16	16
P+ collector depth (μ m)	5	5
P+ collector doping (cm $^{-3}$)	$1 imes 10^{19}$	$1 imes 10^{19}$
Gate oxide thickness (nm)	60	60
N–CSL doping (cm ⁻³)	$8 imes 10^{15}$	$8 imes 10^{15}$
N-CSL thickness (µm)	2	2
N-drift thickness (µm)	110	110
N–drift doping (cm ⁻³)	$4 imes 10^{14}$	$4 imes 10^{14}$
N-buffer thickness (µm)	2.5	2.5
N-buffer doping (cm ⁻³)	$2 imes 10^{17}$	$2 imes 10^{17}$
N+ polysilicon doping (cm^{-3})		$1 imes 10^{19}$
Trench heterojunction thickness (µm)		0.5
Trench heterojunction width (μm)		0.5

Table 1. Detailed structure parameters of the two SiC IGBTs.

Figure 2 shows the main process flows of the HBL–IGBT. The top and down structures of the HBL–IGBT can be received. First, the top structure can grow from the N+ substrate, and the MOSFET structure of the top side is formed via ion implantation. Then, the extra N+ substrate is removed via chemical mechanical polishing (CMP). Similarly, the down structure grows from the N+ substrate. A layer of SiO₂ grows as a masking layer, and the trench can be received through a lithography operation. Then, polysilicon can be formed via chemical vapor deposition (CVD). SiO₂ and extra silicon are removed via chemical mechanical polishing (CMP). Finally, the heterojunction can be formed via plasma–activated direct bonding [24,25].



Figure 2. Main fabrication steps of the HBL-IGBT structure.

The thickness and width of the polySi region are denoted by T_{Si} and W_{Si} , respectively. The turn–off time (t_{off}) is considered as the time from 90% V_{GE} to 10% I_{CE} . The time corresponding to 90% V_{GE} is denoted by t_1 , and the time corresponding to 10% I_{CE} is denoted by t_2 . The t_{off} is described as

$$t_{\rm off} = t_2 - t_1 \tag{1}$$

The trade–off curve of the optimization of W_{Si} and T_{Si} between t_{off} and the V_F of a 10 A current can be seen in Figure 3. The higher V_F corresponded to a worse conduction loss. From Figure 3, with increasing W_{Si} , the V_F monotonically increased, but the t_{off} decreased.

Meanwhile, the higher T_{Si} also caused a worse V_F and a better t_{off} when the W_{Si} was constant. It is obvious that the device performance was influenced by the polySi material parameters, because the energy bandgap of silicon is 1.12 eV, which is about one third of that of silicon carbide (3.24 eV). Thus, holes from the P+ collector and electrons from the N–drift layer can easily flood into polySi, which increases the resistance and weakens the conductivity modulation. As a result, the forward characteristic degenerates for a wider W_{Si} and thicker T_{Si} . At the same time, a wider W_{Si} and thicker T_{Si} could store more carriers when turning off, and the narrower bandgap allows excess carriers to recombine more easily compared with silicon carbide, which can restrain the current tail and provide a better t_{off} and E_{off} . Therefore, increasing T_{Si} and W_{Si} leads to a better turn–off characteristic. It is more beneficial to optimize polySi, which can restrain the current tail and provide a better t_{off} and E_{off} . The optimization dimensions adopted for W_{Si} and T_{Si} were 0.5 µm and 0.5 µm, which are appropriate sizes for etching and photolithography selection. Meanwhile, better trade–off results between the t_{off} and V_F also can be achieved, as shown in Figure 3.



Figure 3. The optimization of T_{Si} and W_{Si} between the V_F and t_{off} of the HBL–IGBT.

The *I*–*V*, blocking, and turn–off characteristics of the two structures were simulated using the Synopsys Sentaurus Technology Aided Design (TCAD) software. The key physical models for SiC power devices were adopted [26], including the Shockley–Read–Hall (SRH) model, Auger recombination model (AUGER), carrier speed saturation model (high–field saturation), incomplete ionization model, and mobility model (Lombardi). To validate the accuracy of the models used in the simulation, a structure consistent with the parameters in [27] was established, which indicated a good fitting result of the *I*–*V* curves, as shown in Figure 4.



Figure 4. Comparison of the on-state characteristics of the SiC IGBT simulation and measurement.

Moreover, a heterojunction interface carrier transport model was introduced because of the discontinuity in the energy band of the SiC/Si interface. The boundary conditions at the heterointerface are given by

$$J_{n,\mathrm{Si}} = v_n q (n_{Si} - n_{SiC} \exp(\frac{\Delta E_C}{kT}))$$
⁽²⁾

$$J_{p,\text{Si}} = v_p q \left(p_{Si} - p_{SiC} \exp(\frac{\Delta E_V}{kT}) \right)$$
(3)

where $J_{n,Si}$ is the electron current density entering polysilicon, which is equal to that leaving SiC; $J_{p,Si}$ is the hole current density entering polysilicon, which is equal to that leaving SiC; ΔE_C is the difference between the conduction bands of the two materials; ΔE_V is the difference between the valence bands of the two materials.

3. Simulation Results and Discussion

Figure 5a illustrates the forward *I*–*V* characteristics of the C–IGBT and HBL–IGBT. It was found that the V_F of C–IGBT was 4.81 V, and that of the HBL–IGBT was 5.35 V, where the HBL–IGBT exhibited a slightly higher V_F . The reason is that the polySi region stores a part of the holes from the P+ collector, which reduces the hole concentration of the drift layer, as shown in Figure 5b. It can be seen that the hole concentration of the HBL–IGBT in the drift region was lower than that of the C–IGBT, resulting in degradation of the conductivity modulation.



Figure 5. Two structures of the (a) simulated on–state curve and (b) hole concentration in the cutline in the center of the cell.

Figure 6 presents the blocking characteristic of the C–IGBT and HBL–IGBT. The breakdown voltage of both structures approached 16 kV because of the identical parameters of the N–drift and CSL layers. Furthermore, the insert figure shows the electric field distribution of the two structures at the breakdown voltage, which shows a similar electric field distribution. The maximum electric fields in the gate oxide of the HBL–IGBT and C–IGBT were 3.31 MV/cm and 3.28 MV/cm, which are acceptable for long–term gate oxide reliability [28].



Figure 6. Breakdown characteristic curves and electric fields of (a) C–IGBT and (b) HBL–IGBT.

The turn–off performance of the two structures was investigated with a double–pulsed circuit, as shown in the insert of Figure 7. The bus voltage was 5 kV. The gate resistor was 10 Ω , and the gate voltage switched from 20 to 0 V. The load inductance, stray inductance, and parasitic capacitance were 3 mH, 20 nH, and 30 pF, respectively.

Figure 7 shows the simulated turn–off curves of the two structures. The turn–off loss (E_{off}) is considered as the global energy during the turn–off process. The turn–off loss is described by the following equation:

$$E_{\rm off} = \int_{t_1}^{t_2} V_{CE} \times I_{CE} \times dt \tag{4}$$



Figure 7. Comparison of turn-off curves between C-IGBT and HBL-IGBT.

It can be seen that the t_{off} of the HBL–IGBT and C–IGBT was 232 ns and 325 ns, respectively. This indicates an improvement of 28.6% in the t_{off} . The E_{off} was reduced from 2.619 mJ for the C–IGBT to 1.375 mJ for the HBL–IGBT, with a reduction of about 47.5%. The main reason is that the excess carriers can flood into the polySi region due to a natural potential well in the SiC/Si heterojunction, as shown in Figure 8, resulting in an increasing carrier concentration in the polySi region. A high carrier concentration and a narrow bandgap allow electrons and holes to combine more easily, resulting in a lower t_{off} and E_{off} .



Figure 8. Comparison of energy band diagrams between HBL–IGBT and C–IGBT with the cutline in the center of the cell.

Figure 9 shows the distribution of the electron concentration of the C–IGBT and HBL–IGBT at the cutline along with the center of the device cell during the turn–off process every 60 ns steps. It can be seen that the electron concentration of the HBL–IGBT in the drift layer nearly reduced to 1×10^{-6} cm⁻³ at 240 ns, while the electron concentration of the

C–IGBT stored in the drift layer remained at about 1×10^9 cm⁻³ at 300 ns. Furthermore, the maximum electron concentration was about 7×10^{18} cm⁻³ for the HBL–IGBT and 1×10^{17} cm⁻³ for the C–IGBT at 300 ns. This indicates that the huge electrons of the C–IGBT are kept in the drift layer and buffer layer, while the electrons flood into the polySi region in the HBL–IGBT during the turn–off process.



Figure 9. The distribution of the electron concentration during the turn-off process.

Figure 10 shows the distribution of holes during the turn–off process. It is easy to see that the hole concentration in the drift layer of the HBL–IGBT was about 1×10^{10} cm⁻³ at 300 ns, which was three orders of magnitude lower than that of the C–IGBT (1×10^{13} cm⁻³). The highest hole concentration of the HBL–IGBT was about 3×10^{18} cm⁻³. In the same position, that of the C–IGBT was about 8×10^{15} cm⁻³. Moreover, the average hole concentration of the HBL–IGBT in the drift layer was about 10^{11} cm⁻³ at 240 ns, which was much lower than that of the C–IGBT. It can be concluded that the holes accumulated in polySi in the HBL–IGBT.



Figure 10. The distribution of the hole concentration during the turn-off process.

The change in the recombination rate with the time variation is shown in Figure 11. The main recombination models are the SRH (Shockley–Read–Hall) recombination model and Auger recombination model, which are described by Equations (5) and (6):

$$R_{SRH} = \frac{np - n_i^2}{\tau_p \left[n + n_i exp\left(\frac{E_{trap}}{kT}\right) \right] + \tau_n \left[p + n_i exp\left(\frac{-E_{trap}}{kT}\right) \right]}$$
(5)

$$R_{Auger} = (C_n n + C_p p) \cdot \left(np - n_i^2\right)$$
(6)

where *n* is the electron concentration, *p* is the hole concentration, and n_i is the intrinsic carrier concentration, which is related to the bandgap and temperature. Additionally, n_i is constant when the bandgap and temperature do not change. It is easy to see that the electrons and holes flood into the heterojunction, which increases the carrier concentration in the polySi region. Therefore, the partial of the equation $np - n_i^2$ increases, resulting in improvements in both SRH recombination and Auger recombination. Moreover, the bandgap of polySi is less than that of SiC, which means $n_i \exp\left(\frac{E_{trap}}{KT}\right)$ decreases. E_{trap} represents the difference between the recombination center and conduction band or valence band. Therefore, the highest recombination rate of the HBL–IGBT was more than 10^{25} cm⁻³·s⁻¹. At the same time, the highest recombination rate of the C–IGBT was about 10^{19} cm⁻³·s⁻¹ at the same position. It can be seen that the recombination was enhanced by the heterojunction structure during the turn–off process.



Figure 11. The distribution of the recombination rate during the turn-off process.

 $V_{\rm F}$ can be reduced and increased by changing the carrier lifetime. A higher carrier lifetime means that more holes can be injected into the N–buffer from the P+ collector, resulting in a better hole injection efficiency and leading to improvements in the conductivity modulation, obtaining a lower $V_{\rm F}$. However, higher amounts of excess carriers require more energy and time to sweep off, resulting in a higher $E_{\rm off}$. The trade–off relationship between the $E_{\rm off}$ and $V_{\rm F}$ is shown in Figure 12. It is shown that the HBL–IGBT presents an improved trade–off between the $E_{\rm off}$ and $V_{\rm F}$ compared with the C–IGBT, indicating a better dynamic performance.



Figure 12. The trade–off relationship between the E_{off} and V_{F} .

4. Conclusions

In this paper, a novel SiC IGBT with a SiC/Si heterojunction in the buffer layer was presented and investigated by using simulation software. A heterojunction transport model was introduced and described in relation to the different bandgaps of SiC and polysilicon.

The simulation results of the new structure showed a better dynamic characteristic with a similar forward voltage ability, which was caused by the carrier storage and enhanced recombination effect in the polySi region. The performance of the proposed structure was influenced by the parameters of polysilicon; therefore, a trade–off curve of the optimization of W_{Si} and T_{Si} between t_{off} and V_F was drawn. The optimization dimensions adopted for W_{Si} and T_{Si} were 0.5 µm and 0.5 µm. For the static characteristics, the V_F of the C–IGBT was 4.81 V, and that of the HBL–IGBT was 5.35 V. However, the breakdown voltage of both structures approached 16 kV. More importantly, the t_{off} reduced from 325 ns to 232 ns, which indicated a 28.6% reduction. Additionally, the E_{off} decreased from 2.619 mJ to 1.375 mJ, which indicated a 47.5% reduction. Moreover, plasma–activated direct bonding technology can be used to form the HBL–IGBT, which is compatible with the conventional process. Therefore, the HBL–IGBT is a desirable structure to optimize the performance of SiC IGBTs.

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