electronics

MDPI

Article

Adaptive Mesh Generation Technique for Efficient Electromagnetic Computation in RFIC Designs

Xianbing Wang, Peng Zhao * and Gaofeng Wang *

MOE Engineering Research Center of Smart Microsensors and Microsystems, College of Electronics and Information, Hangzhou Dianzi University, Hangzhou 310018, China; wxb@hdu.edu.cn
* Correspondence: pengzhao@hdu.edu.cn (P.Z.); gaofeng@hdu.edu.cn (G.W.)

Abstract: A novel adaptive mesh generation technique for efficient electromagnetic simulation of radio-frequency integrated circuits (RFICs) is herein presented. By exploring the geometrical and physical characteristics of RFICs, some adaptive mesh treatments, such as mesh projection, edge refinement, via polymerization, etc., are utilized to improve the accuracy and efficiency of electromagnetic computations. For strong coupling structures, such as two conductors in close proximity for a relatively large area, a projection-based mesh scheme is introduced to improve the accuracy of numerical integration. Moreover, the current most likely concentrates near the edges of conductors due to the edge effect. To better model the edge effect, an edge refinement scheme is applied. For via arrays that appear common in RFICs, an automatic via aggregation approach is adopted to improve computational efficiency yet still keep good computational accuracy. Finally, some numerical examples are given to validate the computational accuracy and efficiency of the novel adaptive mesh generation technique.

Keywords: mesh; projection; edge refinement; electromagnetic computation; RFIC

Citation: Wang, X.; Zhao, P.; Wang, G. Adaptive Mesh Generation Technique for Efficient Electromagnetic Computation in RFIC Designs. *Electronics* **2023**, *12*, 2167. https://doi.org/10.3390/electronics12102167

Academic Editor: Gerardo Di Martino

Received: 30 March 2023
Revised: 20 April 2023
Accepted: 4 May 2023
Published: 10 May 2023

1. Introduction

In radio-frequency (RF) circuits, the RF devices operate under the rule of electromagnetic fields. As a consequence, circuit theory is generally insufficient for analyzing RF devices. Instead, a more rigorous theory, i.e., electromagnetic field theory, must be invoked to study RF devices. Advanced electromagnetic simulation tools help RF engineers to design successful RF chips and accelerate the product design process by evaluating the design performance, reducing trial and error costs, improving design efficiency, optimizing the design configuration, and so on. Efficient electromagnetic computation is an essential engine of all electromagnetic simulation tools.

Due to the diversity and complexity of electromagnetic field problems that need to be solved in practical engineering, a variety of numerical methods have been developed in computational electromagnetics [1–6]. In these algorithms, the numerical solution of Maxwell's equations usually involves meshing or discretization, in which a continuous solution domain is discretized into a finite number of elements and the accuracy of computational results is dependent on the element size. After meshing or discretization, Maxwell's equations are reduced to a linear matrix system. Better accuracy can be obtained by increasing the mesh density. A finer mesh usually leads to higher accuracy but requires longer computational time and larger memory consumption. At the limit, where the mesh becomes infinitely dense, theoretically, the numerical solution should converge to the exact solution of Maxwell's equations [7–9]. In practice, however, computing resources are always limited. Hence, a mesh scheme needs to be developed for attaining a proper mesh on which an accurate solution can be obtained with the minimum consumption of computing resources. In the case of the same computational method, the mesh quality is the most critical factor for determining computational accuracy and efficiency.

There have been many efforts in developing optimal mesh generation schemes for electromagnetic computations. For example, the mesh improvement of the boundary integral method, similar to the traditional finite element method, can have a variety of approaches, such as h-, p-, and r-type schemes. The h-type scheme approximates the exact solution by continuously making the mesh denser while keeping the element order unchanged [10]. The p-type scheme improves the computational results by increasing the lowest order of the elements without changing the meshing of the structure [11]. The r-type scheme reduces the solution errors by rearranging the mesh without changing the number of elements [12].

In addition, there are several forms of hybrid methods. The h-type scheme has good convergence properties for functions with singular points, but the mesh refinement may significantly increase the number of unknowns. Although the p-type scheme does not increase the number of elements, it does increase the order of elements and, thus, the solution complexity. In particular, for the integrated circuits that are usually planar structured, low-order basis functions are more effective. Although the r-type scheme also does not increase the number of elements, rearranging the mesh alone does not guarantee the solution convergence, and, thus, it generally requires mixing the h-type scheme to attain a convergent solution.

The iteration process strongly depends on the efficiency of mesh refinement, in which new grids (elements) are repeatedly added, and the computations are carried out over each refined mesh repeatedly, resulting in a large amount of time consumption. In [13], the hp-type adaptive finite element method was studied in three-dimensional electromagnetic computation. The hp-type adaptive finite element method can effectively improve the solution accuracy. However, the meshes studied in [13] are mainly structured ones, and the adaptive mesh refinement algorithm is aimed at the cuboid meshes only, which is hardly applied to complex and irregular structures. In [14], the dual error estimation weighting method (DEW) was introduced for adaptive mesh refinement control, which can achieve a highly accurate solution. However, the approximate gradient term used in the gradient recovery method must be used in a uniformly conductive region, and otherwise, the error is larger. In addition, the dual residual weighting method (DRW) is much more complex, and thus hardly used in three-dimensional problems. In [15], the unstructured meshing program "Triangle" was reported to create two-dimensional geoelectric models and generate adaptive finite element meshes, to which most studies of adaptive finite element meshing algorithms have been applied. In an analysis of solid and structural mechanics [16], the strain gradient was utilized to analyze local solution characteristics in stress-concentrated and rapidly changing strain regions [12] which can provide a theoretical basis for the mesh refinement but could not guarantee convergence in any form of mesh generation.

In this work, an adaptive mesh generation technique for efficient electromagnetic computation in RFIC designs is developed. According to the characteristics of RFICs, the problems of strong coupling, edge effect, and large-scale via arrays, which plague the efficiency of electromagnetic computation, are paid special attention. In RFICs, some metal structures (e.g., capacitors) are very closely arranged. When the gap between two metals is very small, the mesh size must be generally comparable to the gap for achieving good accuracy which leads to a large number of small elements and, thus, deteriorates the computational efficiency. A projection-based mesh scheme is herein introduced to effectively treat and subdivide very closed-arranged structures which can greatly reduce the number of small elements yet maintain good accuracy. At high frequencies, the current distribution most likely concentrates at the edges of metals. To reflect this edge effect, an adaptive edge mesh scheme is applied to generate finer meshes at metal edges whereas coarser meshes are used in the middle of metals. In addition, via arrays that are commonly present in RFICs. Direct meshing of these tiny metals may lead to a large number of elements or unknowns which could significantly deteriorate the computational efficiency and consume

a great deal of memory resources. A scheme of aggregating these tiny metals is introduced to improve computational efficiency yet keep good computational accuracy.

2. Mesh Schemes

For EM simulation in RFICs, the problem can be formulated in terms of the mixed-potential integral equation (MPIE) [17,18]

$$-\vec{E}^{inc} = \frac{i\omega\mu_0}{4\pi}\int_S dS' \bar{\bar{G}}_A(\vec{r},\vec{r}\,')\cdot\vec{J}(\vec{r}\,') - \frac{1}{4\pi i\omega\varepsilon_0}\nabla\int_S dS' G_\phi(\vec{r},\vec{r}\,')\nabla'\cdot\vec{J}(\vec{r}\,'), \quad (1)$$

where $\vec{J}(\vec{r}\,')$, S, ω, μ_0, ε_0, $\vec{r}$, and $\vec{r}\,'$ are the current density, closed metal surface, angular frequency, permeability in vacuum, permittivity in vacuum, observation point, and source point, respectively. In addition, $\bar{\bar{G}}_A(\vec{r},\vec{r}\,')$ and $G_\phi\left(\vec{r},\vec{r}\,'\right)$ are the dyadic and scalar multilayered dielectric medium Green's functions [19], respectively. Since the effects of multilayered dielectric medium are included in the Green's functions, only the metal structures in RFICs need to be meshed.

The surface current is expanded by virtue of the zero-th divergence conforming basis (DCB) functions (e.g., triangular mesh-based RWG [20] as shown in Figure 1), viz.,

$$\vec{J}(\vec{r}\,') = \sum_{j=1}^{N} x_j \vec{j}_j(\vec{r}\,'), \quad (2)$$

where

$$\vec{j}_j(\vec{r}\,') = \begin{cases} \frac{l_n}{2A_n^+}\vec{\rho}_n^{\,+}, & r \text{ in } T_n^+ \\ \frac{l_n}{2A_n^-}\vec{\rho}_n^{\,-}, & r \text{ in } T_n^- \\ 0, & \text{otherwise} \end{cases}. \quad (3)$$

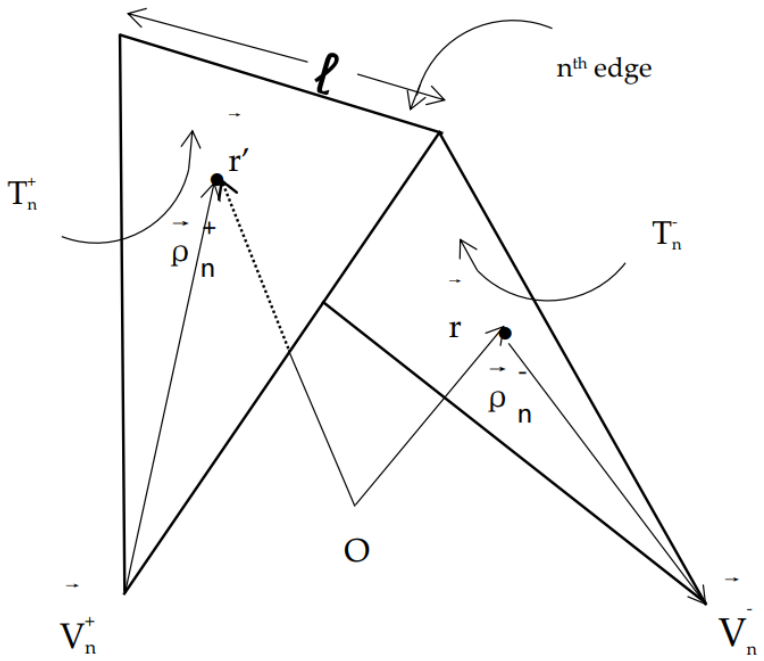


Figure 1. RWG basis.

Then, the Galerkin procedure is applied to (1) to generate a method of moment (MoM) matrix equation, viz.,

$$\bar{\bar{A}}_{N\times N}\cdot\bar{x}_{N\times 1} = \bar{V}_{N\times 1}, \quad (4)$$

where N is the number of basis functions. The entries of the impedance matrix $\overline{\overline{A}}$ and excitation vector $\overline{V}$ are calculated as

$$A_{i,j} = \int_{S_i} dS \int_{S_j} dS' [\vec{j}_i(\vec{r}) \cdot \overline{\overline{G}}_A(\vec{r}, \vec{r}') \cdot \vec{j}_j(\vec{r}') - \frac{1}{\omega^2 \mu_0 \varepsilon_0} \nabla \cdot \vec{j}_i(\vec{r}) G_\Phi(\vec{r}, \vec{r}') \nabla \cdot \vec{j}_j(\vec{r}')], \tag{5}$$

and

$$V_i = \frac{4\pi i}{\omega \mu_0} \int_{S_i} dS \vec{j}_i(\vec{r}) \cdot \vec{E}^{inc}. \tag{6}$$

(a) Projection scheme

In RFICs, metals, such as metal structures in flat plates or finger capacitors that are very closely arranged have strong electromagnetic coupling due to the proximity effect, particularly between two very closely nearby metal surfaces. In order to accurately model such strong electromagnetic coupling, it requires a very high density of meshes in a brute-force approach. Such a brute-force approach could result in too many elements or unknowns which consumes too much memory resource and CPU time and is usually intolerable in many cases.

Consider the numerical evaluations of (5) and (6), in which the Gaussian integration is generally used. By substituting (3) into (5) and using the Gaussian integration, each of the items in the (5) related to $\overline{\overline{G}}_A(\vec{r}, \vec{r}')$ can be expressed as

$$\left(A_{ij}^{\alpha\beta}\right)^{++} = l_i l_j \sum_{m=1}^{N_G} W(m) \sum_{n=1}^{N_G} W(n) \cdot \left[\left(\vec{r}_m - \vec{V}_i\right)^{\alpha} \cdot G_A^{\alpha\beta}(\vec{r}, \vec{r}') \cdot \left(\vec{r}'_n - \vec{V}_j\right)^{\beta} \right], \ \alpha, \beta = x, \ y \text{ or } z, \tag{7}$$

and the component associated with $G_\Phi(\vec{r}, \vec{r}')$ can be expressed as:

$$\left(A_{ij}^{\Phi}\right)^{++} = l_i l_j \sum_{m=1}^{N_G} W(m) \sum_{n=1}^{N_G} W(n) \cdot \frac{4}{\omega^2 \mu_0 \varepsilon_0} \cdot G_\Phi(\vec{r}, \vec{r}'), \tag{8}$$

where $\vec{r}$ and $\vec{r}'$ are in the "+" triangles of RWG i and j, respectively, NG represents the number of Gaussian sampling points, $\vec{r}_m$ and $\vec{r}'_n$ are the sampling points on the field and source triangles, respectively, and $W(m)$ and $W(n)$ denote the corresponding Gaussian integration weights to the sampling points on the field and source triangles, respectively.

Consider the case that two metal surfaces are very closely apart, in which the field and source triangles may still be very close even though they locate in different metal surfaces as shown in Figure 2. In this case, some pseudo-singularity in (7) and (8) needs to be well treated. Without loss of generality, consider the free-space Green's function:

$$G(\vec{r}, \vec{r}') = \frac{e^{ikR}}{R}, \tag{9}$$

where $R = |\vec{r} - \vec{r}'| = |\vec{W} + \vec{h}|$, $\vec{h}$ is the distance vector between two metal surfaces, and $\vec{W}$ is the offset vector between the field and source points.

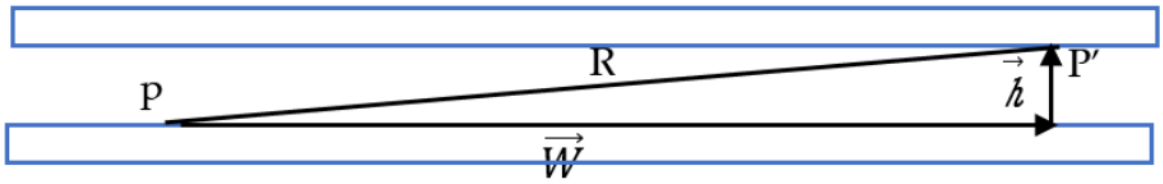


Figure 2. Effect of two metal surfaces that are closely apart.

Since h is very small, there is a pseudo-singularity in (9) which behaves as 1/R or 1/h. When the distance between two metal surfaces is very small, the coupling between them is very strong. In evaluations of (7) and (8), the pseudo-singularity of 1/h plays an important role since 1/h becomes very large as h is very small and may contribute the most to the coupling between the two metal surfaces. However, when the offset W is much greater than the gap h, the value of 1/R becomes much larger than the value of 1/h. As a consequence, the Green's function becomes too small to reflect the strong coupling between the two metal surfaces. In order to accurately capture such a pseudo-singularity behavior in the Gaussian integration, the offset of two nearby sampling field and source points in the Gaussian integration must be smaller than h which may require very fine mesh and, thus, result in too many unknowns in the numerical computation.

Alternatively, a projection-based mesh scheme can be used. Specifically, one can first identify the aligning areas between these two metal surfaces that are closely apart. Then, the two aligned areas are meshed in the same manner through a projection from one metal surface to the other metal surface, so that there is no offset between two meshes along the metal surfaces.

With the projection-based mesh scheme, the triangular elements between the metal surfaces are well aligned, and so do the Gaussian sampling points on these triangular elements. As a consequence, the Green's function computed on the field and source points which locate at the aligned Gaussian sampling points, can take well account of pseudo-singularity 1/h regardless the size of the triangular elements. Therefore, accurate numerical integration in (7) and (8) can be achieved without requiring very fine mesh.

The projection-based mesh scheme can be applied to on-chip parallel-plate capacitors, in which the gap between two metal plates is usually designed to be very small in order to increase the capacitance. For multilayered finger capacitors, the gap between two fingers is also designed to be very small to achieve large capacitance, and, thus, the projection-based mesh scheme is also required to mesh multiple fingers in multiple layers.

The projection algorithm works as follows:

1. Check whether the distance between metal layers satisfies the proximity condition. If so, take the geometries on the metal layers that need to be projected (L1, L2, . . . , Ln) and perform a Boolean AND operation to obtain the common part A.
2. Use "triangle" to generate a triangular mesh for A and record the edge points P.
3. Subtract A from (L1, L2, . . . , Ln) to obtain the shapes (S1, S2, . . . , Sn) and place P on (S1, S2, . . . , Sn).
4. Triangulate (S1, S2, . . . , Sn) with P while enforcing that the edges do not increase the number of points to ensure element alignment.
5. The resulting mesh consists of the elements obtained by triangulating (S1, S2, . . . , Sn) with P and the elements obtained by triangulating A.

(b) Edge refinement

In high-frequency circuits, electrical current changes rapidly and distributes unevenly on cross-sections of metal lines. In general, the current most likely concentrates at the edges whereas is relatively flat in the middle areas of metal lines. To effectively characterize the edge concentration, it is highly desirable to have finer meshes at the edges.

In general, the metal traces in integrated circuits can be refined at the edges proportionally. As shown in Figure 3, for example, the sidewalls of metal traces are subdivided into three segments according to the ratio of 0.2:0.6:0.2, whereas the top and bottom surfaces of metal traces are subdivided into four segments according to the ratio of 0.2:0.3:0.3:0.2.

In general, rectangular meshes are used in the middle areas of metal traces whereas triangular meshes are employed at the corners of metal traces. With mesh edge refinement, the current can be better characterized, and, thus, more accurate numerical results can be obtained with fewer unknowns.

(c) Via aggregation

There are sometimes many small metal objects (such as via arrays) in integrated circuits. These metal objects are huge in number, but their structures are very simple, mainly playing the role of connecting upper and lower metal layers. If they are processed one by one, they could consume a great deal of computer resources in both CPU time and memory storage. Nevertheless, the small elements from these small metal objects and the large elements from RF devices can also cause a wide disparity of geometrical scales which may cause numerical instability.

During the mesh generation, it is, thus, necessary to identify the groups of vias and aggregate each of them into a large via, in which the large aggregated vias should keep the same electrical connections as the original vias do. Fortunately, these small via arrays are regularly arranged in integrated circuits. In many cases, their size, shape, and spacing are exactly the same, and, thus, it can be readily identified whether they belong to the same group of via arrays (as shown in Figure 4).

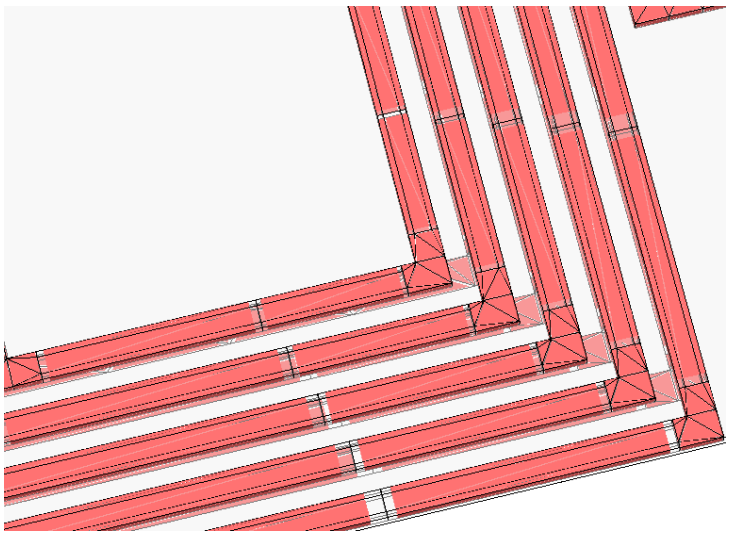


Figure 3. Edge refinement.

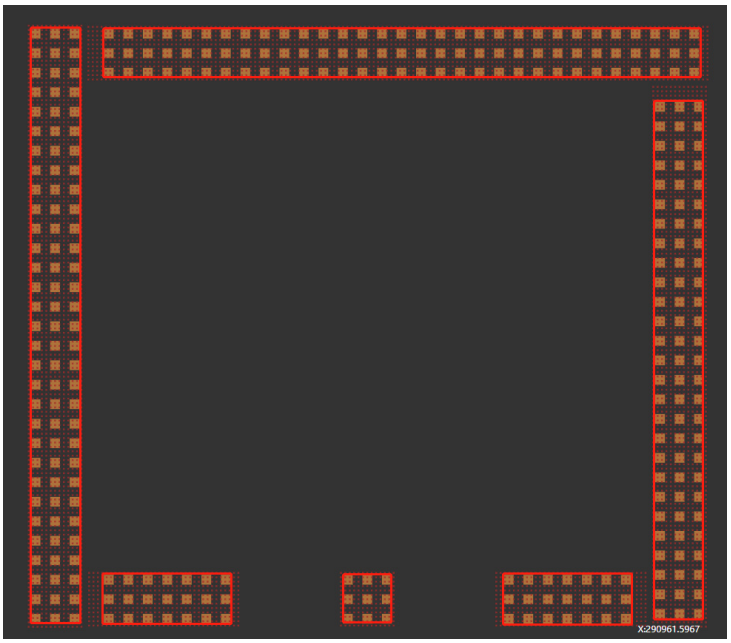


Figure 4. Via aggregation.

The equivalent conductivity of a large aggregated via can be simply modeled as the mean of the conductivities across the entire cross-section that contains the original via array. The large aggregated vias are then meshed, by which the number of unknowns can be greatly reduced, and the wide disparity of geometrical scales can be well resolved. The via aggregation can greatly speed up the electromagnetic computation yet virtually without compromising the result accuracy.

3. Examples and Validation

In this section, some examples are included to validate the mesh schemes proposed in the preceding section. The standard mesh algorithm is a force-brute approach, in which the mesh is most likely to be uniformly distributed without any optimization to on-chip structures. Moreover, in general, the rectangular mesh is used for metal paths and metal sidewalls, while the triangular mesh is employed for all other metal parts. The reference solution is obtained by iteratively refining the mesh until the result is completely converged, in which this final converged result is used as a reference for comparison. Herein, the space in which no dielectric medium is specified is assumed to be air for computations of the multilayered dielectric Green's functions. The hardware configuration of the server used in all the following simulations is as follows: Intel(R) Xeon(R) CPU E7-4830 v4 @ 2.00 GHz 14 Core × 4 400 G RAM Threads 4.

(d) Projection scheme

The first example is a flat plate capacitor as shown in Figure 5. In Figure 5, MET1 and MET2 are two metal layers. Virtual_VIA1 is a via layer that connects to MET2 upwards and is apart with a small gap (i.e., 150 nm) from MET1 below. The small gap between Virtual_VIA1 and MET1 forms the main part of the on-chip flat plate capacitor. VIA2 is another via layer that connects MET1 and MET2. The settings and diagram of layers MET1, MET2, Virtual_VIA1 and VIA2 are illustrated in Figures 6 and 7, respectively. Figure 5 is a 3D view of the device under design which needs to be meshed. Figure 6 defines the RFIC process data with geometrical and physical properties for all the stack layers, such as the substrate, dielectric stack layers, and metal layers. This figure includes names, thicknesses, and material properties of all the layers. From this figure, it can be seen that there is a 150 nm gap between the VIA2 layer and the Virtual_VIA1 layer. Figure 7 is a visual representation of the table in Figure 6.

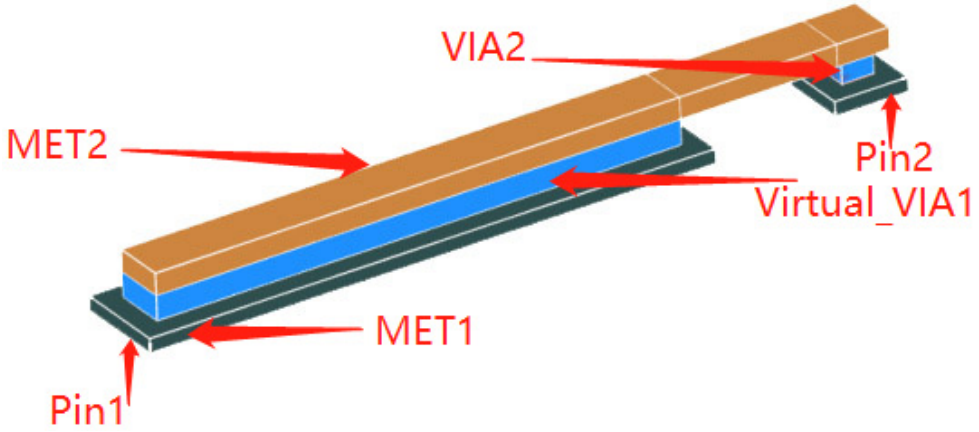
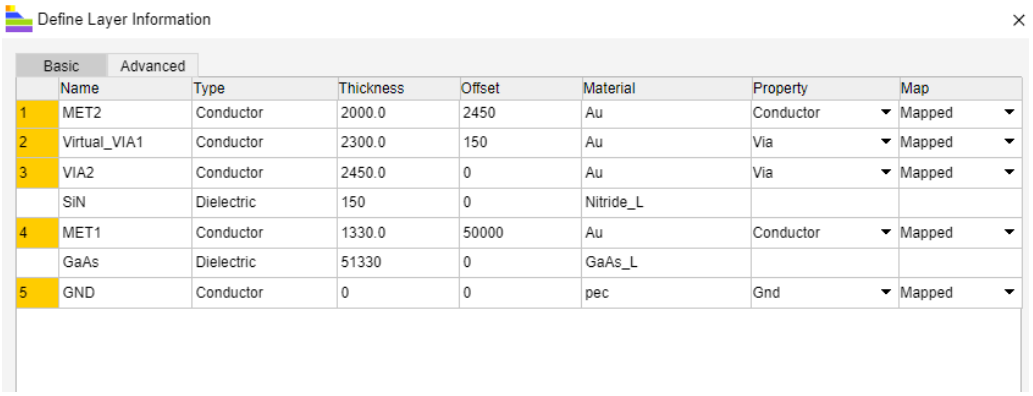


Figure 5. On-chip flat plate capacitor.

The longest dimension of the entire design is 70 microns, whereas the widest dimension is nine microns. The highest frequency under consideration is 40 GHz. Hence, the device size is very small in comparison with the wavelength of electromagnetic waves under consideration. In general, the mesh size must be smaller than one tenth of the wavelength which is readily met by a standard mesh scheme. The upper and lower surfaces are meshed in terms of triangular grids by the standard mesh scheme which results in

79 elements as shown in Figure 8. The left panel of Figure 8 illustrates the meshes on the bottom surface of Virtual_VIA1, whereas the right panel of Figure 8 shows the meshes on the upper surface of MET1. It can be seen that these two meshes on the bottom surface of Virtual_VIA1 and the upper surface of MET1 are quite different and do not coincide with each other.



	Name	Type	Thickness	Offset	Material	Property	Map
1	MET2	Conductor	2000.0	2450	Au	Conductor	Mapped
2	Virtual_VIA1	Conductor	2300.0	150	Au	Via	Mapped
3	VIA2	Conductor	2450.0	0	Au	Via	Mapped
	SiN	Dielectric	150	0	Nitride_L		
4	MET1	Conductor	1330.0	50000	Au	Conductor	Mapped
	GaAs	Dielectric	51330	0	GaAs_L		
5	GND	Conductor	0	0	pec	Gnd	Mapped

Figure 6. Layer settings.

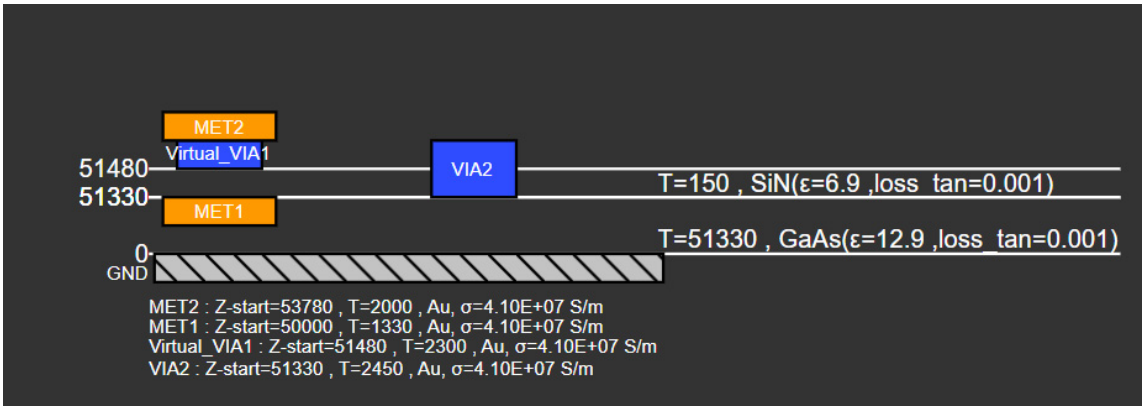


Figure 7. Layer diagram.

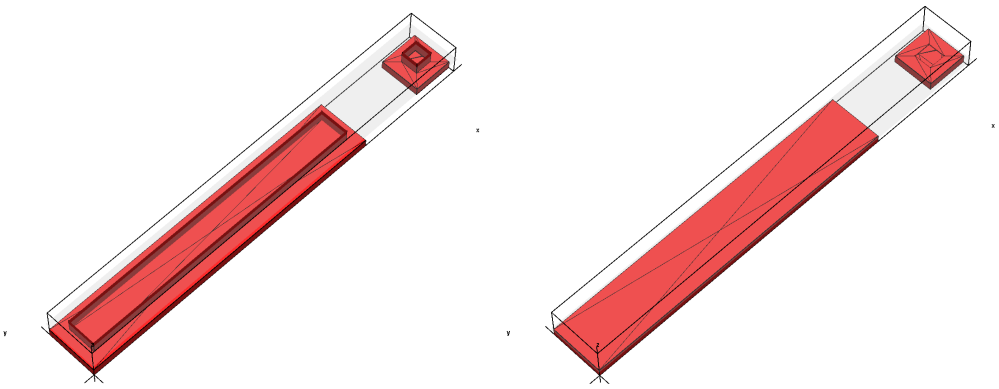


Figure 8. Meshes on two-plate surfaces of a capacitor using standard mesh scheme.

It takes 30 s to complete the computation with a memory requirement of 831.18 MB. Figure 9 shows the simulation results of the S-parameter (S11) and capacitance using the meshes from Figure 8 in comparison with the accurate reference results. One can observe that both the S-parameter and capacitance exhibit large errors by comparison with the accurate reference results. Moreover, as the frequency increases, the errors tend to become bigger.

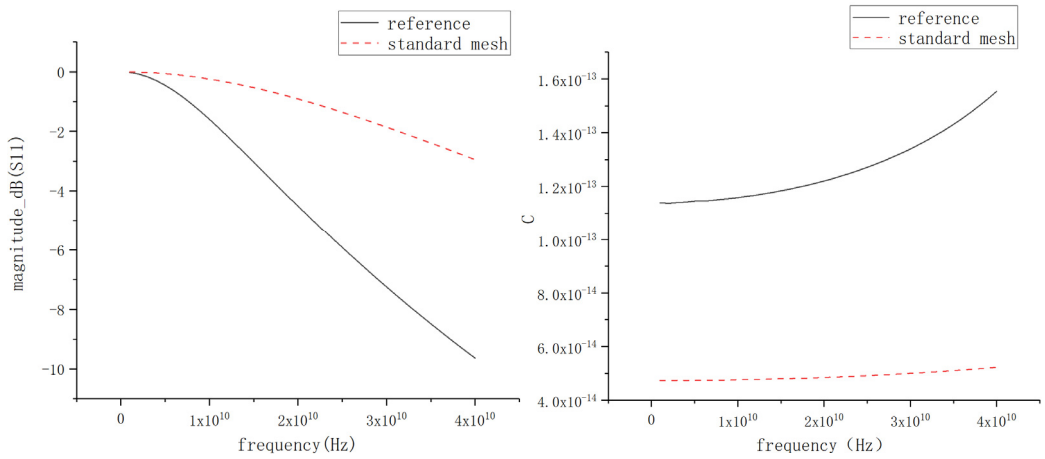


Figure 9. Simulation results of S11 and capacitance using standard mesh scheme.

Now, the meshes are refined to be 10 times denser as shown in Figure 10. The number of elements reaches 1633 at this time. It takes 5.95 min to complete the computation with a memory requirement of 1208.04 MB. The simulation results of the S-parameter (S11) and capacitance using the 10 times refined meshes from Figure 10 are added as shown in Figure 11. One can observe that the simulation results with 10 times refined meshes are much closer to the accurate reference results. However, the errors are still quite significant.

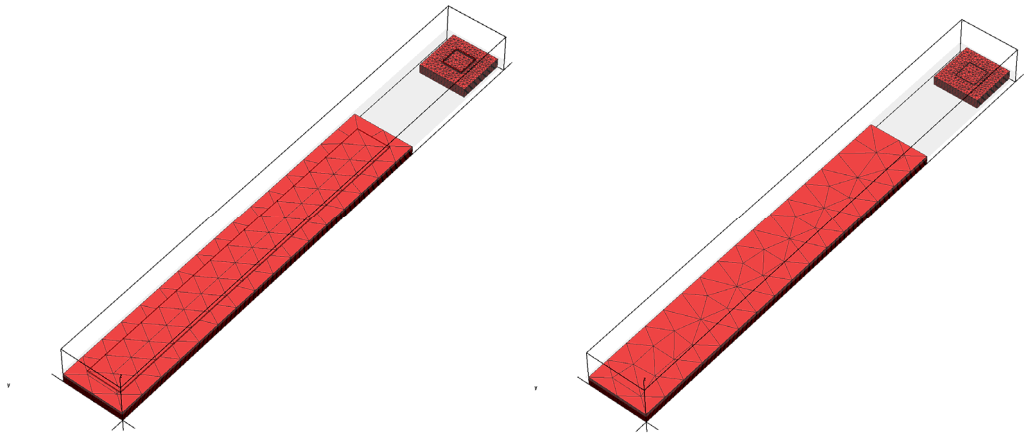


Figure 10. Meshes on two-plate surfaces of a capacitor with 10 times refinement.

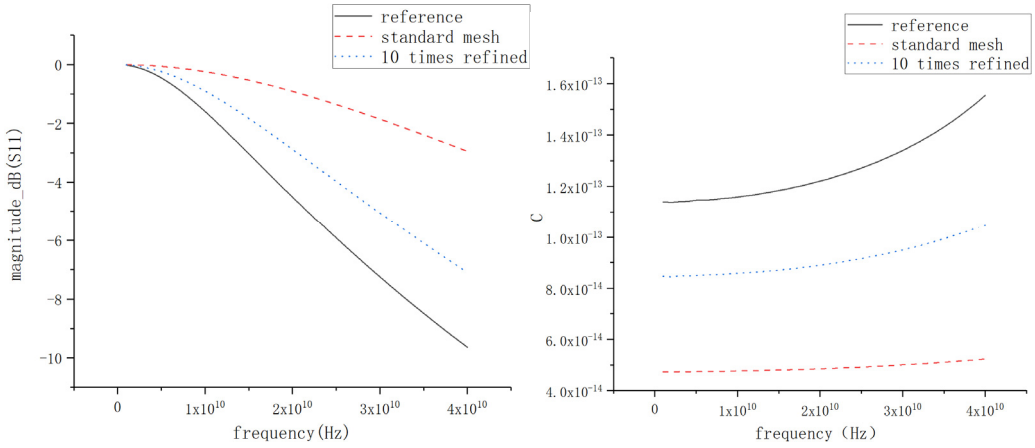


Figure 11. Simulation results of S11 and capacitance using 10 times refined meshes.

By using the proposed projection mesh scheme, the meshes on the bottom surface of Virtual_VIA1 are directly mapped on the upper surface of MET1 as shown in Figure 12. The number of elements is only 85. It takes 27.6 s to complete the computation with a memory requirement of 834.29 MB. The simulation results of the S-parameter (S11) and capacitance using the projection mesh scheme are added as shown in Figure 13. It can be seen that the simulation results from the projection mesh scheme give the closest results to the accurate reference ones. The simulation results, CPU times, and memory consumptions of the above three different mesh schemes are summarized in Table 1.

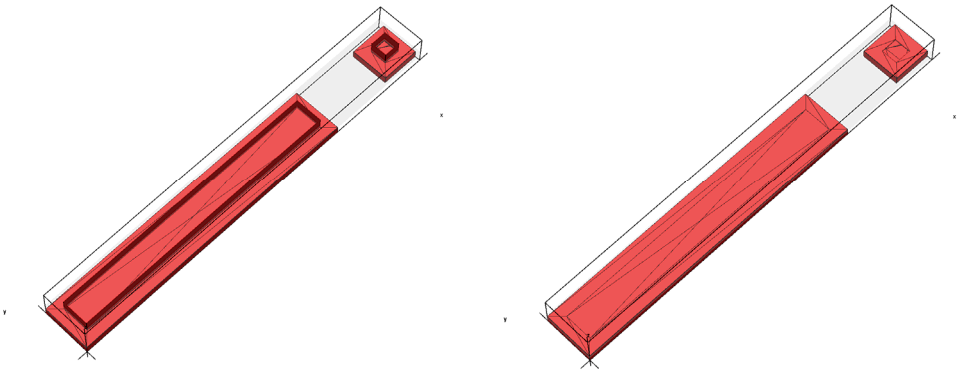


Figure 12. Meshes on two-plate surfaces of a capacitor using the projection scheme.

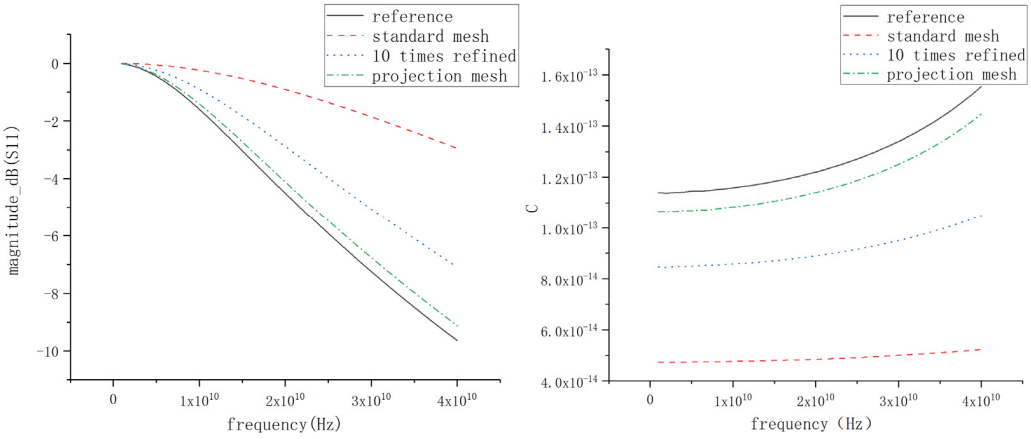


Figure 13. Simulation results of S11 and capacitance using the projection scheme.

Table 1. Accuracy, CPU times, and memory consumptions of different schemes.

Mesh Scheme	# of Elements	CPU Time (Minutes)	Memory (MB)	Capacitance Deviation at 40 GHz
Standard	79	0.5	831.18	59.4%
10 Times Refined	1633	5.95	1208.04	33.4%
Projection	85	0.46	834.29	9.2%

The second example is an on-chip finger capacitor as shown in Figure 14 which consists of five single-layer finger capacitors on metal layers metal2, metal3, metal4, metal5, and metal6. All the single-layer finger capacitors are combined together to form the on-chip finger capacitor through metal vias on via layers V1, V2, V3, and V4. Figures 15 and 16 illustrate the layer settings and diagram, respectively.

Two types of meshes, which are generated by the standard mesh method and the projection scheme, respectively, are examined. Figure 17 shows the detailed mesh elements generated by the standard mesh method, in which the mesh elements are not well aligned. Figure 18 shows the simulation results of the S-parameter (S11) and capacitance using the

meshes from Figure 17 in comparison with the accurate reference results. One can observe that both the S-parameter and capacitance exhibit large errors by comparison with the accurate reference results.

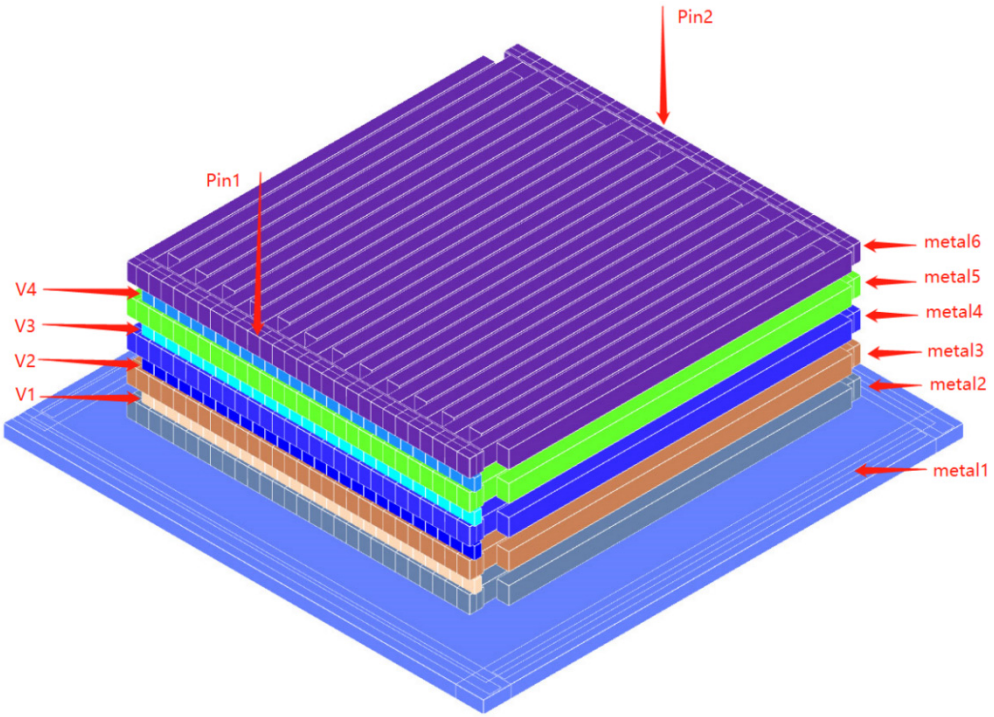


Figure 14. On-chip five-layer finger capacitor.

Figure 19 shows the detailed mesh elements generated by the projection scheme, in which the mesh elements on different layers are well aligned. The simulation results of the S-parameter (S11) and capacitance using the projection mesh scheme are added as shown in Figure 20. It can be seen that the simulation results from the projection mesh scheme give the closest results to the accurate reference ones.

(e) Edge refinement

The third example is an on-chip two-layer quadrilateral spiral inductor as shown in Figure 21. This quadrilateral spiral inductor comprises the rectangular metal structures on layers metal1 and metal2 which are vertically connected by vias on via layers V1 and V2. Two pins are defined on metals (i.e., Pin1) and metal2 (i.e., Pin2). Figures 22 and 23 illustrate the layer settings and diagram, respectively.

Two types of meshes, which are generated by the standard mesh method and the edge refinement scheme, respectively, are examined. Figure 24 compares the meshes generated by the standard mesh method (i.e., the left panel) and the edge refinement scheme (i.e., the right panel). The mesh elements from the edge refinement scheme are finer at the edges than those in the middle of metal traces. Figure 25 shows the simulation results of the S-parameter (S11) for both the meshes from Figure 24 in comparison with the accurate reference results. It can be observed that the S-parameter result with edge refinement is more accurate than that without edge refinement.

(f) Via aggregation

The final example is an on-chip multi-layer octagonal spiral inductor as shown in Figure 26. The on-chip spiral inductor mainly consists of metal structures on two metal layers M8 and M9 which are vertically connected through a via array on via layer V8. Layers M7 and V7 are used to form the bridge at the two ends of the crossover winding on M8. From the perspective view on the right panel of Figure 26, it can be seen that V7 and V8 are the via layers used for vertical connections of the metal layers and the metal

structures on these layers are all via arrays. Figures 27 and 28 illustrate the layer settings and diagram, respectively.

Define Layer Information

Basic Advanced

	Name	Type	Thickness	Offset	Material	Property	Map
1	metal6	Conductor	0.25	0	Copper	Volume	Mapped
	Dielectric25	Dielectric	0.25	0	g65c3	Substrate	
	Dielectric24	Dielectric	0.1	0	g65c3	Substrate	
	Dielectric23	Dielectric	0.03	0	g65c4	Substrate	
2	V4	Conductor	0.18	0	Copper	Via	Mapped
	Dielectric22	Dielectric	0.05	0	g65c5	Substrate	
3	metal5	Conductor	0.25	0	Copper	Volume	Mapped
	Dielectric21	Dielectric	0.25	0	g65c3	Substrate	
	Dielectric20	Dielectric	0.1	0	g65c3	Substrate	
	Dielectric19	Dielectric	0.03	0	g65c4	Substrate	
4	V3	Conductor	0.18	0	Copper	Via	Mapped
	Dielectric18	Dielectric	0.05	0	g65c5	Substrate	
5	metal4	Conductor	0.25	0	Au	Volume	Mapped
	Dielectric17	Dielectric	0.25	0	g65c3	Substrate	
	Dielectric16	Dielectric	0.1	0	g65c3	Substrate	
	Dielectric15	Dielectric	0.03	0	ABS	Substrate	
6	V2	Conductor	0.18	0	Copper	Via	Mapped
	Dielectric14	Dielectric	0.05	0	Alumina	Substrate	
7	metal3	Conductor	0.25	0	Au	Volume	Mapped
	Dielectric13	Dielectric	0.25	0	g65c3	Substrate	
	Dielectric12	Dielectric	0.1	0	g65c3	Substrate	
	Dielectric11	Dielectric	0.03	0	g65c4	Substrate	
8	V1	Conductor	0.18	0	Copper	Via	Mapped
	Dielectric10	Dielectric	0.05	0	g65c5	Substrate	
9	metal2	Conductor	0.25	0	Copper	Volume	Mapped
	Dielectric9	Dielectric	0.25	0	g65c3	Substrate	
	Dielectric8	Dielectric	0.1	0	g65c3	Substrate	
	Dielectric7	Dielectric	0.03	0	g65c4	Substrate	
	Dielectric6	Dielectric	0.05	0	g65c5	Substrate	
	Dielectric5	Dielectric	0.13	0	Air	Substrate	
	Dielectric4	Dielectric	0.03	0	g65c4.5	Substrate	
10	metal1	Conductor	0.18	0.29	Copper	Volume	Mapped
	Dielectric3	Dielectric	0.31	0	g65c4	Substrate	
	Dielectric2	Dielectric	0.257	0	g65c39	Substrate	
	Dielectric1	Dielectric	0.257	0	g65d1	Substrate	
11	Gnd	Conductor	0	0	pec	Gnd	Mapped

Figure 15. Layer settings.

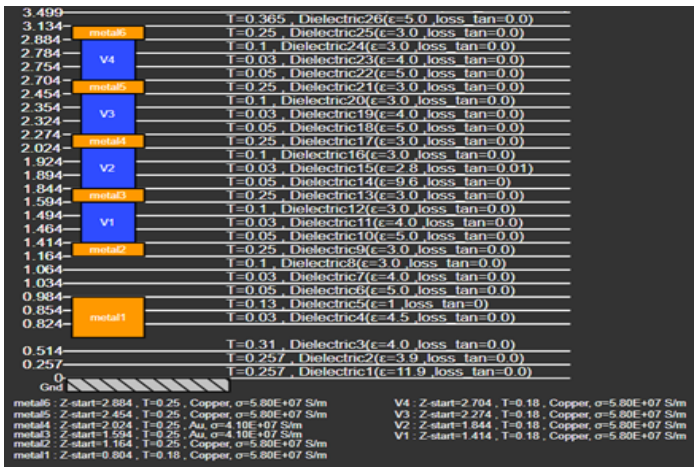


Figure 16. Layer diagram.

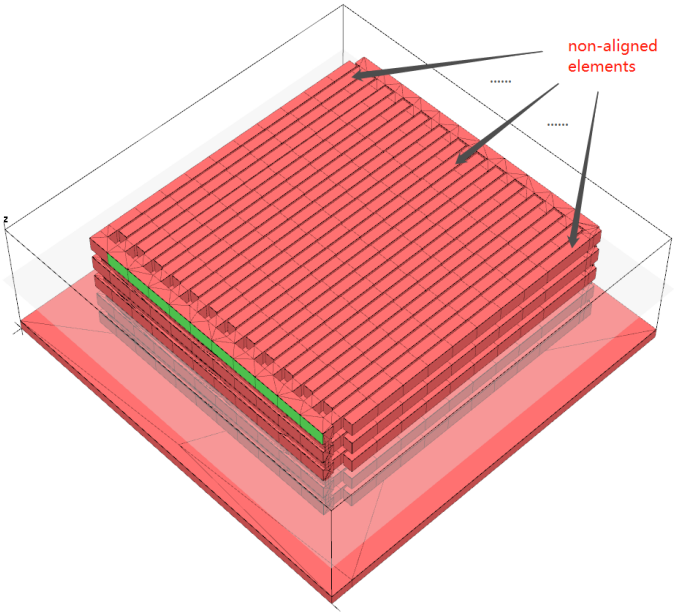


Figure 17. Mesh elements generated by the standard mesh method.

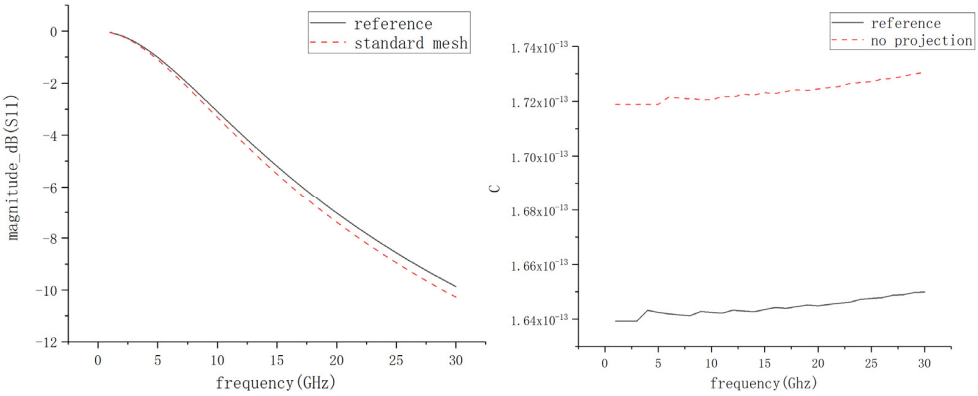


Figure 18. Simulation results of S11 and capacitance using standard mesh scheme.

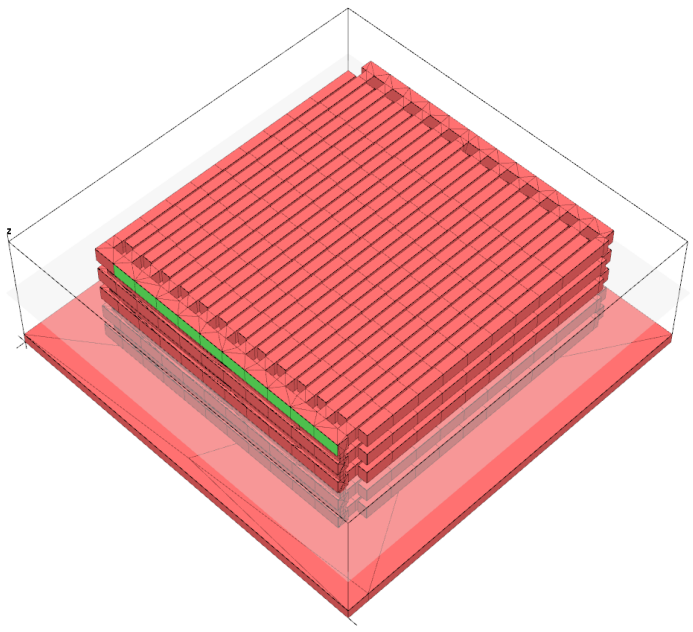


Figure 19. Mesh elements generated by the projection scheme.

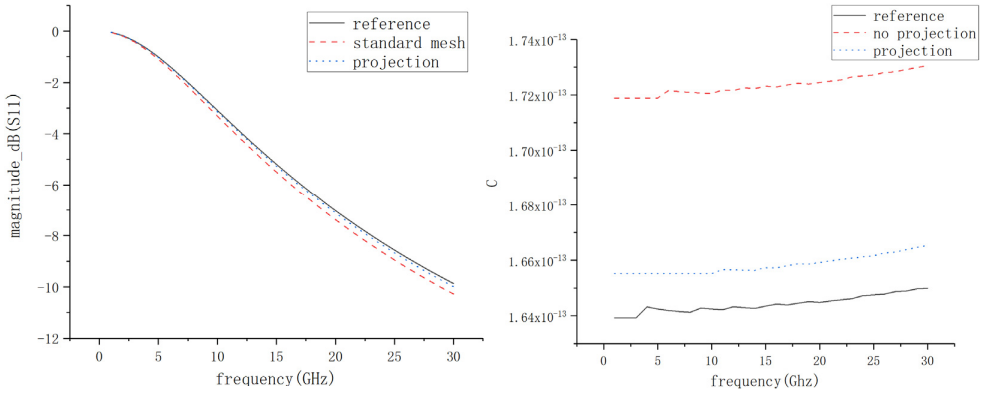


Figure 20. Simulation results of S11 and capacitance using the projection scheme.

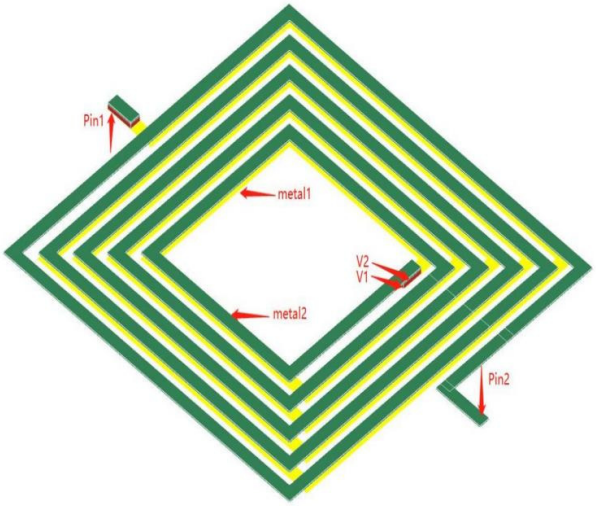


Figure 21. Quadrilateral spiral inductor.

Define Layer Information

Basic | Advanced

	Name	Type	Thickness	Offset	Material	Property	Map
1	metal2	Conductor	0.5	1.6	Ag	Volume	Mapped
2	V2	Conductor	1.6	0	Al	Via	Mapped
	Dielectric3	Dielectric	1.6	0	polyimide	Substrate	
3	V1	Conductor	0.1	0.1	Al	Via	Mapped
4	metal1	Conductor	0	0.1	Copper	Volume	Mapped
	Dielectric2	Dielectric	0.2	0	Alumina	Substrate	
	Dielectric1	Dielectric	545.452	0	Arlon_AD300N	Substrate	
5	Gnd	Conductor	0	0	pec	Gnd	Mapped

Figure 22. Layer settings.

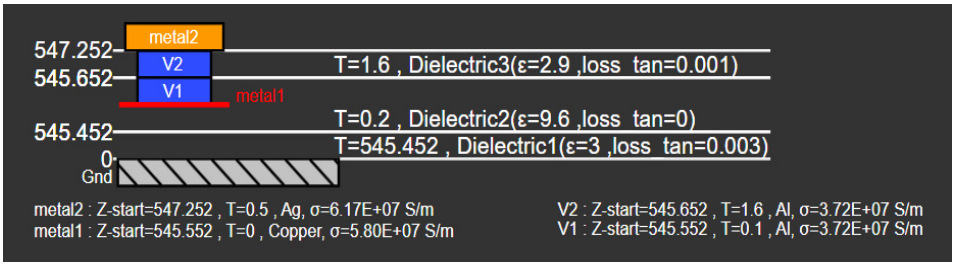


Figure 23. Layer diagram.

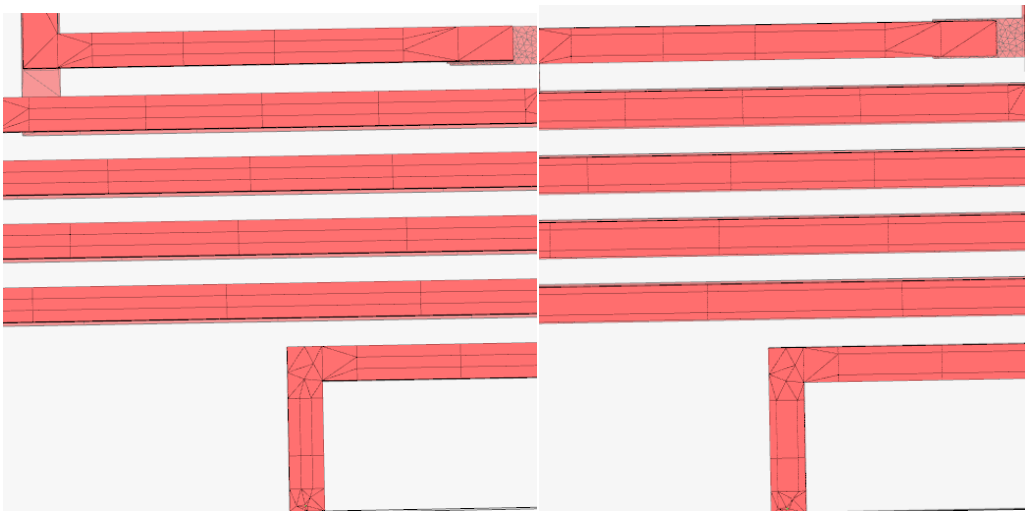


Figure 24. Meshes without and with edge refinement.

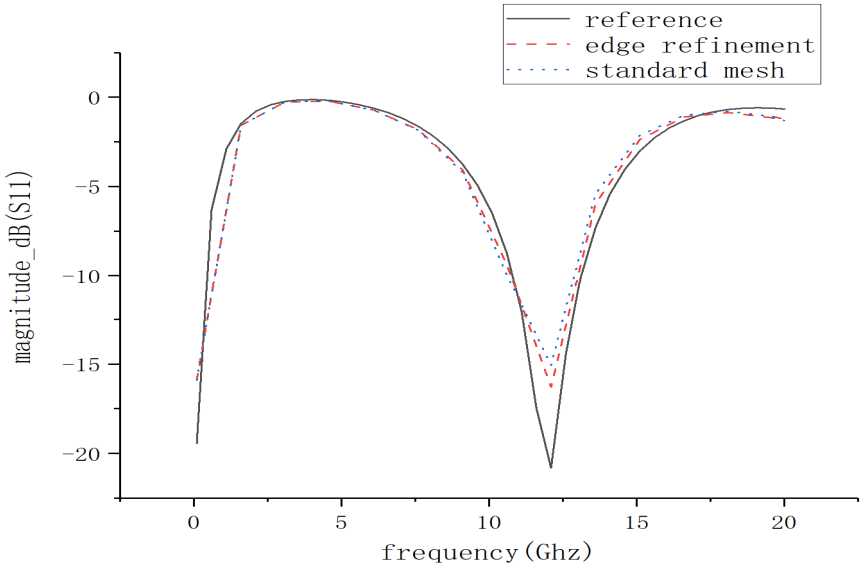


Figure 25. Simulation results of S11 without and with edge refinement.

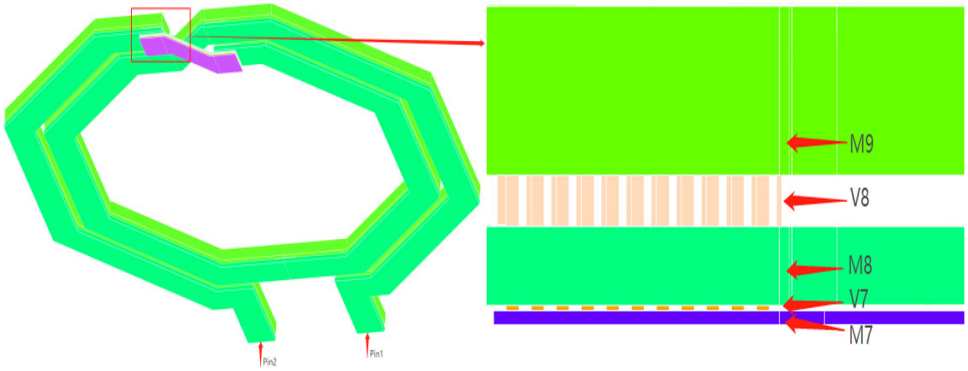


Figure 26. Octagonal multi-layer spiral inductor.

Due to the large number of vias in the via array, the electromagnetic computation consumes a significant amount of CPU time and memory resource. For example, by using the brute-force standard mesh method, the entire electromagnetic computation could consume 23,311 min of CPU time, and 117,908 MB of memory resource.

Define Layer Information

Basic Advanced

	Name	Type	Thickness	Offset	Material	Property	Map
1	M9	Conductor	3000	0	g65m9	Volume	Mapped
	d37	Dielectric	3000	0	g65c4	Substrate	
	d36	Dielectric	110	0	g65c7.8	Substrate	
	d35	Dielectric	725	0	g65c4	Substrate	
2	V8	Conductor	910	0	g65v8	Volume	Mapped
	d34	Dielectric	75	0	g65c7.8	Substrate	
	d33	Dielectric	775	0	g65c4	Substrate	
	d32	Dielectric	50	0	g65c7.8	Substrate	
3	M8	Conductor	1400	45	g65m8	Volume	Mapped
	d31	Dielectric	620	0	g65c4	Substrate	
4	V7	Conductor	95	0	g65v7	Volume	Mapped
	d30	Dielectric	50	0	g65c5	Substrate	
5	M7	Conductor	250	0	g65m567	Volume	Mapped
6	gnd	Conductor	0	0	pec	Gnd	Mapped

Figure 27. Layer settings.

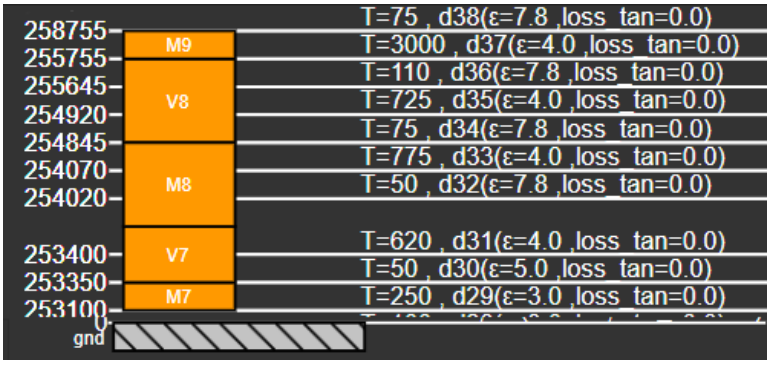


Figure 28. Layer diagram.

To circumvent this difficulty, the proposed via aggregation method can be employed to improve computational efficiency without compromising computational accuracy. Figure 29 shows the original meshes (i.e., the left panel) from the brute-force standard mesh method and the enhanced meshes (i.e., the right panel) from the via aggregation method on layer V8. The numerical results from both meshes are almost identical as shown in Figures 30 and 31. However, the entire electromagnetic computation now only consumes 56 min of CPU time and 3661 MB of memory resources as summarized in Table 2. As the frequency increases, the deviation of the via aggregation results enlarges. In the frequency range under consideration, the deviation is acceptable. However, for much higher frequencies, the deviation may become unacceptable, in which the original massive vias without aggregation need to be used and force-brutely treated.

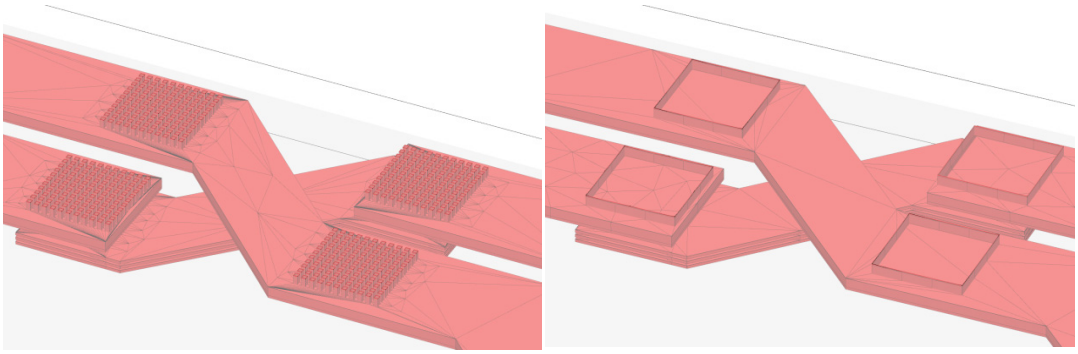


Figure 29. Meshes from the standard mesh method and the via aggregation scheme.

The results obtained by reducing the number of elements on vias are presented in Figures 32 and 33. Although the results are closer to the original results, the computational cost is still in the same order of magnitude as that of the original standard mesh method.

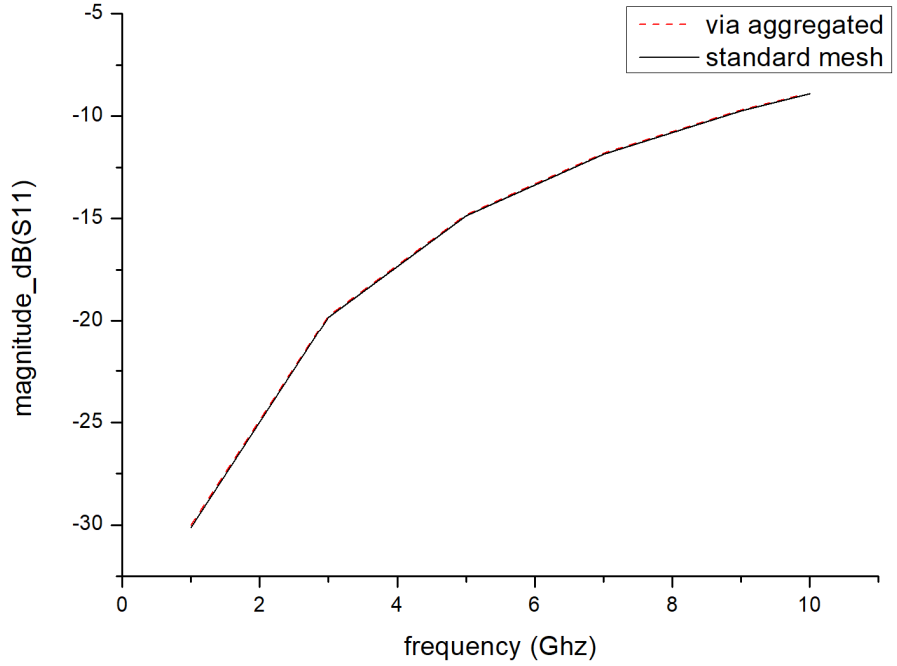


Figure 30. Simulation results of S11 without and with via aggregation.

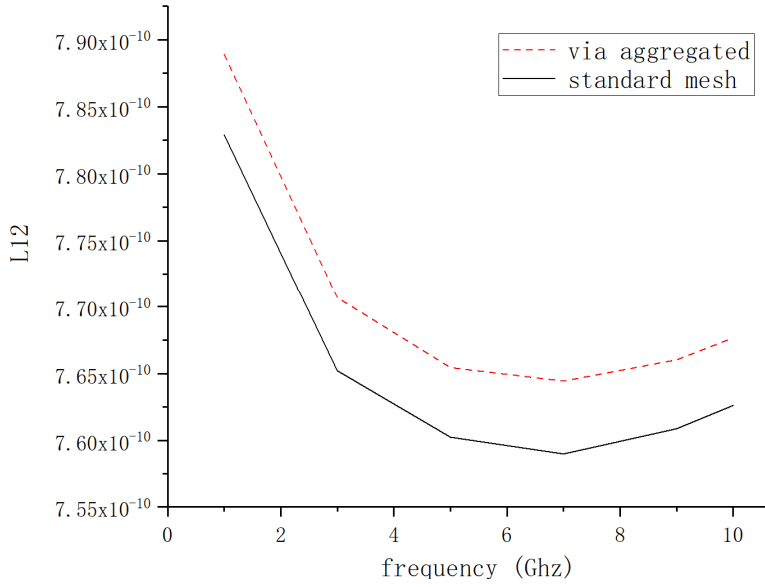


Figure 31. Simulation results of L12 without and with via aggregation.

Table 2. Comparison between the standard, reduced elements and via aggregation methods.

Mesh Scheme	# of Elements	CPU Time (Minutes)	Memory (MB)	Magnitude in dB (S11) at 10 GHz	Inductance at 10 GHz
Standard	31,078	827.9	14,468.27	−8.90463	7.62607×10^{10}
Reduced elements	27,342	563.74	11,665.84	−8.90817	7.622156×10^{10}
Via aggregation	757	25.89	2271.05	−8.86211	7.67668×10^{10}

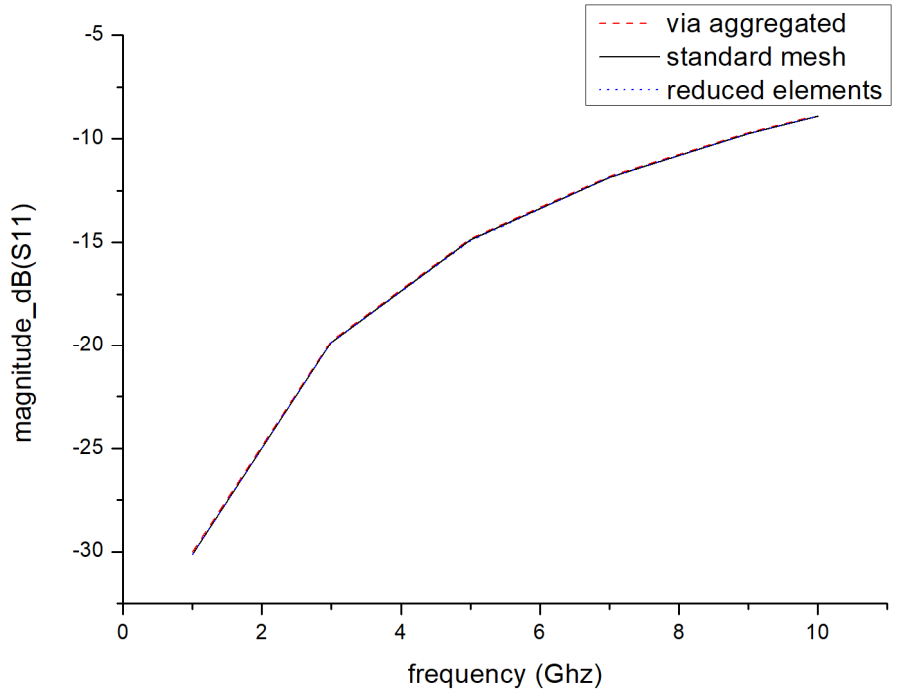


Figure 32. Simulation results of S11 in three cases: original, via aggregation, and reduced number of elements.

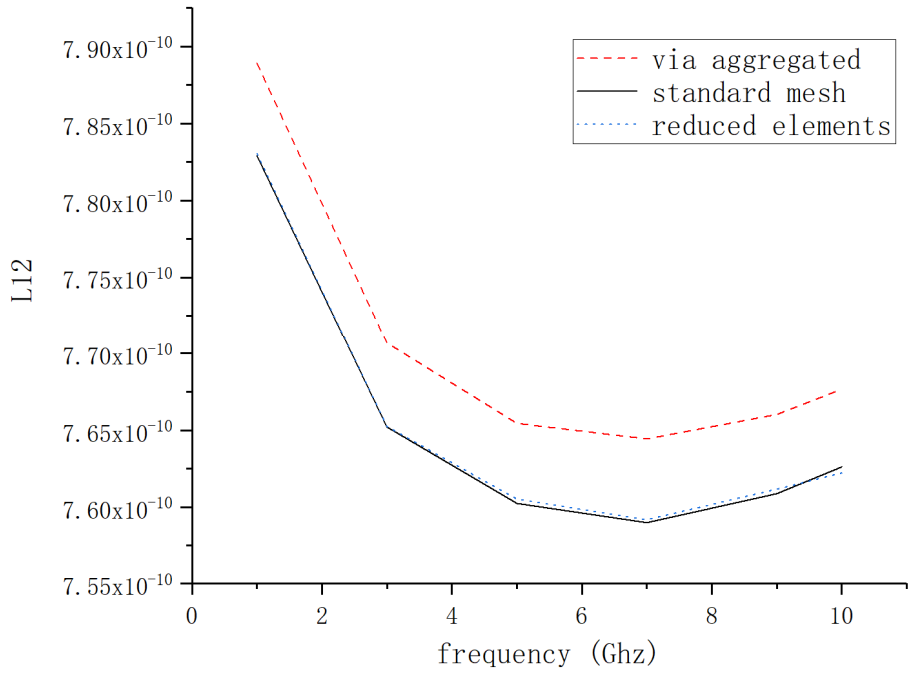


Figure 33. Simulation results of L12 in three cases: original, via aggregation, and reduced number of elements.

4. Conclusions

Adaptive mesh generation technique has been reported for efficient electromagnetic computation in RFIC designs. The electromagnetic coupling between two metal surfaces is very strong when the gap between them is small. If the mesh size is smaller than the gap, the pseudo-singularity of the integral can be well treated, but a very large number of elements may be generated. This is especially true for on-chip capacitors. The projection-based mesh scheme has been introduced to effectively treat and subdivide very closed-arranged

metal structures which can greatly reduce the number of small elements yet maintain good accuracy. At high frequencies, the current distribution most likely concentrates at the edges of metals. To reflect this edge effect, the edge refinement scheme has been proposed to generate finer meshes at metal edges whereas coarser meshes are in the middle of metals. Direct meshing of via arrays may lead to a large number of elements or unknowns which could significantly deteriorate the computational efficiency and consume a great deal of memory space. The scheme of aggregating these small vias has been introduced to improve computational efficiency yet keep good computational accuracy. Several typical devices in RFICs have been used in numerical examples to illustrate and validate the proposed technique.

Author Contributions: Methodology, P.Z.; Writing—original draft, X.W.; Writing—review and editing, G.W. All authors have read and agreed to the published version of the manuscript.

Funding: This research was supported in part by National Nature Science Foundation of China under grant 62141409, in part by Zhejiang Provincial Key Research Development Fund under grant 2021C01041, in part by the Fundamental Research Funds for Provincial Universities of Zhejiang under grant GK239909299001-005 and in part by National Nature Science Foundation of China under grant 62271185.

Data Availability Statement: No new data were created or analyzed in this study. Data sharing is not applicable to this article.

Conflicts of Interest: The authors declare no conflict of interest.

References

1. Harrington, R.F. *Field Computation by Moment Methods*; Wiley-IEEE Press: Hoboken, NY, USA, 1993.
2. Rokhlin, V. Rapid solution of integral equations of classic potential theory. *J. Comput. Phys.* **1985**, *60*, 187–207. [CrossRef]
3. Jin, J. *The Finite Element Method in Electromagnetics*, 2nd ed.; Wiley-IEEE Press: Hoboken, NY, USA, 2002.
4. Wang, G. A hybrid wavelet expansion and boundary element analysis of electro-magnetic scattering from conducting objects. *IEEE Trans. Antennas Propag.* **1995**, *43*, 170–178. [CrossRef]
5. Wang, G.; Pan, G.-W. Full wave analysis of microstrip floating line structures by wavelet expansion method. *IEEE Trans. Microw. Theory Technol.* **1995**, *43*, 131–142. [CrossRef]
6. Wang, G.; Hou, J.; Feng, D. The interaction of EM wave and dielectric bodies—Hybrid equation finite element method. *Sci. China Ser. A—Math. Phys. Astron. Technol. Sci.* **1992**, *35*, 110–121.
7. Maxwell, J.C. A dynamical theory of the electromagnetic field. *Philos. Trans. R. Soc. Lond.* **1865**, *155*, 459–512. [CrossRef]
8. Wang, G. Application of wavelets on the interval to numerical analysis of integral equations in electromagnetic scattering problems. *Int. J. Numer. Methods Eng.* **1997**, *40*, 1–13. [CrossRef]
9. Wang, G. Analysis of electromagnetic scattering from conducting bodies of revolution using orthogonal wavelet expansions. *IEEE Trans. Electromagn. Compat.* **1998**, *40*, 1–11. [CrossRef]
10. Guiggiani, M.; Lombardi, F. Self-adaptive boundary elements with h-hierarchical shape functions. *Adv. Eng. Softw.* **1992**, *15*, 269–277. [CrossRef]
11. Cerrolaza, M.; Alarcon, E. p-adaptive boundary elements for three-dimensional potential problems. *Commun. Numer. Methods Eng.* **2010**, *3*, 335–344. [CrossRef]
12. Ingber, M.S.; Mitra, A.K. Grid redistribution based on measurable error indicators for the direct boundary element method. *Eng. Anal. Bound. Elem.* **1992**, *9*, 13–19. [CrossRef]
13. Demkowicz, L. *Computing with Hp-Adaptive Finite Elements, Vol. 1: One and Two Dimensional Elliptic and Maxwell Problems*; Chapman and Hall/CRC: Boca Raton, FL, USA, 2006.
14. Key, K.; Ovall, J. A parallel goal-oriented adaptive finite element method for 2.5-D electromagnetic modelling. *Geophys. J. Int.* **2011**, *186*, 137–154. [CrossRef]
15. Shewchuk, J.R. Triangle: Engineering a 2D quality mesh generator and Delaunay triangulator. In *Applied Computational Geometry: Towards Geometric Engineering*; Springer: Berlin/Heidelberg, Germany, 1996; pp. 203–222.
16. Zienkiewicz, O.C.; Taylor, R.L. *The Finite Element Method for Solid and Structural Mechanics*; Elsevier: Amsterdam, The Netherlands, 2005.
17. Zhao, P.; Liu, D.Q.; Chan, C.H. A hybrid 2D/3D multilevel Green's function interpolation method for electrically large multilayered problems. *IEEE Trans. Antennas Propag.* **2016**, *64*, 3931–3942. [CrossRef]
18. Zhao, P.; Liu, L.; Xu, K.; Ye, X.; Chen, S.; Wang, G.; Chan, C.H. An improved subspace-regularized DBIM-MLGFIM method for three-dimensional inverse scattering problems. *IEEE Trans. Antennas Propag.* **2021**, *69*, 2798–2809. [CrossRef]

19. Michalski, K.A.; Zheng, D. Electromagnetic scattering and radiation by surfaces of arbitrary shape in layered media, part I: Theory. *IEEE Trans. Antennas Propag.* **1990**, *38*, 335–344. [CrossRef]
20. Rao, S.; Wilton, D. Electromagnetic scattering by surfaces of arbitrary shape. *IEEE Trans. Antennas Propag.* **1982**, *30*, 409–418. [CrossRef]