

Article

Adaptive Dead-Time Control Design with Low Dead-Time Error in 20 MHz 90 V GaN Gate Driver

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Abstract: This paper presents an adaptive dead-time control circuit for a maximum work frequency 20 MHz, maximum voltage level 90 V GaN gate driver. The dead-time is set to prevent straight-through of the upper and lower power transistors of the bridge arm structure and ensure the reliability of the motor driver. For GaN drivers on the market today, fixed or configurable dead-time is widely used in more-than-10 MHz application scenarios. However, the switching loss caused by insufficient dead-time and reverse turn-on loss caused by excessive dead-time of GaN devices have a hazardous influence on the efficiency of drivers, which fixed or configurable dead-time cannot avoid. The gate driver with the proposed adaptive dead-time control circuit has been implemented in a 0.18 μm BCD process. The proposed adaptive control circuit dissipates 56.3 μA quiescent current in a simulation situation and is able to provide maximum 5 ns dead-time error for a GaN gate driver.

Keywords: adaptive dead-time control; GaN gate driver; dead-time error



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1. Introduction

As one of the new types of wide bandgap semiconductor devices, GaN high electron mobility devices have lower conduction resistance, smaller junction capacitance, faster switching frequency, and strong temperature resistance ability, as the power devices for motor drives are expected to improve the highest working frequency and efficiency, and in the meantime reduce the volume and weight [1–4]. Thus, it has very broad range of application scenarios for high-speed motor drives, servo drives, electric vehicles, etc.

When the GaN device is applied to the half bridge topology of the motor driver shown in Figure 1, the insertion dead-time can avoid the bridge arm straight-through situation. However, GaN_FET exhibit a larger reverse conduction drop V_{SD} and loss P due to the lack of a body diode, which will affect the efficiency of the system significantly. I_{SD} is the source-drain current, F_s is operating frequency, and T_{conv} is reverse conduction time [5–8].

$$P = V_{SD} * I_{SD} * F_s * T_{conv} \quad (1)$$

Researchers have carried out relevant studies on dead-time optimization settings. Xue J et al. discuss the reverse conduction loss when dead-time is excessive [9]; Zhang Yi et al. discuss the switch loss caused by output capacitance when dead-time is insufficient [7]. Therefore, the best dead-time is that which can not only avoid the switching loss but also reverse conduction loss. If a low-side GaN transistor turned on after V_{sw} becomes 0 V and a high-side power transistor turned on after V_{sw} becomes V_{BUS} , the switching loss can be eliminated. This switching mode mentioned above is called zero voltage switching (ZVS). Hong Y U et al. propose a scheme which is based on detection of switching node voltage and feedback to the gate of the power transistor [10], but this scheme needs a low delay level shift circuit, otherwise it will produce excessive dead-time. Cheng Q et al. designed a dead-time circuit based on detecting load-side current passing through an appropriate delay drive transistor, but it is not suitable for a wide load range or high voltage applications [11]. Xue J et al. carried out design of a dead-time circuit structure

based on detecting the drain-source voltage of a power transistor [9], in which the small detection delay enables the circuit to work under MHz, but it may lead to switching loss. Xugang Ke et al. completed a GaN driver with active BST balance and Vsw dual-edge dead-time modulation, achieving 8.3% efficiency improvement and 3.4 ns constant propagation delay [12], but its maximum voltage level is 40 V.

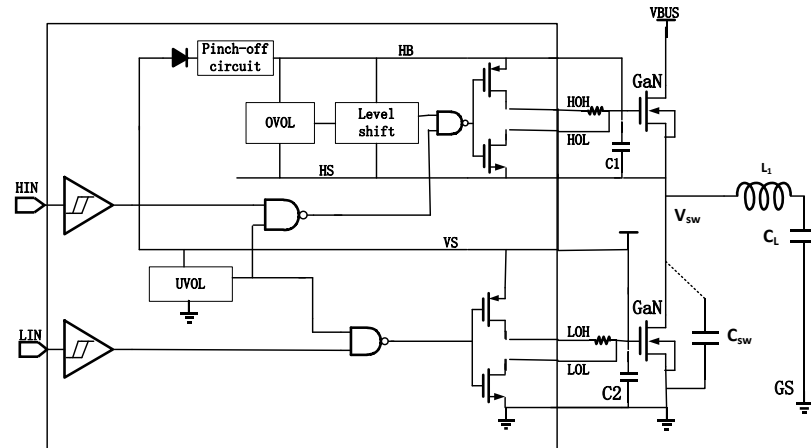


Figure 1. A gate driver of half bridge topology.

Based on the realization of ZVS, the reverse conduction time should be reduced as much as possible to achieve the purpose of reducing the reverse conduction loss by generating appropriate delay according to different load conditions, which can improve the efficiency of the drive circuit. For different load conditions, the slew rate of switch node V_{sw} dissimilates. So, the optimal dead-time T_{opt} should change along with load conditions.

$$T_{opt} = \frac{C_{sw} * V_{BUS}}{I_o} \quad (2)$$

In this formula, C_{sw} is the capacitance of the switch node at the connection point of high and low power transistors, V_{BUS} is bus voltage, I_o is load current. The ideal switching conditions of high- and low-side transistors under different load conditions are shown in Figure 2.

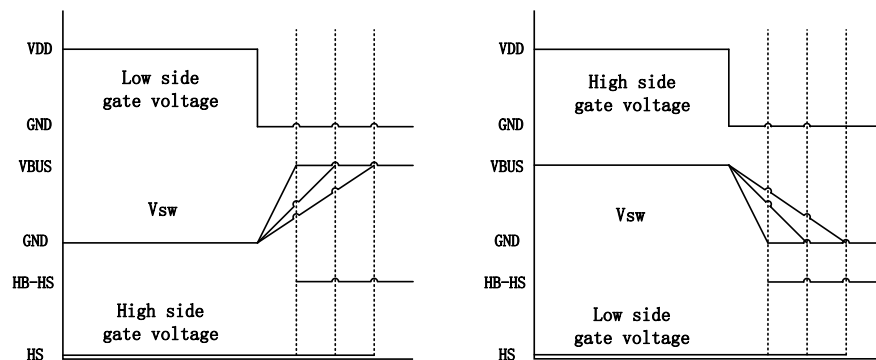


Figure 2. Ideal switching conditions.

To realize ZVS, GaN transistors should turn on when the source-drain voltage drops near to zero. To reduce reverse conduction loss, GaN transistors' turn-on should not be too late after its source-drain voltage drops near to zero. So, this paper proposes an adaptive dead-time control circuit for a maximum work frequency of 20 MHz, maximum voltage level 90 V GaN gate driver, which dissipates 56.3 uA quiescent current and is able to provide maximum 5 ns dead-time error for GaN gate driver.

2. Circuit Structure

The adaptive dead-time circuit proposed in this paper is based on GaN transistors' drain-source voltage detection which belongs to the ipsilateral feedback control; this structure features low delay. The scheme is shown in Figure 3. The adaptive dead-time control circuit includes a Source-Drain Voltage Sense circuit, Current Sense circuit and Delay circuit which can be divided into high-side and low-side. Both high-side and low-side input signal are generated by the forward level shift module in this paper. The subsequent drive module could reverse the V_{OUTH} and V_{OUTL} to V_{GH} and V_{GL} .

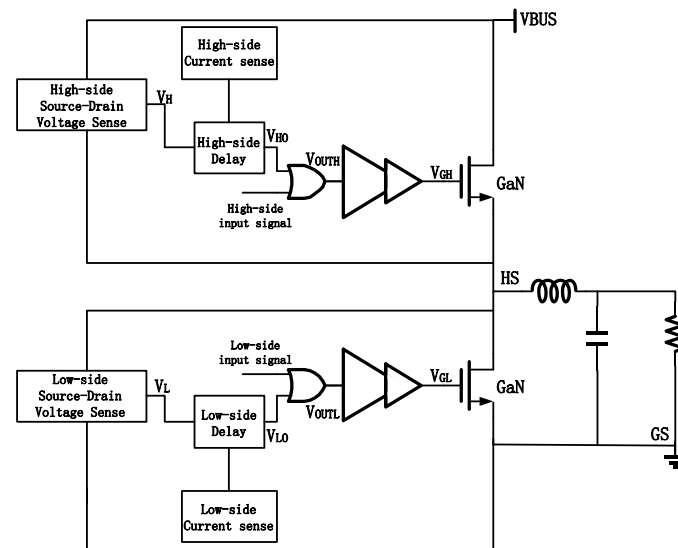


Figure 3. Adaptive dead-time control circuit.

The working waveform is shown in Figure 4, where Delay_H and Delay_L correspond to the delay generated by the high-side delay module and low-side delay module. Dead-time dissimilates along a different delay, V_H and V_L switch when HS starts to switch, and then pass through the delay module which is modulated by Current Sense. Finally, V_{HO} and V_{LO} ORing high-side input signal and low-side input signal to combine turn-on signal and turn-off signal. V_{HO} and V_{LO} provide the turn-on signal while the high-side input signal and low-side input signal provide the turn-off signal. In the meantime, there is a driver (composed of multiple step-step largened buffers to improve current load performance) which possess a delay of about 5 ns (this delay is unavoidable and limits the maximum operating frequency of the gate driver with proposed adaptive dead-time circuit); therefore, we could make V_{OUTH} and V_{OUTL} switch properly or slightly ahead of HS to become 0 V or V_{BUS} in the design of the delay module, and in this way we can reduce the reverse conduction time and maximize operating frequency.

2.1. Source-Drain Voltage Sense Circuit Design

In Figure 5, the proposed Source-Drain Voltage Sense circuit in this paper is displayed. HS is the high-side ground and switch node, MN1 and MP5 are the high voltage LDMOS, and the EN signal works as the fault protection signal. Bipolar Q1 and Q2 clamp the voltage at OUTH and OUTL.

The high-side Source-Drain Sense is showed on the left of the figure; it detects the Source-Drain voltage drop of the high-side GaN transistor—the voltage drop falls when the GaN transistor enters the mill plateau of the turn-on process. MP1 and MN2 are constant turn-on MOSFET, and there is a resistance between MN1's gate and drain which can make MN1 instantaneous turn-on during switching. The input signal of this sense is HS, and transforms the voltage signal into current signal during switching by LDMOS's parasitism, and charge or discharge the upper plate of C_1 ; in this way the current signal transforms into voltage signal at OUTH. When the low-side GaN transistor turns off, HS starts to rise

for the freewheel current of external inductors; while the voltage drops between VBUS and HS start to fall, C_1 starts to discharge from MN2 to MN2, as the charge between C_1 cannot change groundless and MN1 is closed in the beginning, so the charge starts to charge the gate of MN1 through the resistance until MN1 turns on.

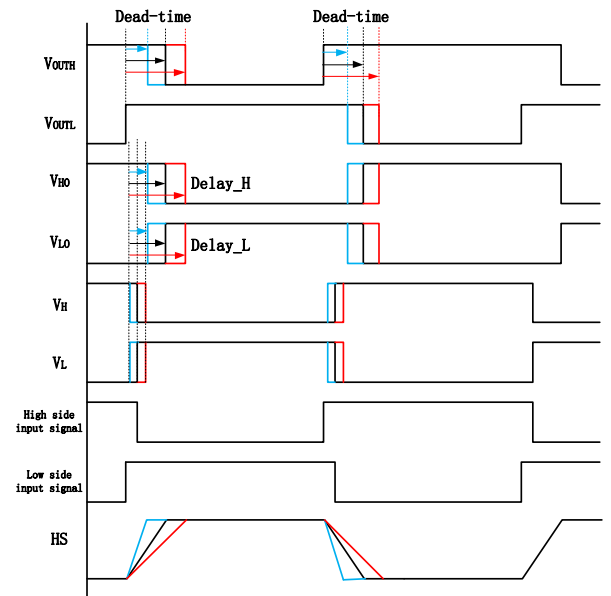


Figure 4. The ideal waveform of adaptive dead-time control circuit.

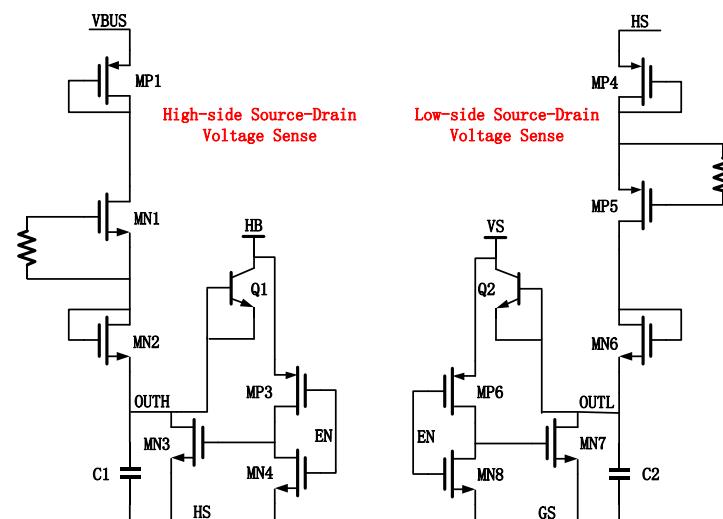


Figure 5. Source-Drain Voltage Sense.

Subsequently, the voltage drops between the upper plate of C_1 and HS falls, and this edge-of-fall works as the enable signal for the following part.

The low-side Source-Drain Sense showed on the right of the figure works in a similar way: when the high-side GaN transistor is turned off, HS starts to fall for the freewheel current of external inductors; while the voltage drop between HS and GS starts to fall, C_2 starts to discharge from MN6 to MP5, for the charge between C_2 cannot change groundless and MP5 is closed in the beginning, so the charge from HS starts to charge the gate of MP5 through the resistance until MP5 is turned on. Subsequently, the voltage drops between the upper plate of C_2 and GS falls, and this edge-of-fall works as the enable signal for the following part. The Sense worked in low quiescent current for a normally closed design.

2.2. Current Sense Circuit Design

The Current Sense Circuit is showed in Figure 6, which is similar to the Source-Drain Sense; the replication of current from VBUS to HS and HS to GS transforms into I_H and I_L . I_H and I_L are used to modulate the delay of the Delay module. It is worth noting that the current would change due to different load conditions (in gate driver means the fall or rise time of HS is different) which corresponds to adaptive adjustment.

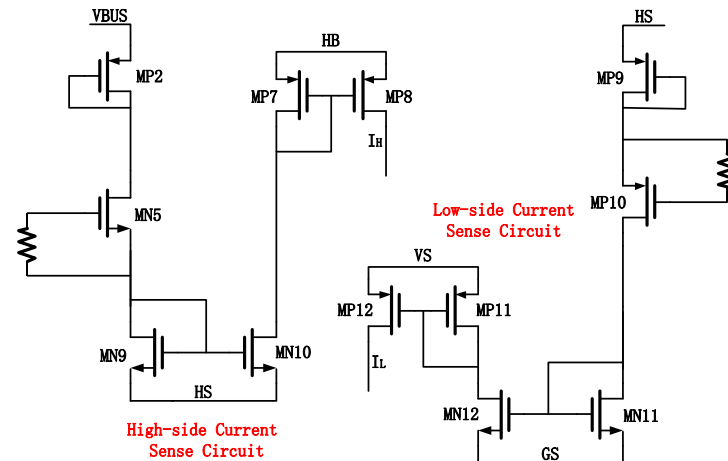


Figure 6. Current Sense Circuit.

2.3. Delay Circuit Design

In Figures 7 and 8, we can see OUTH and OUTL are detected by the threshold of the inverter and modulate the delay by I_H and C_3 or I_L and C_4 into V_{HO} and V_{LO} .

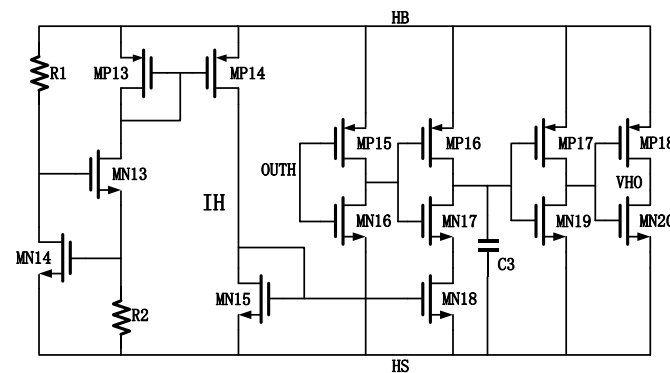


Figure 7. High-side Delay Circuit.

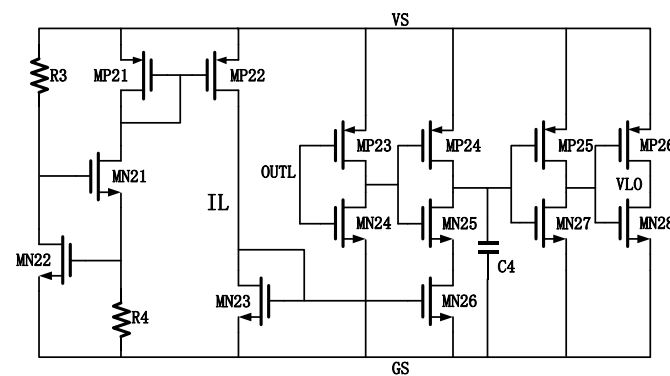


Figure 8. Low-side Delay Circuit.

The delay generated at C_3 can be expressed as T_1 , and the delay generated at C_4 can be expressed as T_2 .

$$T_1 = \frac{C_3 * (V_{HB} - V_{HS})}{I_H + I_{MP14}} \quad (3)$$

$$T_2 = \frac{C_4 * (V_{VS} - V_{GS})}{I_L + I_{MP22}} \quad (4)$$

While the C_3 , C_4 , $V_{HB} - V_{HS}$, $V_{VS} - V_{GS}$, I_{MP14} , I_{MP22} can be regarded as a fixed value, so the delay is only modulated by I_{SEN} (I_L , I_H). To make the delay sensitive only to I_{SEN} , I_{MP14} and I_{MP22} must be insensitive to the supply, so a bias current source is designed as follows.

To achieve a small delay deviation generated by the dead-time control circuit, a current source with low supply sensitivity is designed in Figure 9. When the supply is on, MN22 turns on and provides bias for MN20 and MP17, and the current source starts to provide bias. This structure mainly takes advantage of the fact that MOS saturation current is only relative to overdrive voltage, and MOS resistance can adjust itself along with the current.

$$I = \frac{1}{2} K' \frac{W}{L} (V_{gs} - V_{th})^2 \quad (5)$$

$$R = \frac{1}{K' \frac{W}{L} [V_{gs} - V_{th}]} \quad (6)$$

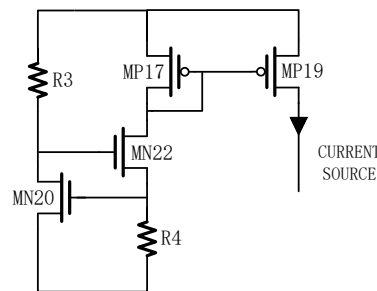


Figure 9. Bias current source.

According to the above formula, it can be concluded that the current and resistance is almost related to $\frac{W}{L}$ and overdrive voltage in the saturated region. It can be concluded from the figure that $V_{DS20} = V_{gs22} + V_{gs20}$. Thus, MN20 is always in the saturated region. According to Ohm's law, we can get (we assume that each transistor threshold is unchanged):

$$V_{gs22} = VS - I_1 R_3 - I_2 R_4 \quad (7)$$

$$I_1 = \frac{1}{2} K' \frac{W_{20}}{L_{20}} (V_{gs20} - V_{th})^2 \quad (8)$$

$$I_2 = \frac{1}{2} K' \frac{W_{22}}{L_{22}} (V_{gs22} - V_{th})^2 \quad (9)$$

$$V_{gs20} = I_2 R_4 \quad (10)$$

I_1 is the current through R_3 and I_2 is the current through R_4 , then we can get:

$$VS = V_{gs22} + \left[\frac{1}{2} K' \frac{W_{20}}{L_{20}} \left(\left[\frac{1}{2} K' \frac{W_{22}}{L_{22}} (V_{gs22} - V_{th})^2 \right] R_4 - V_{th} \right)^2 \right] R_3 + \frac{1}{2} K' \frac{W_{22}}{L_{22}} (V_{gs22} - V_{th})^2 R_4 \quad (11)$$

In this formula, VS and V_{gs22} are variables, and we want to figure out $\frac{dV_{gs22}}{dVS}$, but the order of V_{gs22} in this formula is four times, so figuring out $\frac{dVS}{dV_{gs22}}$ and reversing it is more efficient.

$$\frac{dV_S}{dV_{GS22}} = 1 + \left[K' \frac{W_{22}}{L_{22}} (V_{GS22} - V_{th}) R_4 \right] \left[1 + K' \frac{W_{20}}{L_{20}} R_3 \right] \left[\frac{1}{2} K' \frac{W_{22}}{L_{22}} (V_{GS22} - V_{th})^2 R_4 - V_{th} \right] \quad (12)$$

Taking the typical value and calculating it equals around 50; its reciprocal is 0.02, which means V_{GS22} changes 0.02 V per 1 V V_S . It can be seen that this is a fixed voltage within the working range of 4–5 V. In this way, we can obtain a current source insensitive to supply, which provides bias for the following module by coping the current through MN17 (of course, we ignore the influence of body effect and temperature drift, etc.).

However, in practical applications, the dead-time is slightly larger than the ideal condition, so there is still reverse conduction loss. We must reduce the deviation to small enough to minimize the reverse conduction loss by reasonably adjusting the capacitance and extra current generated by the Current Source.

3. Simulation Results

Dead-time error is divided into high-side dead-time error and low-side dead-time error. High-side dead-time error refers to the delay between high-side dead-time and high-side best dead-time; high-side dead-time is the interval time between low-side power device shut off and high-side power device turn on; high-side best dead-time is the time the HS rises from ground to VBUS, so the high-side dead-time error is the delay between when switching node HS becomes VBUS and the high-side dead-time control circuit generates the enable signal, which is also the high-side reverse conduction time. Low-side dead-time error refers to the delay between low-side dead-time and low-side best dead-time; low-side dead-time is the interval time between high-side power device shut off and low-side power device turn on; low-side best dead-time is the time during which HS falls from VBUS to ground, so the low-side dead-time error is the delay between when switching node HS becomes 0 V and the low-side dead-time control circuit generates the enable signal, which also is the low-side reverse conduction time.

The adaptive dead-time control circuit's input signal is HS voltage, designed in this paper. The simulation condition requires that VBUS equals 90 V while the time of HS falling or rising $\frac{dV}{dt}$ is divided into 90 V/ns, 45 V/ns, and 30 V/ns.

In Figure 10a,b, we can see that VH and VL can collect the switching point correctly; in Figure 10c–f we can see that the Current Sense circuit can generate a different current according to different load conditions.

The following simulation condition requires that VBUS equals 90 V while the time of HS falling or rising $\frac{dV}{dt}$ is divided into 90 V/ns, 45 V/ns, 30 V/ns, and 15 V/ns.

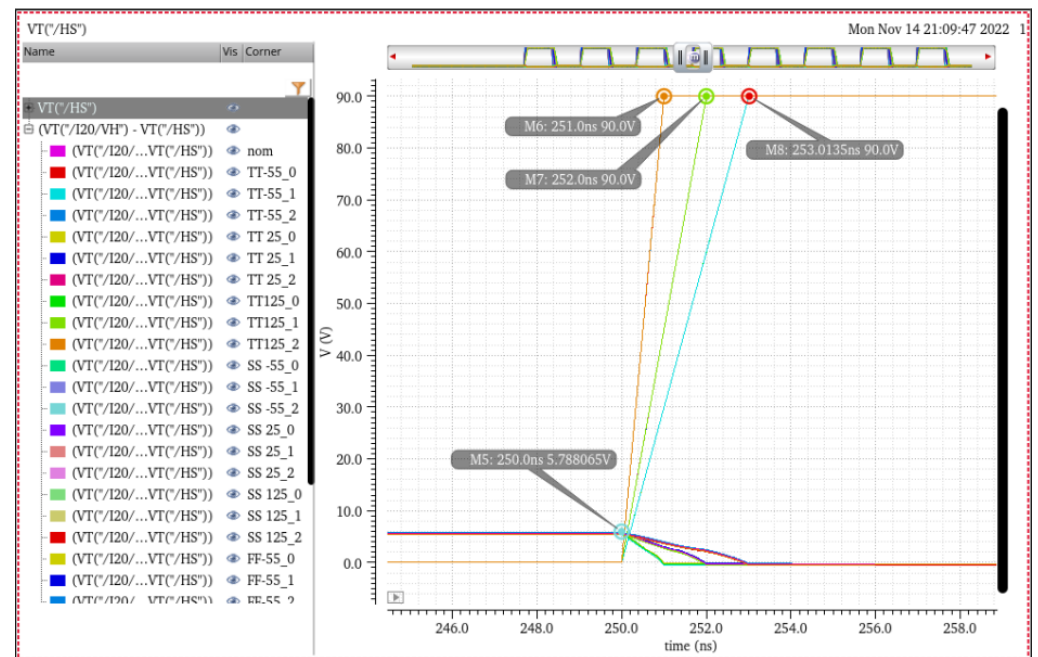
As we can see in Figure 11, dead-time control output VHO and VLO error is within -2.5 ns to 2 ns, while the following driver module delay is about 5 ns, which can match the negative error to maximum working frequency.

Figure 12 shows the proposed gate driver's function; we can see in TT 27 °C V_{GL} and V_{GH} (in Figure 3) would not pass straight through, and V_{GL} rises after HS turns to ground, V_{GH} rises after HS turns to VBUS, and dead-time error is 4 ns. In all corners (TT, SS, FF, $\frac{dV}{dt}$ is divided into 90 V/ns, 45 V/ns, 30 V/ns, and 15 V/ns) dead-time error is within 5 ns.

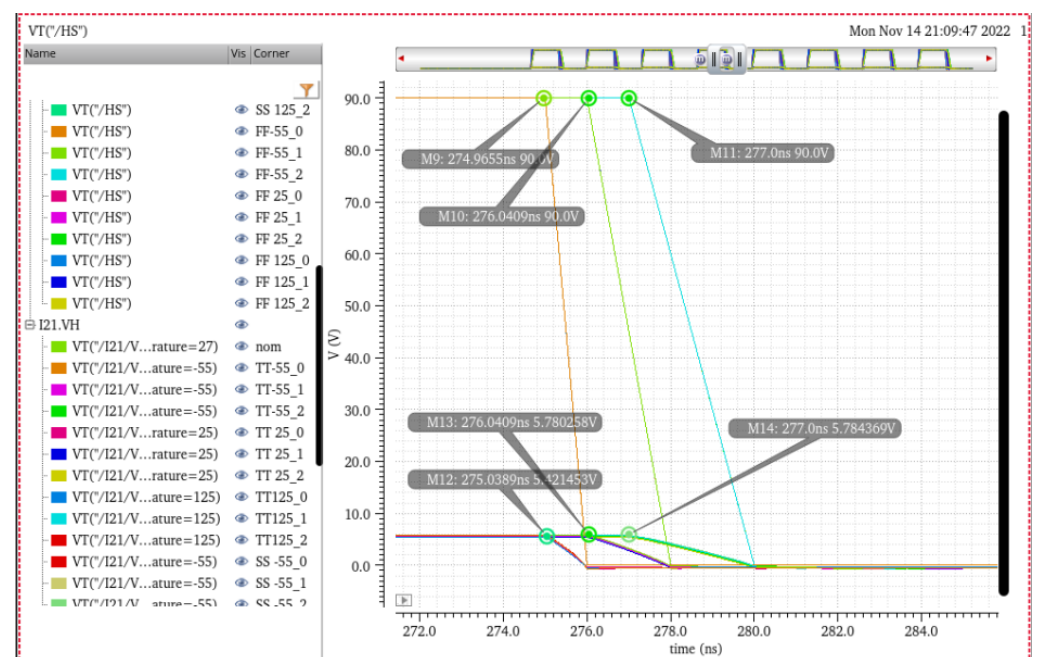
As is shown in Table 1, this work may provide longer dead-time than previous work, but this work can work at higher voltage and consider higher dv/dt (it can work correctly when $dv/dt = 90$ V/ns). Furthermore, this work considers switching loss, so the dead-time is changed according to the rise/fall edge time which called adaptive dead-time control design.

Table 1. Performance comparison.

Design	ISSCC 2016 [12]	EPC AN015 [13]	This Work
Power Switches	GaN	GaN	GaN
Working frequency	10–30 MHz	10 MHz	20 MHz
Dead-time	3.7, 0.9 ns	8 ns	F/R time+(<5 ns)
Dead-time error	/	/	Within 5 ns
V _{BUS} voltage	3–40 V	42 V	90 V

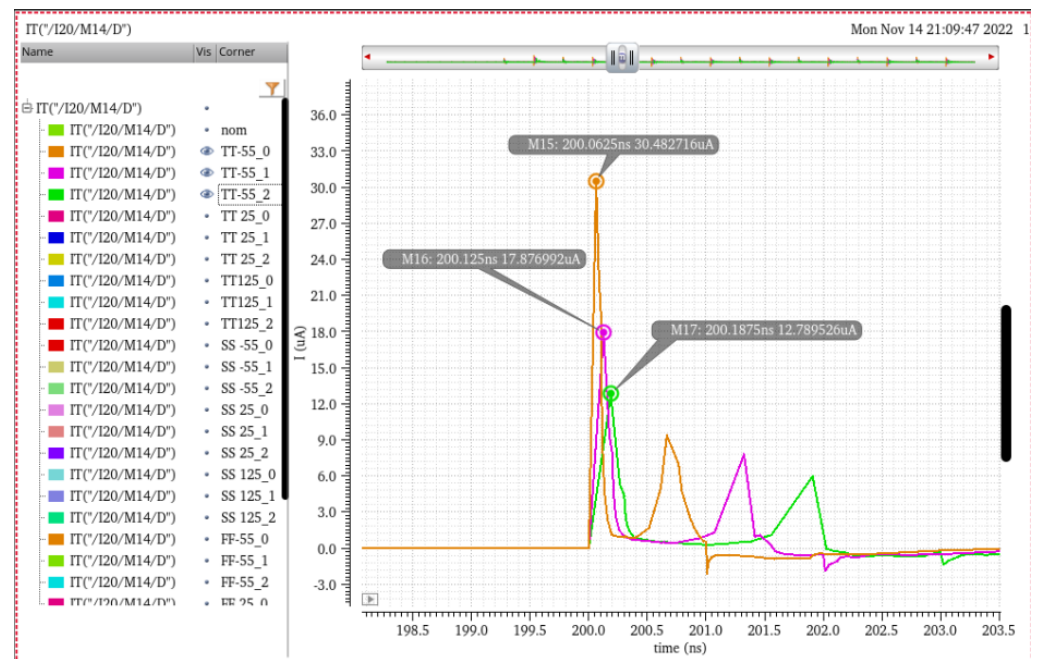


(a)

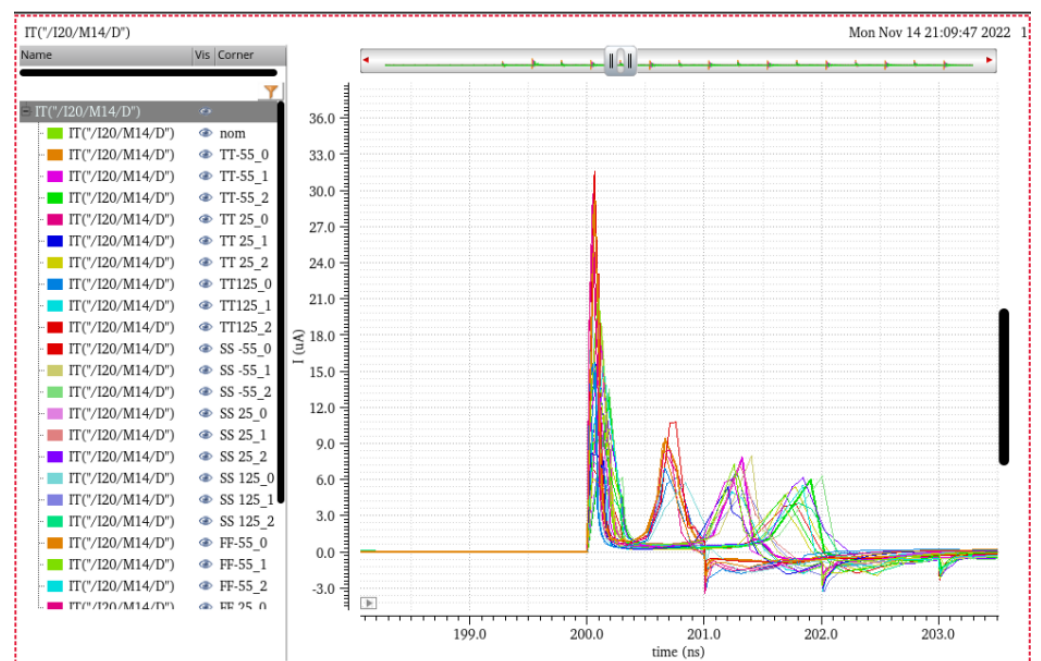


(b)

Figure 10. Cont.

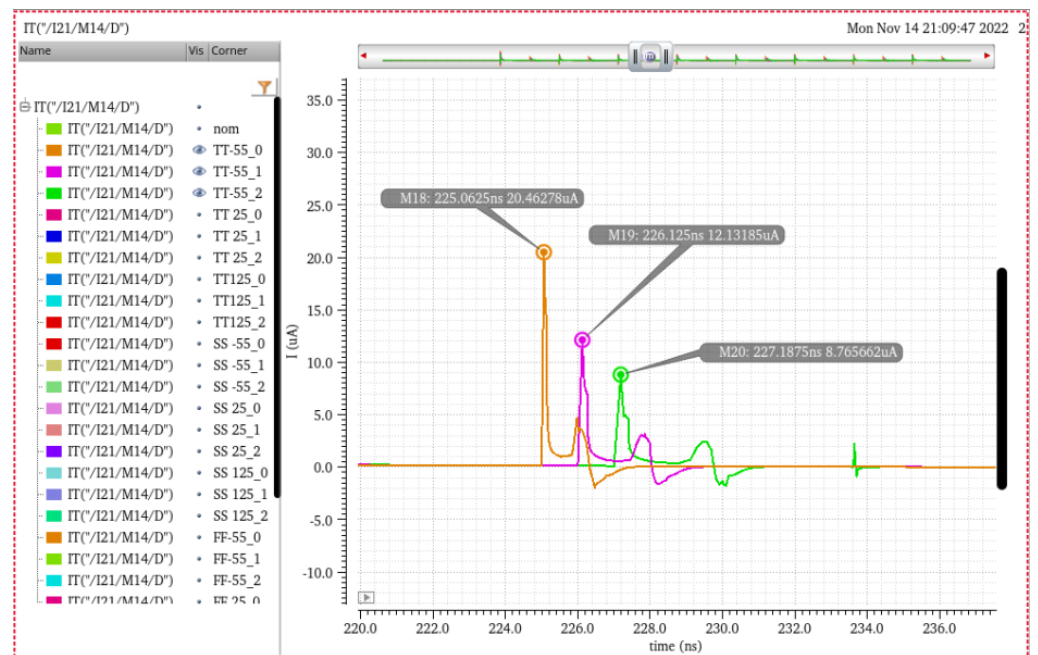


(c)

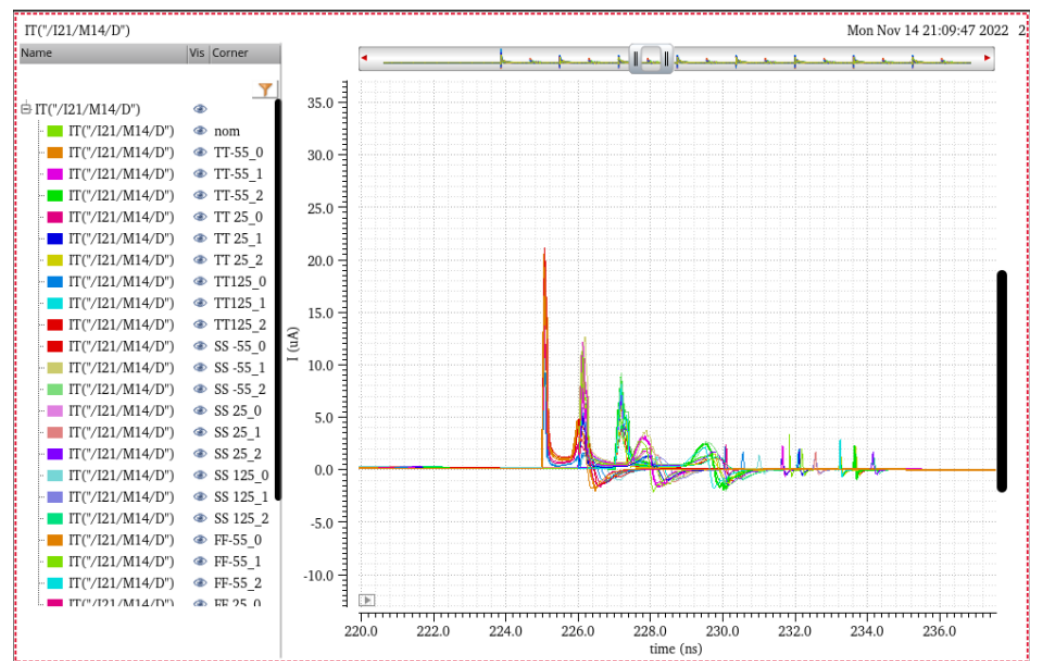


(d)

Figure 10. Cont.

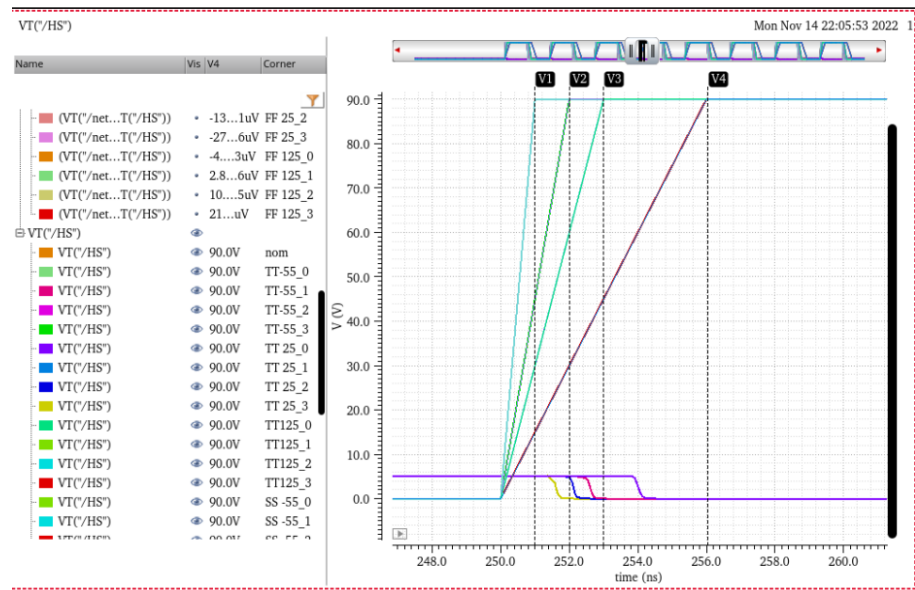


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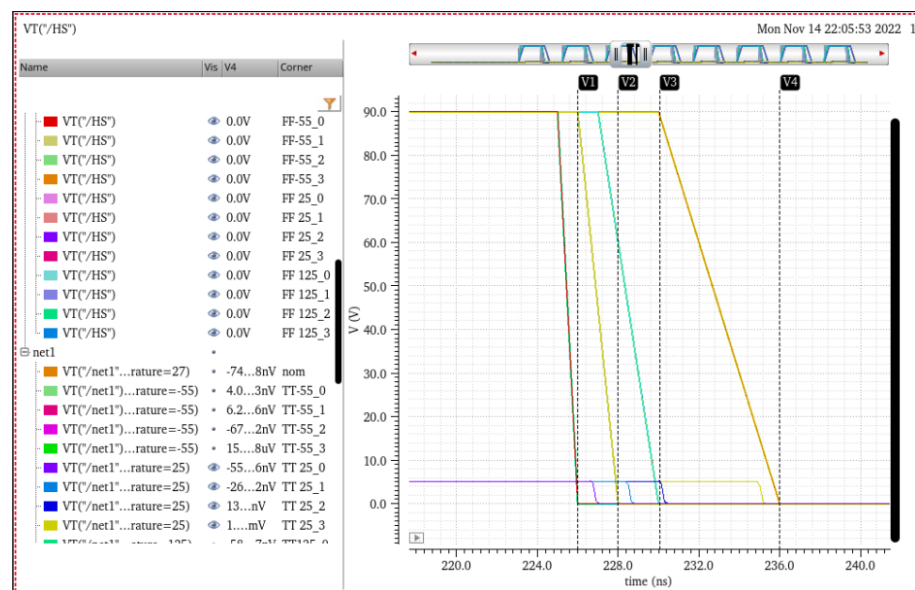


(f)

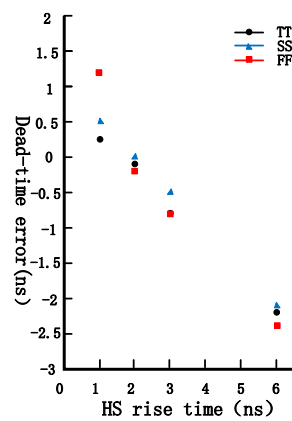
Figure 10. (a) High-side Source to Drain Sense circuit simulation (b) Low-side Source to Drain Sense circuit simulation (c) High-side Current Sense circuit simulation in TT -55°C (d) High-side Current Sense circuit simulation in TT SS FF (e) Low-side Current Sense circuit simulation in TT -55°C (f) Low-side Current Sense circuit simulation in TT SS FF.



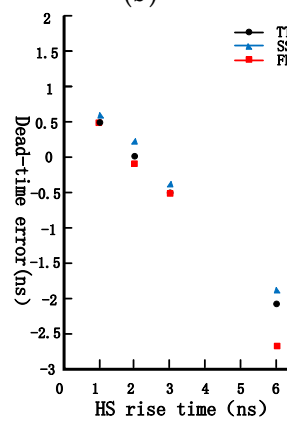
(a)



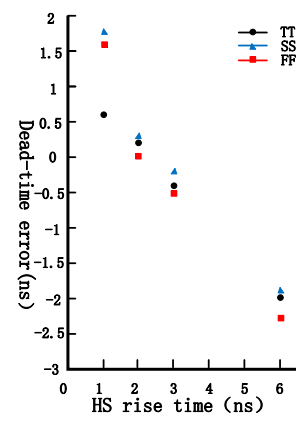
(b)



(c)



(d)



(e)

Figure 11. Cont.

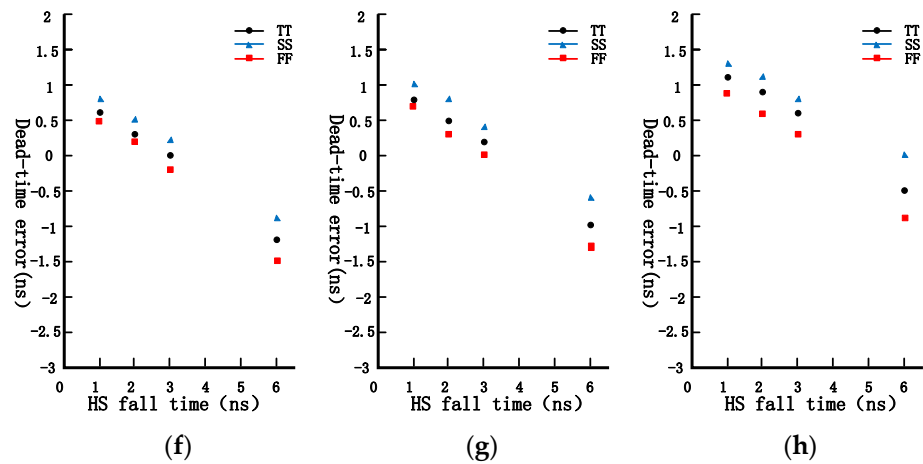


Figure 11. (a) High-side dead-time control circuit VHO simulation (b) Low-side dead-time control circuit VLO simulation (c) High-side dead-time control signal VHO error in $-55\text{ }^{\circ}\text{C}$ (d) High-side dead-time control signal VHO error in $25\text{ }^{\circ}\text{C}$ (e) High-side dead-time control signal VHO error in $125\text{ }^{\circ}\text{C}$ (f) Low-side dead-time control signal VLO error in $-55\text{ }^{\circ}\text{C}$ (g) Low-side dead-time control signal VLO error at $25\text{ }^{\circ}\text{C}$ (h) Low-side dead-time control signal VLO error at $125\text{ }^{\circ}\text{C}$.

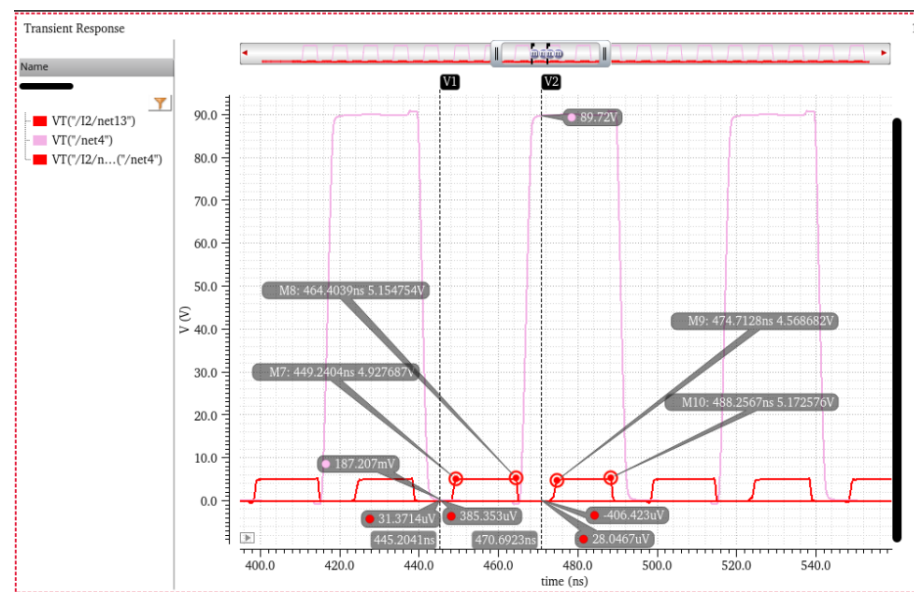


Figure 12. Overall simulation.

4. Conclusions

The gate driver with the proposed adaptive dead-time control circuit has been implemented in a $0.18\text{ }\mu\text{m}$ BCD process. The proposed adaptive control circuit dissipates $56.3\text{ }\mu\text{A}$ quiescent current in simulation situations and can provide a maximum 5 ns dead-time error for GaN gate driver. Distinguished from other related designs, this work can avoid switching loss completely, and modulate dead-time along with the fall/rise time of HS edge. The test result in Figures 13 and 14 prove it can transfer signal correctly within a 5 ns dead-time error. However, this does not complete efficiency measurement, with which this work could measure the actual efficiency improvement. In simulations for 90 V to 42 V and 20 MHz conversion, it can achieve 93.96% efficiency when load current I_o is 1 A .

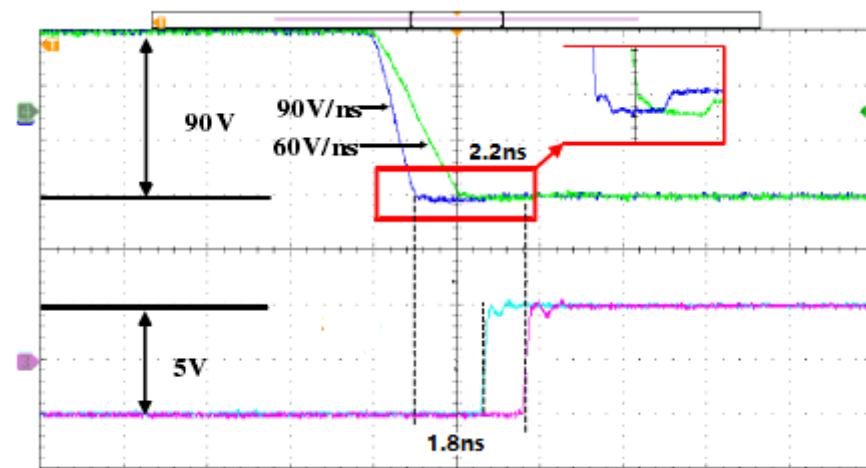


Figure 13. Low-side test results.

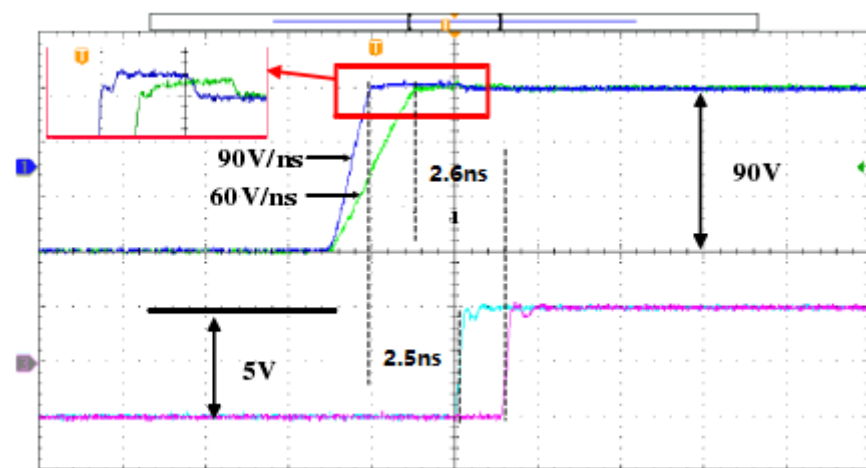


Figure 14. High-side test results.

Author Contributions: Conceptualization, Y.W. (Yong Wang) and Y.K.; methodology, Y.W. (Ying Wang); software, L.P.; validation, Y.H., L.P., and Y.W. (Ying Wang); formal analysis, Y.H.; investigation, Y.H.; resources, Y.W. (Yong Wang); data curation, Y.H.; writing—original draft preparation, Y.H.; writing—review and editing, Y.H.; visualization, Y.H., Y.W. (Yong Wang) and Y.W. (Ying Wang); project administration, Y.K.; funding acquisition, Y.W. (Yong Wang) All authors have read and agreed to the published version of the manuscript.

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