electronics

MDPI

Article

Design Automation of Low Dropout Voltage Regulators: A General Approach

Karimeldeen Mohamed [1,*], Sherif Nafea [1] and Hesham Omran [2,*]

[1] Department of Electrical Engineering, Suez Canal University, Ismailia 41522, Egypt
[2] Integrated Circuits Laboratory (ICL), Faculty of Engineering, Ain Shams University, Cairo 11517, Egypt
* Correspondence: karimeldeen.mohamed@eng.suez.edu.eg (K.M.); hesham.omran@eng.asu.edu.eg (H.O.)

Abstract: Analog design is an inherently intricate process comprising many trade-offs; as a result, it is an iterative time-consuming operation. A low dropout voltage regulator (LDO) is an example of such analog blocks that involve a myriad of trade-offs. In this paper, we present an automated design procedure for LDOs using precomputed look-up tables (LUTs) and the g_m/I_D methodology. Using a symbolic solver and the precomputed LUTs, a design database for an LDO that contains one million design points is generated in a few seconds. The database provides visualization of the design space and exploration of the trade-offs across different corners and load currents. A design example is provided to demonstrate the procedure using 40 nm technology and the results are verified using Cadence Spectre simulator. The approach is holistic in the sense that it uses an accurate symbolic solver to capture the small signal model complexities, incorporates LUTs for accurate calculation of the large signal solution and the small signal parameters, is fast because the simulator in the loop scenario is omitted, and almost all the specifications of LDOs are incorporated.

Keywords: analog design automation; g_m/I_D methodology; low dropout regulators (LDOs); precomputed lookup tables; regulators

Citation: Mohamed, K.; Nafea, S.; Omran, H. Design Automation of Low Dropout Voltage Regulators: A General Approach. *Electronics* **2023**, *12*, 205. https://doi.org/10.3390/electronics12010205

Academic Editors: Andrea Ballo, Gaetano Palumbo and Orazio Aiello

Received: 29 November 2022
Revised: 26 December 2022
Accepted: 26 December 2022
Published: 31 December 2022

1. Introduction

Although analog IC design requires creativity, the analog IC design flow has been almost the same for more than 50 years. With only minor incremental improvements, the design flow lacks methodological cogitation. The analog design process starts with specifications entailed by the system. The designer then relies on his experience along with back-and-forth iterative simulator sweeps until a satisfactory design point is reached. In addition to being a manual and tedious process, the result is not guaranteed to be optimal. These lengthy manual iterations waste considerable time making analog design the bottleneck in a digital-driven system-on-a-chip market.

The lack of a systematic analog design approach is the result of two main factors. First, as the transistor size is scaled down, or the device is biased in moderate or weak inversion, the widely-known simple MOSFET square model fails to capture the actual device behavior. Thus, a design procedure that relies on simple long-channel models suffers from degraded accuracy. On the other hand, more accurate models are too complicated and do not lend themselves to equation-based methodologies. Second, when the circuit includes more transistors, the small signal analysis quickly turns into a burden, and brute force mesh and nodal analysis equations become intractable, and they hardly provide any design insight. Design-oriented analysis methods such as the N-extra elements method [1], and its modern variant, the generalized time and transfer constant method [2], provide more efficient analysis techniques. However, to benefit from their invaluable efficacy in design, many approximations still need to be completed. In addition, modifying the simplified textbook MOSFET small signal model [3] to account for parasitic resistances and the parasitic drain-source capacitance (*cds*) in deep sub-micron technologies renders the analysis impractical.

As a remedy for the first limitation, the g_m/I_D design methodology [4–6] along with precomputed lookup tables (LUTs) come into play. The versatility of the g_m/I_D design methodology made it a powerful choice for analog design automation [7–11]. The key notion of the methodology is that the g_m/I_D defines the inversion level of the transistor regardless of the bias current (I_D) and the device length (L); hence g_m/I_D can be used as an orthogonal and normalized design knob for the transistor bias point. The orthogonality of g_m/I_D, L and I_D provides a systematic design and fair exploration of the design trade-offs. To invoke the methodology in an analog design automation procedure, the LUTs are built using a circuit simulator that uses the most accurate device models, thus dismissing the need to use simple approximate models. This procedure bridges the aforementioned gap and facilitates calculation of the different device parameters accurately. Furthermore, the process of LUT generation is performed once per technology. Regarding the second shortcoming, using a fast small signal symbolic solver that can easily accommodate different technology parasitics is an effective solution. Nonetheless, rough hand analysis is indispensable as qualitative guidance to understand the design trade-offs and to define a reasonable search space.

Low-dropout regulators (LDOs) are imperative in modern system-on-chips (SoCs) given the continuous downscaling of the supply voltage and the inherently noisy environment of SoC. Owing to the nature of the LDO being an analog block, its design is not a straightforward task, as it involves many trade-offs, design variables, and degrees of freedom. Finding a design point that meets all the specifications is complicated. Several attempts have been made to automate or optimize the design of LDOs. In [12], an equation-based optimization scheme is adopted. A surrogate model for the LDO is used from which design equations are derived. Physics-based models along with curve fitting are used to approximate the small signal behavior of the transistors. Although fast, this approach lacks accuracy due to the approximations made in the equations and the device models. Similarly, the work in [13,14] used the same equation-based optimization scheme. In the former study, equations were formulated using the g_m/I_D methodology, leading to the use of rough approximations. In addition, the settling time is reported without explicit mention of the calculation method. The latter formulated the equations in a posynomial form to be able to use geometrical programming. However, the posynomial model accuracy deteriorates at short channel lengths. In [15,16], simulation-based optimization is used. Simulation-based approaches are more accurate. Nonetheless, a very high computational power is needed and a large amount of time is required. Moreover, the previous attempts did not provide design space visualization under different constraints.

In this paper, we present a general automated design flow for LDOs that overcomes the accuracy and speed limitations of the approaches reported in the literature, incorporates line transient regulation with accuracy and speed, and considers the systematic mismatch forced by the feedback in both the design and evaluation of the specifications. The rest of the paper is organized as follows. Section 2 presents an overview of LDO specifications. Section 3 describes the automation flow along with an explanation of how the specifications are calculated. Results and design examples are provided in Section 4. Section 5 concludes the paper.

2. LDO Specifications Overview

This section provides an overview of the LDO specifications that will be considered in our design procedure. A rough hand analysis is carried out for the sake of completeness and to illustrate the design trade-offs presented in Section 4. Figure 1 shows the schematic of the LDO used as an example in this paper. A simple architecture is chosen to elaborate on the design flow. However, the flow is general, and can be applied to any other architecture. $M_{1a,b}$, $M_{2a,b}$, and M_4 constitute the LDO error amplifier, M_3 is the pass device used to supply the current to the load. I_L and C_L are the current drawn by the load and the capacitance of the load, respectively. R1 and R2 are the resistive feedback network that determines the ratio between the reference voltage V_{ref} and the output voltage of the

regulator V_{reg}. Finally, C_C is the miller compensation capacitor used to ensure stability. The considered LDO specifications are presented in the following subsections.

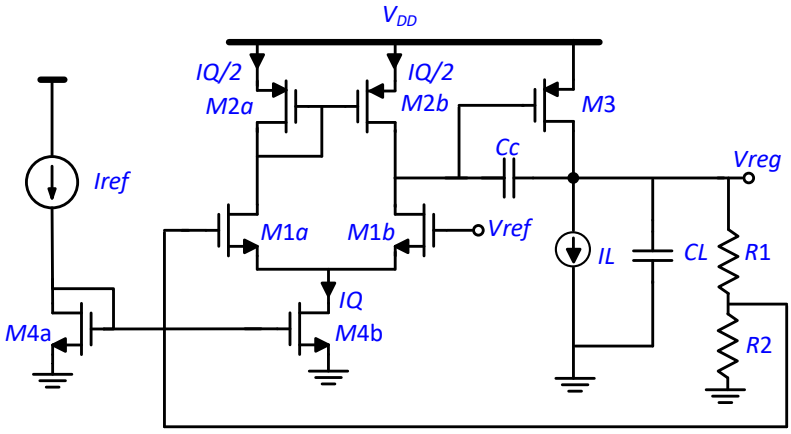


Figure 1. Circuit diagram of the LDO.

2.1. Dropout Voltage

The dropout voltage is defined as the minimum difference between the input (V_{DD}) and the output (V_{reg}), such that the regulation is maintained [17]. As this is the minimum value of V_{DS} of M_3, the dropout can be considered as its saturation voltage (V_{DSAT}). A smaller dropout at a given load current implies a wider device.

2.2. Loop Gain

Cutting the feedback loop at the gate of M_{1a}, the loop gain is obtained as follows:

$$LG_{DC} \approx \frac{g_{m1a,b}}{(g_{ds2a,b} + g_{ds1a,b})} \frac{g_{m3}}{g_{ds3} + Y_L} \frac{R_2}{R_1 + R_2} \tag{1}$$

where Y_L is the equivalent load resistance and the term $(R_1 + R_2)^{-1}$ is omitted from the addition in the denominator of the second term, as these resistors are usually relatively large. The Miller effect causes pole splitting, leading the dominant pole at the gate of the pass device to be

$$\omega_{P1} \approx \frac{(g_{ds3} + Y_L)(g_{ds2a,b} + g_{ds1a,b})}{g_{m3}(C_C + C_{gd3})} \tag{2}$$

while the non-dominant pole is at the output node and is obtained by

$$\omega_{P2} \approx \frac{g_{m3} + g_{ds3} + Y_L}{C_L} \tag{3}$$

given that $C_c + C_{gd3} \gg C_{gs3}$. If the previous inequality is not satisfied, the phase margin (PM) will exhibit strong dependence on Y_L. Additionally, a zero exists at $\omega_Z \approx \frac{g_{m3}}{C_C}$. The overall loop gain can be written as

$$LG(s) \approx LG_{DC} \frac{(1 - \frac{s}{\omega_Z})}{(1 + \frac{s}{\omega_{p1}})(1 + \frac{s}{\omega_{P2}})} \tag{4}$$

2.3. Load Regulation

Load regulation is the change of the regulated output voltage with respect to the change in the load current, i.e., $\frac{\partial V_{reg}}{\partial I_L}$. As noted in the definition, this represents the output impedance of the LDO. The output impedance is the parallel combination of Y_L, g_{ds3},

$(R_1 + R_2)$ and the closed-loop output impedance of the pass device R_{out3}. The pass device can be thought of as being diode-connected with its g_m boosted by the amplifier [18]; hence,

$$R_{out3} \approx \frac{(g_{ds1a,b} + g_{ds2a,b})}{g_{m3}g_{m1a,b}}(1 + \frac{R_1}{R_2}) \tag{5}$$

The load regulation expression is dominated by the last term being much smaller than the others. As a result, load regulation is expressed as

$$L_{DR} \approx \frac{(g_{ds1a,b} + g_{ds2a,b})}{g_{m3}g_{m1a,b}}(1 + \frac{R_1}{R_2}) \approx \frac{1}{g_{ds3}LG_{DC}} \tag{6}$$

the previous expression is sometimes referred to as AC load regulation, as it relates small changes in the load current to changes in the regulated voltage. The DC load regulation, defined as $\frac{\triangle V_{reg}}{\triangle I_L}$, is related to the AC load regulation as follows:

$$L_{DR_{DC}} = \frac{1}{\triangle I_L}\int L_{DR_{AC}}\, dI_L \tag{7}$$

Since the integral is a linear operator, decreasing the AC load regulation necessarily decreases the DC load regulation, which is intuitive. Load transient regulation involves adding a load current transient step and observing the regulated output voltage. However, the analysis of the load transient is not straightforward due to the strong dependence of the small signal parameters on the load current, along with the presence of a large signal behavior; the slew rate [19].

2.4. Power Supply Rejection (PSR)

PSR is an important specification that reflects the LDO ability to shield the load from supply variations. There are two paths from which the supply noise can propagate to the output, namely, from the gate-source voltage of the pass device and through its small signal output resistance g_{ds3}. The used amplifier topology is type A; hence, $PSR_{Amp} \approx 1$ [19]. Since the gate of the pass device tracks its source, the propagation of the first path is neglected. The contribution of the second path can be thought of as a voltage divider between $R_{out3}||Z_{Ltot}$ and g_{ds3} where $Z_{Ltot} = Y_L^{-1}||\frac{1}{SC_L}||(R1 + R2)$; hence, the PSR can be written as

$$PSR_{DC} \approx \frac{g_{ds3}(g_{ds1a,b} + g_{ds2a,b})}{g_{m3}g_{m1a,b}}(1 + \frac{R_1}{R_2}) \approx \frac{1}{LG_{DC}} \tag{8}$$

where Z_{Ltot} is neglected at low frequencies. To account for frequency dependence, the same voltage divider principle is used with the following modification: $R_{out3} \approx \frac{1}{g_{ds3}LG_{DC}}(1 + \frac{S}{\omega_{p1}})$. After some algebraic manipulations, it can be shown that

$$PSR(s) \approx PSR_{DC}\frac{(1 + \frac{s}{\omega_{P1}})}{(1 + \frac{s}{LG_{DC}\omega_{P1}})(1 + \frac{s}{\omega'_{P2}})} \tag{9}$$

where

$$\omega'_{P2} \approx \frac{1}{C_L(Y_L^{-1}||(R1 + R2))} \tag{10}$$

The DC counterpart of PSR is line regulation. Same as the DC load regulation,

$$L_R = \frac{1}{\triangle V_{DD}}\int PSR_{DC}\, dV_{DD} \tag{11}$$

Nevertheless, at a fixed load current, approximating the line regulation to be PSR is quite accurate owing to the high linearity implied by the feedback. An accurate method to compute the line transient from PSR is proposed in Section 3.

2.5. Output Noise

The main noise sources in the LDO are: the amplifier noise modeled as input referred voltage noise $\overline{V_{n,Amp}^2}$, the pass device noise modeled by its gate referred voltage $\overline{V_{n,3}^2}$, which can be divided by the amplifier gain, A_{vamp}^2, to be placed in series with $\overline{V_{n,Amp}^2}$, and the resistors noise. The noise current of both resistors flow through R_1, producing $\overline{V_{n,R}^2} = 4kTR_1(1 + \frac{R_1}{R_2})$ at the output. The total output noise can be written as follows:

$$\overline{V_{n,out}^2} \approx (1 + \frac{R_1}{R_2})^2(\overline{V_{n,Amp}^2} + \frac{\overline{V_{n,3}^2}}{A_{vamp}^2} + 4kT(R_1||R_2)) \tag{12}$$

3. Design Automation Procedure

The design automation procedure main flow is shown in Figure 2. The flow uses precomputed LUTs that store the large signal and small signal behavior of the devices, in addition to automatically generated symbolic expressions of the performance metrics. An array of design points that uniformly covers the design space of interest is used. A vectorized evaluation of the design metrics is performed to compute the DC solution, in addition to the substitution in the symbolic solver equations. The flow is detailed in the following sub-sections.

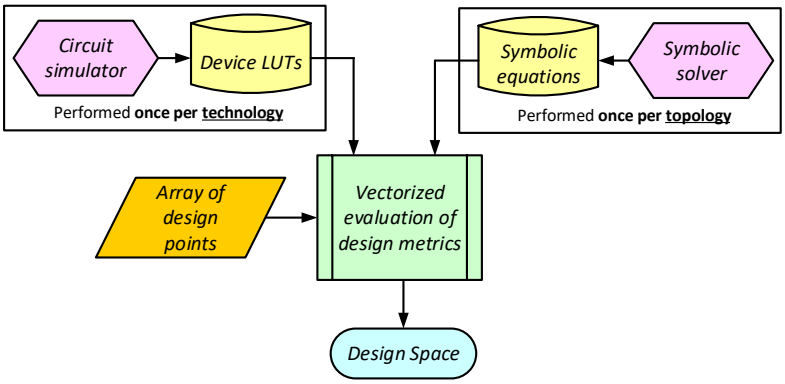


Figure 2. Design automation procedure flow.

3.1. LUTs Generation

The process of LUT generation for the transistors is achieved by performing sweeps across four main grid axes $(V_{GS}, L, V_{DS}, V_{SB})$. The characterization is performed at a single reference width $Wref$, since for a given bias point the parameters of the MOSFET scale linearly with the width, which facilitates the calculation of the large signal current and the small signal parameters at any given width using simple linear scaling. At each grid point, OP and noise analyses are carried out to obtain the DC, the small signal, and the noise parameters of the device. These parameters are stored in 4D arrays. Post-processing is performed to facilitate inverse lookup, i.e., looking up the parameters using g_m/I_D as the main axis instead of V_{GS}, as dictated by the g_m/I_D methodology. All the lookup operations and off-grid points interpolations are carried out according to the method proposed in [20] to ensure accuracy, speed, and practical LUTs size. The simulator is invoked in the LUT generation step only. The used LUT size is 780 MB (one for NMOS and one for PMOS). Each LUT has two corners, namely TT at 27 °C and SS at 75 °C. The sampling of the parameters is as follows:

- $Wref$: 1 µ
- L: 40 n:0.02 µ:0.5 µ, 0.6 µ:0.1 µ:1 µ, 1.2 µ:0.2 µ:2 µ, 2 µ:0.5 µ:6 µ
- V_{GS}: 0:20 m:1.2
- V_{DS}: 25 m:25 m:1.2
- V_{SB}: 0:50 m:1.2

The sampling step is fine for V_{GS} and relatively coarse for V_{DS} and V_{SB} since V_{GS} is the primary variable controlling the transistor behavior. The LUT complete generation process required 4 h. However, this process is performed once per technology.

3.2. The Symbolic Solver

A custom-written symbolic solver with Python is used to calculate the small signal transfer functions of the circuit. The input to the symbolic solver is the circuit netlist. The netlist is parsed by a custom-written parser and each MOSFET is replaced by its small signal equivalent model. This model can be modified easily to account for different parasitics according to the technology under consideration. Alternatively, the small signal model can be fixed and the effective small signal parameters are extracted to account for the parasitics. A matrix of the circuit is built based on a modified nodal analysis (MNA) and transfer functions are calculated by solving the linear matrix. In the noise analysis, the equivalent noise current source of each MOSFET is placed in the model between the drain and the source of the MOSFET; then, the total noise contribution at the output can be calculated by superposition. For loop gain calculation, the loading effects and bilaterality of the loop are taken into consideration by applying the loop-based method described in [21], which yields highly accurate results at all frequencies of interest. The output expressions are then stored to be used during the design database generation. Editing the netlist or adding a new netlist for another topology does not require any additional coding. The procedure of generating the symbolic expressions is performed once per topology.

3.3. Corners and Degrees of Freedom (DoFs)

Corners can be defined as the global variables for which the whole circuit is solved and the specifications are evaluated. In addition to the MOSFET process corners, temperature, and V_{DD}, the load current (I_L), the load capacitance(C_L), and the reference voltage (V_{ref}) are considered as corners. The degrees of freedom (DoFs) are the independent variables of the circuit for which the design is evaluated for each DoFs combination. The DoFs are mainly the g_m/I_D, I_D, and L of each device in addition to other circuit and topologically imposed DoFs. These DoFs are set to random values between a user-defined minimum and maximum value for each DOF. Table 1 demonstrates the corners and DoFs for the LDO design problem under consideration.

Table 1. Corners and DoFs for the LDO.

Corners	DoFs
MOSFET Process Corners	$M_1(L)$
Temp	$M_2(L)$
V_{DD}	$M_3(L)$
I_L	$M_4(L)$
C_L	$M_1(g_m/I_D)$
V_{ref}	$M_2(g_m/I_D)$
$IQ/IQ_{Nominal}$	$M_3(g_m/I_D)$
	$M_4(g_m/I_D)$
	V_{reg}
	I_Q
	C_C
	R_1

3.4. Design and Solve Modes

Circuit design (determining device widths given the g_m/I_D) is performed at the typical corner which is designated by the largest load current supplied by the LDO. As a result, the pass device is guaranteed to be in saturation when solving for any lower load current. The design is provided for all DoFs combinations at the same time as the LUTs are vectorized, leading to superior speed performance. The sizing of each device is achieved

based on its g_m/I_D, L, and I_D. For the diode-connected device M_{4a}, it has the same L as that of M_{4b}, while its width is a scaled version of M_{4b} depending on $Iref$. The design algorithm is detailed in Algorithm 1. The notation $\mathcal{L}(Y)\ (X)$ indicates the lookup value (Y) as a function of (X). Two special functions denoted as $\mathcal{L}_{DC}(Y)\ (X)$ and $\mathcal{L}_{FS}(Y)\ (X)$ are used to lookup the V_{GS} of a diode connected device and a floating source device (given the known drain and gate voltages), respectively.

Algorithm 1 Design mode algorithm

$R_2 = R_1/((V_{reg}/V_{ref}) - 1)$
$M_3(I_D) = I_L + V_{reg}/(R_1 + R_2)$
$M_3(V_{GS}) = \mathcal{L}(V_{GS})((g_m/I_D)_3, L_3, V_{DD} - V_{reg}, 0)$
$M_3(J_D) = \mathcal{L}(J_D)(M_3(V_{GS}), L_3, V_{DD} - V_{reg}, 0)$
$M_3(W) = M_3(I_D)/M_3(J_D)$
$M_{2a}(V_{GS}) = \mathcal{L}_{DC}(V_{GS})((g_m/I_D)_2, L_2, M_{2a}(V_{GS}), 0)$
$M_{2a}(J_D) = \mathcal{L}(J_D)(M_{2a}(V_{GS}), L_2, M_{2a}(V_{GS}), 0)$
$M_{2a}(W) = (I_Q/2)/M_{2a}(J_D)$
$M_{2b}(W) = M_{2a}(W)$
$M_{1b}(V_D) = V_{DD} - M_{2b}(V_{DS})$
$M_{1b}(V_{GS}) = \mathcal{L}_{FS}(V_{GS})((g_m/I_D)_1, L_1, V_{ref}, M_{1b}(V_D))$
$M_{1b}(J_D) = \mathcal{L}(J_D)(M_{1b}(V_{GS}), L_1, M_{1b}(V_{DS}), M_{1b}(V_{SB}))$
$M_{1b}(W) = (I_Q/2)/M_{1b}(J_D)$
$M_{1a}(W) = M_{1b}(W)$
$M_{4b}(V_{DS}) = V_{ref} - M_{1b}(V_{GS})$
$M_{4b}(V_{GS}) = \mathcal{L}(V_{GS})((g_m/I_D)_4, L_4, M_{4b}(V_{DS}), 0)$
$M_{4b}(J_D) = \mathcal{L}(J_D)(M_{4b}(V_{GS}), L_4, M_{4b}(V_{DS}), 0)$
$M_{4b}(W) = I_Q/M_{4b}(J_D)$

Note that for design, symmetry of the OTA is assumed. This is correct given the open loop operation. However, due to negative feedback, a slight mismatch occurs between the current in the two branches of the OTA. This requires a solving algorithm block to correct the DC bias point shift due to the current mismatch, as PSR is sensitive to such a bias point shift. The solving algorithm is shown in Algorithm 2. When solving the circuit across corners, Algorithm 2 is used in addition to accounting for M_3 bias point dependence on I_L.

Algorithm 2 Design mode algorithm

while $i < max_{itr}$ **do**
  while $j < max_{itr}$ **do**
    $M_{2b}(V_{GS}) = M_{2a}(V_{GS})$
    $M_{2b}(V_{DS}) = M_3(V_{GS})$
    $M_{2b}(J_D) = \mathcal{L}(J_D)(M_{2b}(V_{GS}), L_2, M_{2b}(V_{DS}), 0)$
    $M_{2b}(I_D) = M_{2b}(W) * M_{2b}(J_D)$
    $M_{1b}(J_D) = M_{2b}(I_D)/M_{1b}(W)$
    $M_{1b}(V_{GS}) = \mathcal{L}_{FS}(V_{GS})((M_{1b}(J_D), L_1, V_{ref}, M_{1b}(V_D))$
    $M_{2a}(I_D) = M_{4b}(I_D) - M_{2b}(I_D)$
    $M_{2a}(V_{GS}) = \mathcal{L}_{DC}(V_{GS})(M_{2a}(J_D), L_2, M_{2a}(V_{GS}), 0)$
    $M_{1a}(V_D) = V_{DD} - M_2(V_{GS})$
    $M_{1a}(V_s) = V_{ref} - M_{1b}(V_{GS})$
    $M_{1a}(V_{GS}) = \mathcal{L}_{FS}(V_{GS})((M_{1a}(J_D), L_1, M_{1a}(V_{DS}), M_{1a}(V_{SB}))$
  end while
  $M_{4b}(V_{DS}) = V_{ref} - M_{1b}(V_{GS})$
  $M_{4b}(J_D) = \mathcal{L}(J_D)(M_{4b}(V_{GS}), L_4, M_{4b}(V_{DS}), 0)$
  $M_{4b}(I_D) = M_{4b}(W) * M_{4b}(J_D)$
end while
$V_{reg} = V_{ref} - M_{1b}(V_{GS}) + M_{1a}(V_{GS})$

The algorithm may seem to be complex. However, it is practically divided into blocks to ensure code reuse for other LDO topologies. Furthermore, the process of generating the DC design and solving equations can be automated to be generated directly from the circuit netlist for greater efficiency.

3.5. Specifications Calculation

3.5.1. Dropout Voltage

The dropout voltage can be calculated directly from the LUT as the saturation voltage of the pass device. The saturation voltage can be defined as V_{DSAT} (as defined in the device model) or $V^* = 2/(g_m/I_D)$.

3.5.2. Loop Gain

The loop gain is calculated from the expression generated by the symbolic solver by substituting the small signal parameter values. Additionally, the loop gain unity gain frequency and the phase margin are calculated from the same expression.

3.5.3. Load Regulation

The AC load regulation is calculated from the symbolic solver expressions. The DC load regulation is calculated as the difference between the V_{reg} value at each load current corner divided by the change in the load current value. This will provide highly accurate results as the DC bias point is calculated accurately.

3.5.4. Power Supply Rejection (PSR)

For PSR calculation, direct substitution is performed in the symbolic solver transfer function at any required frequency. DC line regulation is calculated similarly to DC load regulation directly from the value of V_{reg} at each V_{DD} value. Nevertheless, evaluating transient line regulation is not as simple. The brute force method is to invoke the simulator, and then perform transient analysis at each design point in the database. This will give rise to an extremely large time overhead in the process. Building a custom transient engine is also inefficient and will require a long execution time, similar to a standard simulator.

The difficulty with calculating transients in analog design is that transients usually enforce non-linear behavior, which makes the analysis more difficult. Fortunately, the deviations induced in the small signal parameters due to the change of the bias point do not have much impact. This is due to the high linearity of the circuit at a given load current imposed by the negative feedback. The latter promotes the use of the PSR transfer function to calculate the line transient regulation. The time-varying pulse applied on the V_{DD} rail is not an ideal square wave; rather, it can be fairly approximated as a difference between two ramp functions $\frac{\triangle V_{DD}}{T}(r(t) - r(t-T))$, where T is the rise time of the input waveform.

The expected way to compute the line transient, since now we approximate the system by its linear small signal representation, would be to take the Laplace transform of the input wave signal and multiply it by the transfer function $PSR(s)$, and then take the inverse Laplace transform of one million design points of the DDB to obtain the time domain signal. However, the process of inverse Laplace transform in the case of our complex exact $PSR(s)$ transfer function obtained from the symbolic solver is a computational burden and will lead to extra time.

A simple quick method is devised to compute the line transient accurately. Using a simpler form of $PSR(s)$ in Equation (9), it can be rewritten as $PSR(s) \approx PSR_{DC}(1 + \frac{s}{\omega_{P1}})$ with fair accuracy, and the Laplace transform of the input signal is $\frac{\triangle V_{DD}}{T}(\frac{1-e^{-sT}}{s^2})$. Multiplying both functions and then applying inverse Laplace transform, the change in v_{reg} as a function of time will be

$$\triangle v_{reg}(t) = \triangle V_{DD} PSR_{DC}(\omega_r(r(t) - r(t-T)) + \frac{\omega_r}{\omega_{P1}}(u(t) - u(t-T))) \quad (13)$$

where ω_r is the inverse of the rise time T. The maximum amplitude of the output wave is seen to be $\triangle V_{DD} PSR_{DC}(\frac{\omega_r}{\omega_{P1}} + 1)$, which is $\triangle V_{DD}$ multiplied by $PSR(j\omega)$ evaluated at ω_r given that $\omega_r \gg \omega_{P1}$. Thus, we only need to evaluate $PSR(j\omega_r)$ to calculate line transient. Adding more terms from the PSR transfer function will not affect the maximum amplitude of the time domain signal. For example, adding the pole of $PSR(s)$ from Equation (9) in the previous derivation will contribute a term with magnitude $\triangle V_{DD} PSR_{DC}(\frac{\omega_r}{LG_{DC}\omega_{P1}})$, which is lower than the derived maximum amplitude by the LG_{DC}. The proposed method is extremely fast compared to the conventional method; even when trying to evaluate ω_{P1} itself from the transfer function, it also prevents invocation of the simulator in the loop. The accuracy is good, as will be shown in Section 4.

3.5.5. Output Noise

Total integrated output noise can be calculated by integrating the symbolic solver noise transfer function up to the desired frequency. Additional, thermal noise density can be evaluated at any required frequency.

3.5.6. Mismatch

The effect of random mismatch on *Vreg* is typically characterized by performing Monte Carlo simulations. This type of simulation is time consuming as the circuit has to be solved hundreds of times to obtain the output statistical distribution. We consider the mismatch effect according to the fast method described in [11], where the mismatch is considered to be a small perturbation imposed on the nominal bias point, facilitating the use of the linearized small-signal models of the devices. The transfer functions from each mismatch source to the output are then used to yield the statistical distribution. The effect of systematic mismatch due to feedback was already considered in DC Design/Solve in addition to the small signal netlist.

4. Results and Discussion

As mentioned, the design flow is agnostic to the technology and the topology used. To illustrate the flow, a 40 nm technology is used and a database is generated for the LDO in Figure 1. The LDO is designed to sink a current of 5 mA and the design will also be evaluated at corners. The Design corners for the database are shown in Table 2, where $C1$ denotes the corner at which I_L is minimum, $C2$ represents the corner with variations in the voltage generator output $Vref$, and variations in $Iref$, which is denoted by $IQ/IQ_{Nominal}$, and in $C3$, the LUT tables at SS and $T = 75$ are used, as they were used to design the LDO in [22]. Note that for $C2$, the change in $Vref$ is assumed to be 1% which is a large variation as the change in the voltage reference generator is in the order of a few ppm. Additionally, the change in $Iref$ is taken to be 10%. The DoFs are shown in Table 3. One million design points are generated in the database in 4.9 s. The computer used for the generation has a Core(TM) i7-8565U CPU and 8 GB RAM.

Table 2. Corners for the generated DDB.

Corners	Typical	C1	C2	C3	Units
MOSFET Corners	TT	TT	TT	SS	-
Temp	27	27	27	75	°C
V_{DD}	1.2	1.2	1.2	1.2	V
I_L	5	10^{-4}	5	5	mA
C_L	1	1	1	1	pF
V_{ref}	0.9	0.9	0.891	0.9	V
$IQ/IQ_{Nominal}$	1	1	1.1	1	V

Table 3. DoFs ranges for the generated DDB.

DoFs	Min	Max	Units
$M_1(L)$	0.5	6	µm
$M_2(L)$	0.5	6	µm
$M_3(L)$	40	40	nm
$M_4(L)$	0.5	6	µm
$M_1(g_m/I_D)$	10	30	S/A
$M_2(g_m/I_D)$	10	30	S/A
$M_3(g_m/I_D)$	5	15	S/A
$M_4(g_m/I_D)$	10	30	S/A
I_Q	0.1	10	µA
C_C	0.3	1	pF
R_1	5	500	kΩ
V_{reg}	1	1	V

4.1. Design Space Visualization

In this section, we use the generated database to explore trade-offs through design space visualization. The design points are plotted as a scatter plot and constraints can be applied to the design points to designate the subspace that fulfills the constraints. The x and the y axes can be any DOF or output specifications. The painted design space readily provides the designer with information about the feasibility limits of the topology under consideration and the available room for improvement. The DoFs can be tuned to move the design point interactively until it reaches the required specifications. Alternatively, the best design point for a given goal function can be extracted from the database and further optimization can be performed by using it as an initial seed.

Figure 3 demonstrates the design space of the database where the axes are the quiescent current of the OTA and the transient line regulation. The blue points are all the design points, while the orange points are those that obey the constraints of $LG_{DC} > 100$ and $PM > 60°$. The Pareto optimal front clearly shows the trade-off between the transient line regulation and the quiescent current. This is obvious from Equation (9); decreasing the current means a higher output resistance at the output of the OTA. This leads to a decreased value of the pole at this point, which happens to be zero in the high-frequency PSR. As a result, PSR degrades earlier, which causes the deterioration of the transient line regulation. In the figure, the tuned points are moved on the optimal front to minimize both the transient regulation and the current.

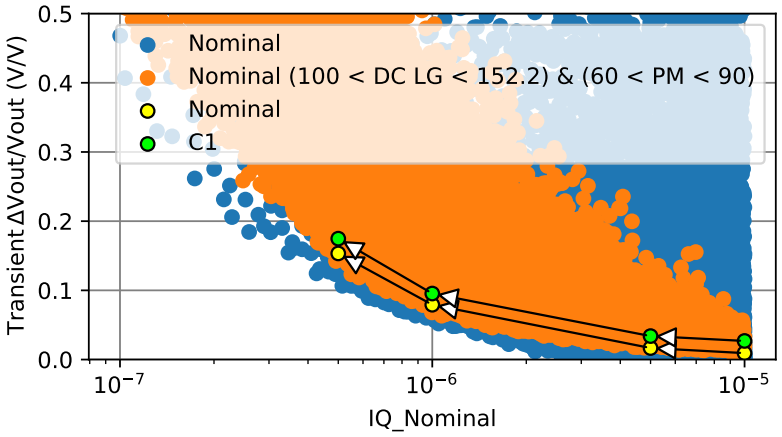


Figure 3. Transient line regulation vs I_Q design space for the maximum and minimum load current. The white arrows represent the movement of the chosen design point on the Pareto optimal front as different weights are assigned to each specification.

The trade-off between the DC *PSR* and area is demonstrated in Figure 4. In Equation (8), decreasing *PSR* requires decreasing the output conductances and increasing the transconductance of the pass device, which translates directly to an increase in area. To minimize both quantities, a point on the Pareto front should be chosen. The position of the point is determined by the weight given to each specification in the optimization process.

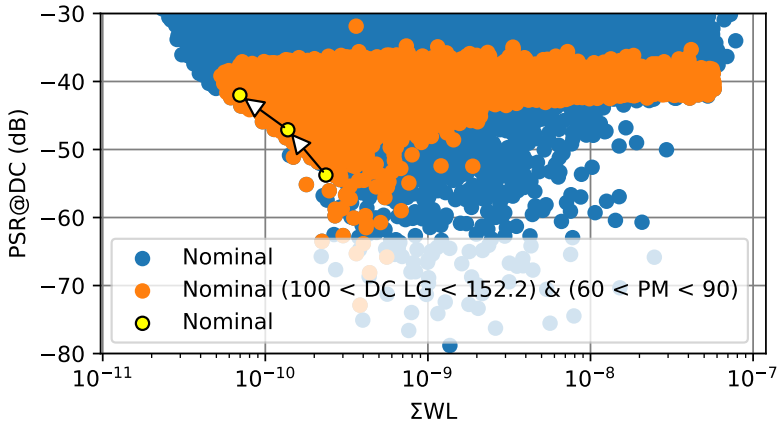


Figure 4. PSR@DC vs. Area design space for the maximum load current. The white arrows represent the movement of the chosen design point on the Pareto optimal front as different weights are assigned to each specification.

Another trade-off is explored in Figure 5 between the DC and high-frequency PSR. The trade-off can be explained by Equations (8) and (9). As mentioned before, decreasing the DC *PSR* requires decreasing the output conductances and increasing the transconductance of the pass device. Accordingly, the dominant node will have higher impedance and higher parasitics, thereby degrading *PSR* at high frequencies.

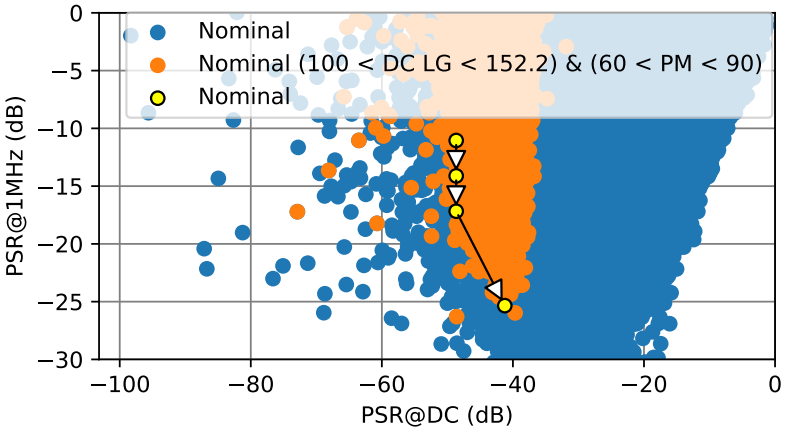


Figure 5. PSR@1MHz vs. PSR@DC design space for the maximum load current. The white arrows represent the movement of the chosen design point on the Pareto optimal front as different weights are assigned to each specification.

4.2. Design Examples

Two design examples are presented using 40 nm technology with the previously generated database. The design point should satisfy certain constraints while optimizing two specifications simultaneously. Equal weights are given to the two specifications in the optimization process. The sizing parameters will be shown and the synthesis results will be compared to the simulation results.

4.2.1. First Design Example

The first design example should satisfy the specifications shown in Table 4. The sizing parameters are shown in Table 5. Table 6 compares the synthesis results to the simulation results. Note that for transient line regulation, the *PSR* test signal is a square wave with a 200 mV peak to peak and 500 ns rise time. Additionally, the load regulation is the same for the two corners (Nominal and *C*1) as it is an across-corner specification. I_{Qtot} is the total current consumed in the OTA and the resistive divider. The synthesis shows excellent agreement with the simulation. The error in transient line regulation is expected as we used an AC quantity to approximate it. Nevertheless, the accuracy is good. In addition, Figure 6 shows the *PSR* vs. frequency of the tuned point for the first two corners and *LG* is shown in Figure 7. The curves of synthesis and simulation are almost identical for the whole frequency range, validating the accuracy of the proposed flow.

Table 4. Design requirements for the first design example.

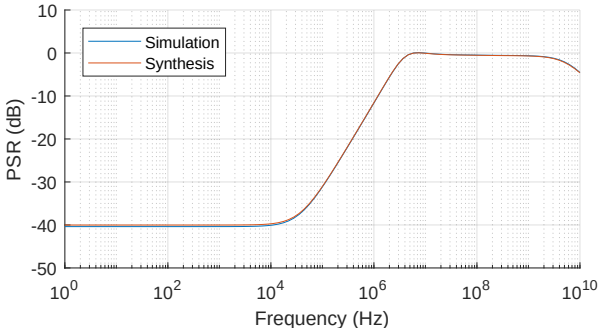
Specification	Condition
LG_{DC}	>100
PM	>60°
$Transient\ \frac{\triangle V_{reg}}{V_{reg}}$	Minimize
I_{Qtot}	Minimize

Table 5. Sizing parameters for the first design example.

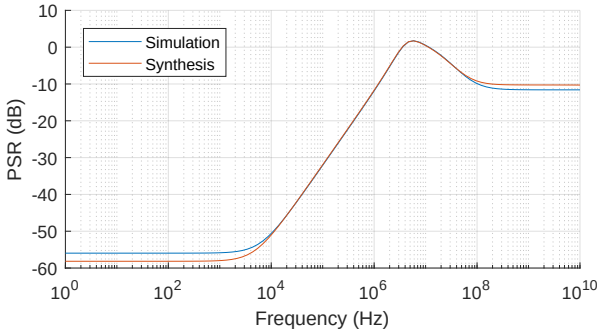
Parameter	Value	Unit
$M_1(L)$	3.1	µm
$M_2(L)$	5.7	µm
$M_3(L)$	40	nm
$M_4(L)$	5.4	µm
$M_1(W)$	8.8	µm
$M_2(W)$	4	µm
$M_3(W)$	996.4	µm
$M_4(W)$	2	µm
I_{Qtot}	10.1	µA
R_1	12.3	kΩ
R_2	110.5	kΩ
C_C	520.3	fF

Table 6. Comparison of the synthesis and simulation results for the first design example.

	Nominal		C1		C2		C3	
Spec.	**Synth.**	**Sym.**	**Synth.**	**Sim.**	**Synth.**	**Sim.**	**Synth.**	**Sim.**
PSR@DC (dB)	−40.02	−40.4	−58.16	−56.01	−41.91	−42.27	−39.07	−39.25
PSR@1 MHz (dB)	−11.55	−11.65	−11.7	−11.89	−12.28	−12.38	−10.87	−10.86
LG_{DC}	104.6	105.4	113.5	114.9	111.7	112.5	100.1	102.5
PM (°)	74.31	74.06	61.11	60.9	73.9	73.64	74.7	74.48
$Transient\ \frac{\triangle V_{reg}}{V_{reg}}$ (mV/V)	33.66	43.95	32.27	37.68	31.18	38.9	36.45	49.65
I_{Qtot} (µA)	10.06	10.24	10.22	10.23	10.25	10.26	10.06	10.07
Dropout voltage (mV)	144.4	144.4	84.52	84.53	144.1	143.9	152.2	151.5
V_{reg} (V)	0.999	1	1.01	1.01	0.989	0.99	0.999	1
Load Regulation (mV/mA)	2.24	2.18	2.24	2.18	2.13	2.15	2	2.1
Output Integ. Noise (µVrms)	130	122.3	146.4	136.6	130.6	123	141.9	135.3

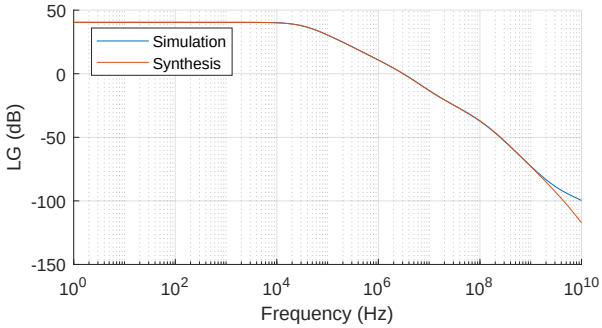


(**a**)

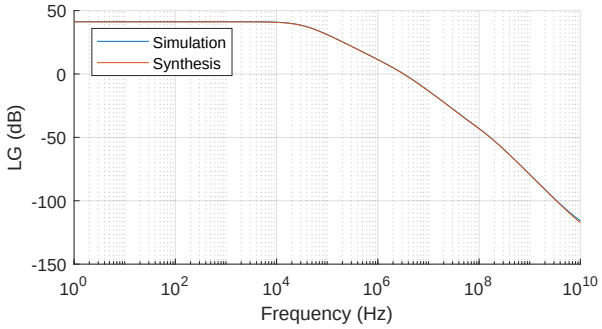


(**b**)

Figure 6. PSR vs. Frequency. (**a**) Nominal. (**b**) C1.



(**a**)



(**b**)

Figure 7. LG vs. Frequency. (**a**) Nominal. (**b**) C1.

The random mismatch effect was calculated using the noise analysis transfer functions. Monte Carlo simulations were performed with Cadence Spectre using 200 runs. In Figure 8, the histogram is plotted from the simulation data, and the fit is achieved using the estimated mean and standard deviation from these data. The synthesis plot is constructed using

the calculated mean and standard deviation from the mentioned procedure. Both the simulation and the synthesis results are close to each other.

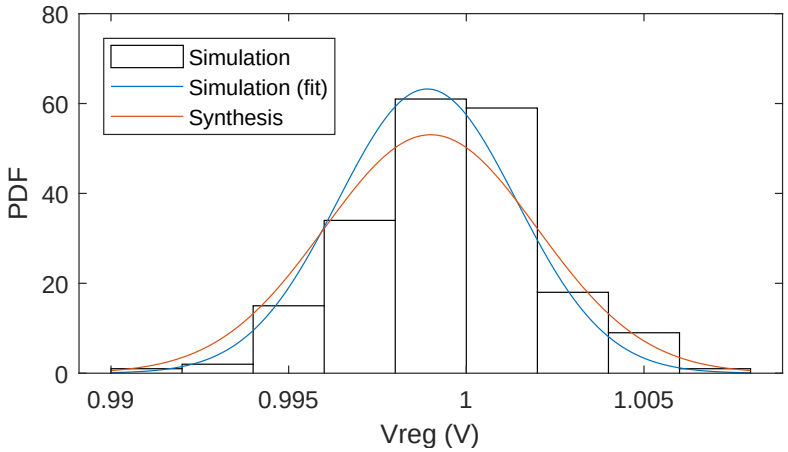


Figure 8. Probability density function (PDF) of *Vreg* due to random mismatch.

4.2.2. Second Design Example

The second design example should satisfy the specifications shown in Table 7. The sizing parameters are shown in Table 8. The constraints are the same for this design example; however, the objectives are different. The chosen point does not quite reside on the Pareto optimal front because the sacrifice of 2 dB from the DC *PSR* decreases the width of the pass device by a large factor. Table 9 compares the synthesis results to the simulation results, and it can be seen that both are very close to each other.

Table 7. Design requirements for the second design example.

Specification	Condition
LG_{DC}	>100
PM	>60°
$PSR@DC$	*Minimize*
$PSR@1\ MHz$	*Minimize*

Table 8. Sizing parameters for the second design example.

Parameter	Value	Unit
$M_1(L)$	1.5	µm
$M_2(L)$	3.8	µm
$M_3(L)$	40	nm
$M_4(L)$	5.9	µm
$M_1(W)$	11.1	µm
$M_2(W)$	7.2	µm
$M_3(W)$	1142	µm
$M_4(W)$	20	µm
I_{Qtot}	23.3	µA
R_1	5.8	kΩ
R_2	52.3	kΩ
C_C	748.5	fF

Table 9. Comparison between the synthesis and simulation results for the second design example.

	Nominal		C1		C2		C3	
Spec.	**Synth.**	**Sym.**	**Synth.**	**Sim.**	**Synth.**	**Sim.**	**Synth.**	**Sim.**
PSR@DC (dB)	−43.01	−42.8	−57.97	−57.17	−44.37	−44.02	−44.26	−44.14
PSR@1 MHz (dB)	−18.19	−18.17	−18.4	−18.38	−18.87	−18.88	−17.5	−17.48
LG_{DC}	105.1	103.3	115.6	114.8	109.6	107.4	105.8	104.1
PM (°)	75.69	75.66	60.79	61.06	75.36	75.31	76.03	75.99
Transient $\frac{\triangle V_{reg}}{V_{reg}}$ (mV/V)	15.91	20.07	15.24	18.84	14.83	17.7	17.14	22.56
I_{Qtot} (µA)	23.26	23.31	23.44	23.62	24	24.2	23.5	23.2
Dropout voltage (mV)	139.8	139.8	85.55	85.49	140	139.3	146.8	146.7
V_{reg} (V)	0.999	1	1.01	1.009	0.99	0.989	1	1.001
Load Regulation (mV/mA)	2.23	2.19	2.23	2.19	2.2	2.18	2.31	2.23
Output Integ. Noise (µVrms)	120	111.7	136.7	126.5	120.6	112.4	130.5	123.4

4.2.3. Flow Performance Summary

In general, the efficacy and strength of the flow against other approaches and standard optimization engines embedded in cad tools can be summarized as follows:

- Design space visualization: The proposed flow can solve hundreds of thousands of design points for a given LDO topology to visualize the complete design space (not possible with SPICE-in-the-loop even for DC/AC sim) and understand the trade-offs.
- Speed and accuracy: The flow is extremely fast. One million design points are generated in 4.9 s, which is an average of 4.9 micro seconds per design point. Using the simulator, the AC, DC and transient simulations for a single design point spanned 5.06 s on the same machine used to generate the database. In addition, the results are accurate when compared to the simulator and almost all the specifications of LDOs are included.
- Feasibility: SPICE-in-the-loop optimization does not provide any information about whether the used LDO specifications are feasible or not. The presented procedure indicates the topology limits, i.e.,: what the maximum PSR achievable is, what is the minimum line transient regulation, etc.
- Applicability: The flow can be easily applied to any LDO topology with as few steps as possible, as opposed to other approaches which require a large setup overhead to account for new topologies.

Table 10 presents a qualitative comparison between the proposed flow and other reported procedures.

Table 10. A qualitative comparison to other flows.

	This Work	**[16]**	**[12]**	**[15]**
Design Space Visualization	Yes	No	No	No
Speed	Fast	Slow	Fast	Slow
Feasibility	Yes	No	No	No
Applicability overhead	Minor	Minor	Major	Minor

5. Conclusions

This paper presented a general flow for the design automation of LDOs. LUTs were used to sustain accuracy without the need to invoke the simulator in the loop. A symbolic solver was used to preserve the expression accuracy and account for different parasitics. The g_m/I_D methodology was used for the design to facilitate orthogonal exploration of the trade-offs. A fast technique was introduced to calculate the line transient regulation without the need to call the simulator. A database with one million design points was generated in

4.9 s on a computer with standard capabilities that facilitated design space visualization and tuning across corners. Design examples were provided using a 40 nm technology, and the synthesis results showed excellent agreement with the simulator results.

Author Contributions: Conceptualization, K.M. and H.O.; methodology, K.M. and H.O.; software, K.M. and H.O.; validation, K.M.; formal analysis, K.M.; investigation, K.M.; resources, K.M. and H.O.; data curation, K.M.; writing—original draft preparation, K.M.; writing—review and editing, K.M. and H.O.; visualization, K.M. and S.N.; supervision, H.O. and S.N.; project administration, H.O.; funding acquisition, H.O. All authors have read and agreed to the published version of the manuscript.

Funding: This research was funded by Egypt's Information Technology Industry Development Agency (ITIDA) grant number ARP2021.R30.4.

Acknowledgments: The authors would like to thank the Analog Designer's Toolbox (ADT) team at Master Micro LLC for supporting this work.

Conflicts of Interest: The authors declare no conflict of interest.

References

1. Middlebrook, R.; Vorperian, V.; Lindal, J. The N Extra Element Theorem. *IEEE Trans. Circuits Syst. I Fundam. Theory Appl.* **1998**, *45*, 919–935. [CrossRef]
2. Hajimiri, A. Generalized Time- and Transfer-Constant Circuit Analysis. *IEEE Trans. Circuits Syst. I Regul. Pap.* **2010**, *57*, 1105–1121. [CrossRef]
3. Johns, D.A.; Martin, K. *Analog Integrated Circuit Design*; John Wiley & Sons: Hoboken, NJ, USA, 2008.
4. Silveira, F.; Flandre, D.; Jespers, P.G. A gm/ID based methodology for the design of CMOS analog circuits and its application to the synthesis of a silicon-on-insulator micropower OTA. *IEEE J. Solid-State Circuits* **1996**, *31*, 1314–1319. [CrossRef]
5. Jespers, P. *The gm/ID Methodology, a Sizing Tool for Low-Voltage Analog CMOS Circuits: The Semi-Empirical and Compact Model Approaches*; Springer Science & Business Media: New York, NY, USA, 2010.
6. Aminzadeh, H. Systematic circuit design and analysis using generalised gm/ID functions of MOS devices. *IET Circuits Devices Syst.* **2020**, *14*, 432–443. [CrossRef]
7. Tlelo-Cuautle, E.; Sanabria-Borbon, A. Optimising operational amplifiers by evolutionary algorithms and gm/Id method. *Int. J. Electron.* **2016**, *103*, 1665–1684. [CrossRef]
8. Jespers, P.G.; Murmann, B. *Systematic Design of Analog CMOS Circuits*; Cambridge University Press: Cambridge, UK, 2017.
9. Sabry, M.N.; Omran, H.; Dessouky, M. Systematic design and optimization of operational transconductance amplifier using gm/ID design methodology. *Microelectron. J.* **2018**, *75*, 87–96. [CrossRef]
10. Elmeligy, K.; Omran, H. Fast Design Space Exploration and Multi-Objective Optimization of Wide-Band Noise-Canceling LNAs. *Electronics* **2022**, *11*, 816. [CrossRef]
11. Omran, H.; Amer, M.H.; Mansour, A.M. Systematic Design of Bandgap Voltage Reference Using Precomputed Lookup Tables. *IEEE Access* **2019**, *7*, 100131–100142. [CrossRef]
12. Soto-Aguilar, S.; Sanabria-Borbón, A.; Sánchez-Sinencio, E. Surrogate-based Optimization-aided Design for Low Power Analog Circuits. In Proceedings of the 2018 IEEE 61st International Midwest Symposium on Circuits and Systems (MWSCAS), Windsor, ON, Canada, 5–8 August 2018; pp. 566–569.
13. Chen, Y.L.; Chu, G.M.; Lien, Y.C.; Lee, C.M.; Liu, C.N.J. Simultaneous optimization for low dropout regulator and its error amplifier with process variation. In Proceedings of the Technical Papers of 2014 International Symposium on VLSI Design, Automation and Test, Hsinchu, Taiwan, 28–30 April 2014; pp. 1–4. [CrossRef]
14. DasGupta, S.; Mandal, P. An automated design approach for CMOS LDO regulators. In Proceedings of the 2009 Asia and South Pacific Design Automation Conference, Yokohama, Japan, 19–22 January 2009; pp. 510–515. [CrossRef]
15. López-Arredondo, J.; Tlelo-Cuautle, E.; Fernández, F.V. Optimization of LDO voltage regulators by NSGA-II. In Proceedings of the 2016 13th International Conference on Synthesis, Modeling, Analysis and Simulation Methods and Applications to Circuit Design (SMACD), Lisbon, Portugal, 27–30 June 2016; pp. 1–4.
16. Martins, I.; Olivera, F.; Petraglia, A. A Computer-Aided Approach for Low-Power LDO Regulator Design. 2021. Available online: https://www.researchgate.net/publication/351308616_A_Computer-Aided_Approach_for_Low-Power_LDO_Regulator_Design (accessed on 10 November 2022).
17. Rincón-Mora, G.A. *Analog IC Design with Low-Dropout Regulators (LDOs)*; McGraw-Hill Education: Berkshire, UK, 2009.
18. Razavi, B. The Low Dropout Regulator [A Circuit for All Seasons]. *IEEE Solid-State Circuits Mag.* **2019**, *11*, 8–13. [CrossRef]
19. Torres, J.; El-Nozahi, M.; Amer, A.; Gopalraju, S.; Abdullah, R.; Entesari, K.; Sanchez-Sinencio, E. Low Drop-Out Voltage Regulators: Capacitor-less Architecture Comparison. *IEEE Circuits Syst. Mag.* **2014**, *14*, 6–26. [CrossRef]
20. Youssef, A.A.; Murmann, B.; Omran, H. Analog IC design using precomputed lookup tables: Challenges and solutions. *IEEE Access* **2020**, *8*, 134640–134652. [CrossRef]

21. Tian, M.; Visvanathan, V.; Hantgan, J.; Kundert, K. Striving for small-signal stability. *IEEE Circuits Devices Mag.* **2001**, *17*, 31–41. [CrossRef]
22. Razavi, B. The Design of An LDO Regulator [The Analog Mind]. *IEEE Solid-State Circuits Mag.* **2022**, *14*, 7–17. [CrossRef]