



# Article Novel Radiation-Hardened High-Speed DFF Design Based on Redundant Filter and Typical Application Analysis

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**Abstract:** A cell-level radiation hardening by design (RHBD) method based on commercial processes of single event transient (SET) and single event upset (SEU) is proposed in this paper, in which new radiation-hardened D-type flip-flops (DFFs) are designed. An application-specific integrated circuit (ASIC) of a million gates level is developed based on DFFs, and SEU and single event functional interruption (SEFI) heavy-ion radiation tests are carried out. The experimental results show that the new DFF SEU ability is increased by 63 times compared with the DICE-designed DFF, and is three orders of magnitude higher than the redundantly designed DFF. The SEFI ability of the ASIC designed by the new DFF is 2.6 times higher than the circuit hardened by the TMR design.

Keywords: D-type flip-flop; single event transient; single event upset; radiation hardened



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## 1. Introduction

Heavy ions and high energy protons in space can produce single event effects (SEE) on semiconductor devices, while single event soft errors in digital integrated circuits have become the main cause of failure of space vehicles. First, SEU is more sensitive in a small size process, which makes the multi node upset (MNU) occur more easily in the adjacent device due to the charge sharing [1]. Second, with the increasing working frequency of the circuit, SET is more likely to be captured by sequential units and be converted to SEU [2]. Third, the single continuous error (SCU) is easier to generate due to the clock tree affected by SET as the circuit scale increases [3], which will lead to the probability of single event soft errors being greatly increased in digital integrated circuits.

The RHBD method based on the commercial process has the advantages of not needing to modify the process parameters, having a low cost of tape-out, and having a good hardened performance, and has been widely used in the development of aerospace integrated circuits. The guard ring structures method is commonly used in the layout level of anti-SET [4]. The single event charge sharing can be suppressed by inserting minority carrier guard rings between the adjacent drains. The cell-level anti-SET and anti-SEU methods of DFF include triple modular redundancy (TMR) [5], C cell [6], dual interlocked cell (DICE) [7], and error correction code (ECC) [8], which improve the anti-SEE performance at the expense of area or time.

To improve the anti-SEU capability of DFF, considering SETs from buffers or logic gates inside the cell may cause DFF errors. A new DFF IP cell that is resistant to SET, SEU, and MNU, is designed by optimizing the filter of the DFF input to reduce the influence of SET [1,3]. In addition, two types of DFFs with different reinforcement levels are used for the circuit design, which can save layout area overhead and ensure a high SEU resistance by rationally screening and replacing DFFs on non-critical paths. Finally, the design, tape-out, and radiation tests of the verification circuit ASIC based on the 0.18  $\mu$ m commercial standard CMOS process are completed through the above methods.

# 2. DFF Design

A novel DFF structure based on redundant delay filter (RDF) and dual DICE is designed, as shown in Figure 1 [3], and is called RDD-DFF. DICE is used to improve the SEU threshold, while RDF is used to filter out the external SET. The two outputs in our design are independent, so the SET generated by a single output will not affect the dual-mode redundant DICE latch. In this way, the source of the SET can be eliminated maximally.



Figure 1. The RDD-DFF structure.

## 2.1. SET Simulation

The SET simulations were performed on Sentaurus TCAD, applying a Fermi–Dirac statistics and hydrodynamic model, taking into account the effects of doping, electric field, carrier–carrier scattering, and interface scattering on mobility, as well as the effect of band-gap narrowing, while the temperature was set at 25 °C. The simulation results of Bi–923.2MeV and Cl–158MeV are shown in Figure 2a,b, while the arrow direction is the vertical 90–degree incident direction of the heavy ions. The SET horizontal track widths under irradiation can be obtained at about 1  $\mu$ m. The electrostatic potential distribution is shown in Figure 2c. The SET sensitive area generated by the heavy ions is mainly on the drain region of the device in the off state. At this time, the drain PN junction is at a reverse bias, and a depletion region is formed, which is the main region for collecting charges. The holes induced by radiation are collected at the drain, resulting in the potential of the drain increasing.



**Figure 2.** The TCAD simulation results of SET: (**a**) Bi-923.2MeV; (**b**) Cl-158MeV; (**c**) electrostatic potential distribution.

Charge sharing comes from diffusion effects in NMOS, which is the main course of SET on the double-well process, while for PMOS, charge sharing mainly comes from the bipolar amplification. The guard rings and contact holes are designed to speed up the collection of interfering charges to reduce the SET pulse width. In addition, it is also necessary to strengthen the charge sharing of transistors with different polarities. With the guidance of the SET width obtained by simulation, the isolation of the sensitive node pairs is realized by introducing another complementary well between the same phase nodes. The distances between the same phase nodes are designed to be greater than 2  $\mu$ m, as shown in Figure 3. In this way, the charge between the same polarity transistors can be eliminated, and the charge deposited on the sensitive nodes is reduced.



the charge sharing of transistors with different polarities

the sensitive node pairs are isolated by wells

Figure 3. The hardened layout using charge sharing.

The RDF structure is designed as shown in Figure 4 [3]. The filtering delay threshold is set to be adjustable. The appropriate filtering threshold can be set according to the SET circuit test results, while a corresponding time overhead is required.



Figure 4. RDF structure.

### 2.3. Anti-SEU Design

The SEU-sensitive node pairs in the DICE memory cell are shown in Figure 5. The state of node A is flipped from 1 to 0 when the heavy ion is irradiated on the reverse-biased NMOS drain region (n1), so that NMOS-M7 is turned off and PMOS-M4 is turned on, which makes the state of node B flip from 0 to 1. Then, PMOS-M6 will turn off while nodes C and D are both in a floating state. The DICE cell will finally flip if both nodes are simultaneously

affected by the charge sharing effect or oblique angle injection. Therefore, all sensitive node pairs should be properly laid out during the layout design stage.



Figure 5. The sensitive node analysis of the DICE cell.

The team has proposed an error quenching double DICE (EQDD) method using the layout crossing of two DICE cells to improve the SEU ability of DICE [1], through which the SEU LET threshold could effectively be improved. The charge sharing between the non-sensitive nodes in one DICE cell can be used to reduce the SET error through a quenching effect, while the distance between the sensitive nodes within adjacent DICEs can be set to more than 6  $\mu$ m. In this way, the sensitive node pairs can be separated without losing the area cost through the layout crossing design of two DICE cells, as shown in Figure 6.



Figure 6. Layout of the EQDD method.

#### 2.4. Selective SEU Design

The RDD-DFF design needs an extra delay and area, although it has both a better SEU and SET performance. At the VLSI level, DFFs can be chosen at different anti-SEE levels according to the timing constraints. The DFF on the non-critical path can be replaced with RDD-DFF to improve the SEE capability under the premise that the overall circuit delay will not be increased after replacement.

All path delay values can be comprehensively enumerated with the help of the DC tool to import the circuit netlist, through which the critical path can be formed by counting the maximum path delay. The improvement of the circuit SEE can be obtained at the cost of a minimal area overhead, with the help of a program written in C# (as shown in Figure 7) to identify alternative DFFs.

```
//Circuit_DC: Circuit Delay Information File
//DFF_Compilations[]: DFF array of Name&Delay&ProTime
Wihle(!Circuit_DC.EndOfStream)
{
    If (Circuit_DC.ReadLine().Contain( " DFF " ))
    DFF_Compilations.add(DFF_Name, DFF_Delay,DFF_ProTime);
    }
DFF_Max_Delay=MAX(DFF_Compilations.Delay);
For (i=0;i<DFF_Compilations.Size();i++)
    {
        Deta_t=RDD_DFF.ProTime-DFF_Compilations[i].ProTime;
        if (DFF_Max_Delay>(DFF_Compilations[i].delay+Deta_t))
        Replace(DFF_Compilations[i].name,RDD_DFF);
    }
```

Figure 7. The algorithm to identify alternative DFFs.

## 3. Radiation Tests

An ARINC 659 bus protocol control circuit (ASIC) is designed using the RDD-DFF cell with the above-mentioned RHBD methods at 0.18  $\mu$ m through the CMOS process. The circuit scale is about 1.65 million gates with 26,725 DFFs, which has the highest operating frequency at 144 MHz. The appearance of the chip is shown in Figure 8.



Figure 8. The chip appearance.

An SEU test system based on a scan chain is developed to verify the RDD-DFF SEE performance. The test clock frequency is set at 1 MHz and the internal DFFs are in the dynamic mode so as to read back the "01" code stream. A typical functional SEFI test system is also developed to evaluate the SEU performance of the circuit. FPGA is used to input the same excitation vector to both the device being tested and the comparison device, while the operating frequency is set at 144 MHz. The output results of the device being tested and the comparison device are collected separately by FPGA, while the real-time comparison result is used to determine whether a single event function interruption or error occurred. The SEE experiments are carried out on the HIRFL cyclotron accelerator in Lanzhou and the HI-13 tandem accelerator in Beijing, respectively. The heavy ions are shown in Table 1. The test site picture is shown in Figure 9.

Table 1. The heavy ion parameters.

Ion	Energy (MeV)	LET (MeV × cm²/mg)	Range (µm)	Accelerator
Cl	158	13.1	51.1	
Ti	169	21.8	37.9	HI-13
Ge	205	37.3	30	
Bi	923.2	99.8	53.7	HIRFL



Figure 9. SEE test on HIRFL.

## 4. Results and Discussion

The SEU results of RDD-DFF obtained based on the SCAN method are shown with the red line in Figure 10, while the SEU results of the DICE-DFF that did not use the EQDD method before are shown with the blue line for comparison. The other results of the 0.18  $\mu$ m CMOS DFF (DFF-R) designed using the RHBD method of two redundant storage node topologies proposed in [9] are shown with the black line. The SEU saturated cross-section is obtained by fitting and drawing the Weibull curve, while the SEU LET threshold value can be taken as corresponding to 10% of the saturated cross-section. The SEU on-orbit error rates normalized to each bit is shown in Table 2, which are obtained using the RPP model in the radiation environment of the Adams 90% maximum bad case and the 3-mm equivalent Al shielding.



Figure 10. The SEU Weibull curve.

Table 2. The heavy ion parameters.

Types	Saturation Cross Section (cm <sup>2</sup> /bit)	LET Threshold (10%) (MeV $\times$ cm <sup>2</sup> /mg)	SEU On-Orbit Error Rate (/bit/day)
RDD-DFF	$7.48 imes10^{-10}$	28.4	$5.50 imes10^{-10}$
DICE-DFF	$2.05  imes 10^{-8}$	35.0	$3.51  imes 10^{-8}$
DFF-R	$7.90 imes10^{-8}$	3.1	$3.87 imes10^{-6}$

The results show that the SEU of RDD-DFF is similar to the DFF using ordinary DICE under the condition of small LET ions, which can be due to the small LET ions having a small charge sharing radius, which is difficult to occur through SEU in DICE. Thereof, the probability of SEU occurrence in DICE using EQDD is equivalent to the traditional DICE, while the SEU of DFF is mainly derived from the SET occurring in RDF and CLK. However, the SEU cross-section is reduced by about 27 times under large LET ions by using the EQDD method, which means it is more effective against SEU than the traditional DICE. The SEU error rate of RDD-DFF is 63 times better than DICE-DFF and four orders of magnitude better than DFF-R, which indicates that DICE plays an important role in SEU, as well as RDF in SET.

To compare the SEFI performance, the SEFI Weibull curves of the designed ASIC, the DSP circuit SMV320C6701 at 0.18  $\mu$ m process in [10], and the DSP circuit RTAX4000D at 0.15  $\mu$ m process in [11] are drawn in Figure 11, while the SEFI index is calculated as shown in Table 3.



Figure 11. The SEFI Weibull curve.

Table 3	. The	heavy	ion	parameters.
				1

Types	Frequency	Saturation Cross Section (cm <sup>2</sup> /bit)	LET Threshold (10%) (MeV × cm <sup>2</sup> /mg)	SEFI On-Orbit Error Rate (/bit/day)
ASIC RTAX4000D SMV320C6701	144 MHz 120 MHz 140 MHz	$1.7  imes 10^{-6}$ $5.4  imes 10^{-6}$ $4.8  imes 10^{-4}$	27.2 34.0 9.4	$8.12 \times 10^{-7}$ $2.11 \times 10^{-6}$ $3.57 \times 10^{-3}$
5101 0 52000701	140 IVII IZ	4.8 × 10	2.4	$3.37 \times 10$

As the key status and data registers in complex circuits such as ASIC and DSP are generally DFF cells, they are likely to cause a disorder of the state machine of DUT and lead to SEFI, while SEU occurs on these registers. The SEFI probability of ASIC is 2.6 times smaller than that of RTAX4000D due to the better SEU performance of DICE-DFF. The R-cell in RTAX4000D is a TMR design, which has a better resistance to SEU, while the filter is used to improve the SET performance. In contrast, the ASIC in this paper adopt hardened-design of DFF cells instead of TMR strategy, which can effectively reduce the layout area, power consumption, and the operating fre-quency performance.

The SEFI probability of ASIC is three orders of magnitude smaller than SMV320C6701, while the SEU results of the cache, memory, and other storage cells in SMV320C6701 show that no effective SEU hardening design is carried out at a cell level. In contrast,

ASIC does not reduce the operating frequency, which is the same advantage as using the RHBD method.

#### 5. Conclusions

In the field of aerospace, more attention has been paid to the cost of chips, which makes obtaining reliable radiation resistance and a high performance with the smallest area cost an eternal topic. In this paper, the SEU performance is improved 63 times through designing a new hardening circuit structure and layout innovation, as well as through using selective optimization methods of DFF. The traditional cell-level hardening design of DFF is improved, while maintaining no additional increase in area. The SEFI performance of ASIC hardening by the cell is better than using the TMR method by about 2.6 times, which indicates that cell-level hardening design is one of the most cost-effective ways to design aerospace integrated circuits.

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