



Article Modular Battery Emulator for Development and Functional Testing of Battery Management Systems: The Cell Emulator

Roberto Di Rienzo *^D, Alessandro Verani ^D, Federico Baronti ^D, Roberto Roncella ^D and Roberto Saletti^D

Dipartimento Ingegneria dell'Informazione, University of Pisa, Via Caruso 16, 56122 Pisa, Italy; alessandro.verani@phd.unipi.it (A.V.); federico.baronti@unipi.it (F.B.); roberto.roncella@unipi.it (R.R.); roberto.saletti@unipi.it (R.S.)

* Correspondence: roberto.dirienzo@unipi.it

Abstract: Battery Management Systems are fundamental components of the present battery generation. The development and characterization phases of a BMS often require an emulator of the battery cells with which the Battery Management System functions can be assessed with no safety risks as it would instead happen using a real battery. This work describes the design and characterization of a modular cell emulator circuit to be used as platform for the Hardware-in-the-loop test of a Battery Management System. The design constraints and choices are first described. Then, the experimental characterization of the cell emulator is shown and discussed. The proposed circuit shows a voltage resolution of 76 μ V, an accuracy of 2.17 mV, and a setting time of 340 μ s. Its cost is around 40 USD. The circuit results to be a very good trade-off between performance and cost. The Project is available to the scientific community as open hardware platform freely downloadable. It could be useful to small-size laboratories to self-produce a low-cost battery emulator with good performance for the development and the functional test of custom Battery Management Systems.

Keywords: Battery Management System; battery cell emulator; hardware in the loop; open hardware platform; BMS characterization

1. Introduction

The phases in which the Battery Management System (BMS) control algorithms are assessed and the BMS functional test is carried out are ones of the most complex and time-consuming phases in the development of a BMS for the design of present and new generation batteries. The BMS and its companion battery are connected together to perform the tests, with obvious concerns about the safety of the operations, should BMS failures show up during the tests. The hardware-in-the-loop (HIL) approach simplifies and improves safety in these phases, because it replaces the real battery with a twin that reproduces the behavior of the battery cells in safe and controllable way [1]. In particular, the HIL platform consists of a system that provides the inputs to the BMS under development and acquires its outputs like a real battery was connected to it. Usually, HIL platforms are divided in two categories: communication HIL platforms and power HIL platforms [2]. The general architecture of the two HIL approaches are shown in Figure 1.

The battery cells are completely simulated in the first category, and the inputs to the BMS are provided by means of a communication interface that reproduces the output of the analog to digital front-end of the BMS as shown in Figure 1a. This approach is suitable for the development and verification of the BMS control and state estimation algorithms. However, it is not appropriate to check all the functionalities of the BMS because the BMS analog front-end is not included in the loop. As an example, the authors in [3] proposed a communication HIL platform able to develop and verify the State of Charge (SOC) and parameters identification algorithms of a BMS for electric vehicle batteries, that was implemented on a Field Programmable Gate Array (FPGA). The proposed HIL platform



Citation: Di Rienzo, R.; Verani, A.; Baronti, F.; Roncella, R.; Saletti, R. Modular Battery Emulator for Development and Functional Testing of Battery Management Systems: The Cell Emulator. *Electronics* **2022**, *11*, 1215. https://doi.org/10.3390/ electronics11081215

Academic Editors: Antonio J. Marques Cardoso and Khaled Laadjal

Received: 7 March 2022 Accepted: 8 April 2022 Published: 12 April 2022

Publisher's Note: MDPI stays neutral with regard to jurisdictional claims in published maps and institutional affiliations.



Copyright: © 2022 by the authors. Licensee MDPI, Basel, Switzerland. This article is an open access article distributed under the terms and conditions of the Creative Commons Attribution (CC BY) license (https:// creativecommons.org/licenses/by/ 4.0/). provides to the FPGA-based BMS the simulated voltage, current and temperature of the cells that compose a vehicle battery by means of a communication interface. The same interface is used to acquire the BMS computed outputs to verify the algorithm implementation and validate the BMS behavior.



Figure 1. Block diagram of a general Hardware-In-the-Loop architecture based on Communication (**a**) and Power (**b**) approaches.

Instead, the power HIL platforms provide with an emulator circuit all the input signals to the BMS, such as voltage, current and temperature of the cells as shown in Figure 1b. Unfortunately, the complete emulation of the cell behavior is difficult and expensive because it requires the management of high power levels. However, the availability of the maximum power of a battery cell is only needed to verify particular BMS functionalities, such as the interruption of the charge and discharge phases in case of events where the maximum allowable current level is exceeded. Indeed, most of the BMS functionalities can be developed and verified using a low-power emulator of the cells. Checking the functionality of the measuring systems, verifying the balancing circuit and its equalization algorithm, controlling the accuracy of the State of Charge estimation algorithm, and validating the basic safety functionalities are tasks easily carried out with a low-power emulator of the battery cells. Therefore, the power HIL platforms are very useful in the BMS development and test. This work presents the design of a modular emulator of a battery cell that is able to reproduce the voltage, current and temperature signals of a battery cell. The emulator may be series-connected to obtain a "virtual battery" useful to develop and test new BMSs.

Several battery emulators have been presented in the literature. For example, Refs. [4–11] report possible solutions that only emulate the cell voltage or the cell voltage and temperature at most. However, the cell voltage emulation only is not sufficient to verify the BMS estimation algorithms, such as the State of Charge [12,13] and State of Health [14], which require the emulation of the temperature and the presence of a current signal, too. A low-cost freely-available battery emulator platform able to emulate the cell voltage, current, and temperature signals of a battery composed of series connected cells does not exist to the best of our knowledge. The aim of this paper is to overcome this limit by providing the scientific community with the design of a modular battery emulator available as open-hardware part [15].

The proposed power HIL platform is published under the Open Hardware License and allows small-size laboratories and the battery-interested community to self-produce a low-cost battery emulator with good performance for the development and the functional test of custom BMSs. This project also adds a new piece to the open hardware system developed to test and design lithium-ion batteries, which started in [16] where a low-cost cell characterization system was presented. The battery emulator is composed of a variable number of standard cell-emulator modules. They communicate with each other to emulate a battery composed of a variable number of series-connected cells. Each standard module is allocated in a rack in which up to eight cell emulator boards can be inserted, together with one board that emulates up to eight Negative Temperature Coefficient (NTC) thermistors, and one board that reproduces the output signal of the most commonly used current sensors. A specific interface connects the battery emulator to a PC that controls the entire system. The final goal is to enable the emulation of the voltage and current of each cell according to specific equivalent models of the cells, for example the equivalent electrical

3 of 15

circuit model with 2 RC branches provided with an electrical equivalent thermal model as shown in [17].

The main design aspects and the experimental characterization tests of the proposed cell emulator module are described in this paper. The background analysis is reported in Section 2, in which the best cell emulator structure is identified. The cell emulator design constraints are described in Section 3, the design is described in Section 4, and the experimental characterization tests are shown in Section 5. Section 6 reports the cell emulator comparison with other solutions presented in the literature. Finally, the conclusions are drawn in the last section.

2. Background

Very powerful high-end commercial battery emulators are available on the market, but they are often not affordable to small-size laboratories. For example, the Chroma 87001, the Hioki SS7081-50, and the Speedgoat IO991 commercial battery emulators are compared in [4]. On the other hand, several battery emulators have been presented in the literature. For example, the authors in [5] propose a power HIL solution based on a dSpace commercial platform. This solution guarantees a very short development time of the platform, but it is expensive and requires a commercial development software available with license. Ref. [6] proposes to emulate the cell behavior with a bidirectional DC/DC converter, and Ref. [7] presents a circuit in which a bipolar transistor V_{BE} multiplier circuit is used to emulate a cell. The last solution is very cheap, but it shows a rather low stability of the cell voltage with respect to the output power and circuit temperature variations. Moreover, it is not able to sink or source large current values. This last limitation also occurs in [8], in which the power HIL platform is divided in modules that emulate four cells each. The module is based on four Digital to Analog Converters (DAC). They set the cell output voltages that are amplified by four operational amplifiers. The operational amplifier utilized in [8] can sink and source up to 30 mA. This current value is sufficient to check the BMS cell voltage measurement functionality but it is too low to verify, for example, the balancing function that usually involves higher current levels [18].

Moreover, the architecture presented in [8] was improved by using a power operational amplifier able to manage current levels up to the amperes, as presented in [9,10]. In addition, the authors of these works developed a single-cell emulator able to be series-connected to emulate an entire battery. Each cell is equipped with a voltage and current measurement circuit and a microcontroller (μ C). The microcontroller sets the cell voltage according to the output of a 2-RC electrical model [19] of the cell and communicates with an external PC. The use of one microcontroller for each cell reduces the complexity of the control system but increases the emulator cost.

A very similar HIL platform is divided in three hierarchical levels to reduce the platform cost in [11]. The lower level of the platform is composed of the cell modules in which the microcontroller is omitted. The second layer is composed of a variable number of microcontroller boards, which manage up to four cell modules each, and communicate with a PC that constitutes the highest hierarchical level. This last architecture represents the best trade-off among cost, complexity, and flexibility. For this reason, it was the starting point from which the freely-available low-cost cell emulator board proposed in this work is developed.

3. Cell Emulator Constraints

The main design constraints of the cell emulator developed in this work stand in the output voltage and current values that must be reached. The output voltage range must be large enough to mimic all the different lithium-based battery technologies resulting in a voltage range from 1.5 to 4.5 V [20]. On the other hand, the maximum output current that the emulator must be able to sink or source depends on the BMS under test. Excluding the power path that is not emulated in this case, the BMS balancing system is the most demanding function with respect to the output current. Usually, the balancing system

is based on a passive or active approach. In the first one, the BMS connects a bleeding resistor to the most charged cells that are discharged until the charge stored in each battery cell is equalized [21]. The higher the balancing current, the shorter the balancing time. However, high balancing currents produce high dissipated power on the bleeding resistors that makes the thermal management of the BMS board challenging. Consequently, the passive balancing current is usually kept below 0.5 A, for a maximum dissipated power on each bleeding resistor of 2.25 W in the worst case of high-voltage lithium-ion cells.

Instead, active power balancing systems consist of a circuit able to move energy from the most charged cells to the lowest charged ones. Even though high-power active balancing systems have been investigated in the literature [22], their practical application is less common. Indeed, active balancing circuits may be rather expensive, and the continuous improvement of the cell production processes makes the cell mismatch and unbalance a less critical problem. Therefore, low-power passive balancing circuits are the most common solution applied in the present day BMSs. For these reasons, a maximum sink/source output current of 0.5 A is a reasonable constraint value for the cell emulator design described here.

Other important constraints of the emulator are the resolution of the output voltage, defined as the minimum voltage output variation, and the maximum voltage update frequency. These constraints depend on the BMS under test because the cell emulator resolution must be comparable to the resolution of the BMS measurement circuit. Usually, BMSs are equipped with analog to digital front-ends based on Analog to Digital Converters (ADC) with a voltage reference of 5 V and a number of bits from 12 to 16. The corresponding resolutions are 1.2 mV and 76 μ V, respectively. Moreover, the sampling period for the acquisition of the cell voltage is usually in the range from 100 ms to 1 s and can reach 10 ms in BMSs for specific applications. Therefore, a voltage update frequency for the emulator larger than the maximum sampling frequency of the BMS (e.g., 100 Hz) is sufficient to satisfy the requirement.

Finally, the cell emulator must be able to be series-connected with other cell emulators to compose a battery module. For this reason, the communication and the power input interface of the emulator must be isolated.

The design constraints of the cell emulator derived from the considerations reported above are summarized in Table 1.

Table 1. Design constraints of the cell emulator.

Feature	Requirement
Voltage range	0.5 to 4.5 V
Voltage resolution	\approx 76 μ V
Voltage update frequency	\geq 100 Hz
Maximum continuous source/sink current	0.5 A

4. Cell Emulator Circuit Design

The architecture of the battery cell emulator described in this work is shown in Figure 2. It is based on a DAC and a power operational amplifier. The operational amplifier defines the power output characteristics of the emulated cell, whereas the DAC determines the resolution of the output voltage.

The 16-bit Texas Instruments DAC8560 converter was used to achieve the required voltage resolution. This DAC generates the input voltage of the operational amplifier OPA567, manufactured by Texas Instruments, which is connected as non-inverting amplifier. It is a rail-to-rail amplifier with configurable maximum output current up to 2 A. Configuring the maximum source/sink current of the emulator is a very appealing feature. It could be useful to avoid unsafe situations during the early stage of the BMS development process, when firmware bugs or other faults could occur. The output voltage value V_{out} of the cell emulator can be obtained from the following equation:

$$V_{out} = G(nV_{ref}/2^N) \tag{1}$$

where *G* is the gain of the output power amplifier (G = 2), *n* is the DAC input code, V_{ref} is the DAC reference voltage (2.5 V), and *N* is the DAC number of bits (16 bit).



Figure 2. Architecture of the battery cell emulator described in this work.

A bidirectional current sensor, the Allegro MicroSystems ACS723LLCTR-05AB-T, is series-connected to the output to measure the sink/source current of the emulator. It is a Hall current sensor with range of ± 5 A, primary conductor resistance of 0.65 m Ω , and ratiometric analog output voltage from the power supply. The ADS1118 circuit, a 16-bit 4-channel Sigma-Delta ADC, is then used to acquire the output signal of the current sensor. At the same time, two other ADC input channels are used to measure the emulated cell output voltage and the power supply voltage of the emulator. The knowledge of the power supply voltage is needed for the conversion of the current sensor voltage in the measured current value.

Both the ADC and DAC integrated circuits are controlled with the same SPI interface by means of two different Chip Select signals. The Analog Devices ADUM3151 chip is used to isolate the communication with the module that controls the emulator and sets its parameters. Thus, the same SPI bus can be used for all the emulator cells when they are series-connected to compose the multi-cell battery used in the HIL platform. For the same reason, the emulator is equipped with an isolated DC/DC converter that supplies power to each component of the board.

The cell emulator was developed using the open source electronic design automation suite KiCad EDA [23], to encourage the project results sharing among the community. The project files can be downloaded from [15], in which the schematic, the Printed Circuit Board (PCB), the Bill Of Materials (BOM) and the GERBER files can be found. The estimated cost of one cell emulator is about 40 USD. The cost is split in 30 USD for the components and 10 USD for the PCB and the mounting service.

5. Experimental Characterization of the Cell Emulator

Four cell emulators were assembled and labeled from C#1 to C#4 to verify the cell emulator design and to measure its electrical characteristics. To this end, a very simple control system for the cells was developed using an NXP microcontroller evaluation board (LPCXpresso board with LPC1769 microcontroller) and a PC LabView interface. The first one implements the communication and control functions of the cell. It also acts as a bridge between the cell emulator and the PC interface. The second one consists of a simple user interface with which the output voltage of the cell emulator is set. It also acquires and shows to the user the quantities measured by the emulator. Moreover, the interface is able to control a sourcemeter Keithley 2460. It is used as power device that sinks and sources current from the cell emulator and accurately measures the output current and voltage using the 4-wire technique. These quantities are used as reference values to calculate the setting and measurement output voltage errors and the measurement current error of our emulator. The experimental setup is shown in Figure 3, in which one cell emulator, the



microcontroller evaluation board and the Keithley 2460 are shown. The other instrument visible in the picture is a Keithley 2420 that only supplies power to the cell emulator.

Figure 3. Experimental setup used for the cell emulator characterization.

5.1. Characterization Test Results for the Emulator Cell #1

The following results describe the characterization tests carried out on the emulator cell C#1. The same test procedure was applied to all the four emulator cells. They all present a very similar behavior, as it will be shown in the next subsection. The results pertaining to cell C#1 are thus representative of the general behavior of the cell emulator proposed here.

First of all, the complete sweep of the DAC value from 0 to the maximum value $(2^{16} - 1)$ was carried out to characterize the cell emulator output voltage. The output current was set to 0 in this test. This corresponds to the open circuit voltage of a real cell. The voltage measured from the sourcemeter is used as reference value. It is compared with the expected voltage value obtained from Equation (1) in the top chart of Figure 4. The bottom chart of Figure 4 shows the difference between the two quantities, i.e., the setting voltage error.



Figure 4. Characterization of the setting output voltage with no output current. Measured and expected values (**top**). Setting voltage error (**bottom**).

We note that the setting voltage error ranges from about -5 to -4 mV with an average value of -4.42 mV and a variance of $95 \mu V^2$ and that the error would be rather small (below 1 mV) if the offset was corrected.

The next test aims at characterizing the cell emulator when the output current varies. The cell emulator output voltage was changed from 0.5 V to 4.5 V with steps of 0.5 V and, for each voltage step, the current value was changed from -500 mA to 500 mA with steps of 100 mA. The duration of the current step was set to 300 s. The current was set again to 0

for 300 s at the end of the step to allow the emulator board to cool down. In this way, we can characterize the output voltage behavior as a function of the output current and, at the same

time, evaluate possible thermal effects on the performance due to the component heating. The setting voltage error of the cell is reported in the top diagram of Figure 5 as a function of the output voltage for every value of the output current. It is calculated by subtracting the mean value of the reference voltage measured by the sourcemeter in the first second (10 samples) of each current step to the expected value obtained with Equation (1). The calculation can be referred to the room temperature behavior because the components after one second are not heated yet. The continuous plot in Figure 5 is the setting error measured with no current, already shown in Figure 4. The bottom plot of Figure 5 shows the mean error calculated for a given value of the output current reported as a function of the current itself. It can be noted that the mean error in the setting voltage is fairly approximated with a linear function with respect to the output current. For this reason, the emulator output can be modeled with a voltage generator, the value of which is the setting voltage plus the offset setting error, and a resistor equal to the slope of the linear function that is equal to $5.6 \,\mathrm{m}\Omega$ in this case.

The measurement setup chosen for the cell emulator characterization also allows us to extract information about the behavior of the emulated cell as a function of the temperature. In fact, the test when the output current is sunk or sourced lasts 5 min. The emulator cell board shows an evident temperature change during the test, due to the power dissipated in the active devices. If the first measured data can be associated to the room temperature behavior, the last data are associated to the highest temperature reached during the experiment. Thus, the evaluation of the effect of the temperature is obtained by comparing the mean output voltage values measured in the first and last second (10 samples) of the test performed for each current step. The difference between the two extreme situations results to be lower than 0.8 mV for all the steps, showing a rather limited effect of the temperature on the cell emulator performance.



Figure 5. Characterization of the setting output voltage with different cell current values. Error as a function of the output voltage for different output currents (**top**). Mean error as a function of the output current (**bottom**).

Nevertheless, the thermal behavior was experimentally investigated focusing on the power amplifier. The power P_{diss} dissipated by the operational amplifier is expressed as:

$$\begin{cases}
P_{diss} = (V_{cc} - V_{out})I_{out} & \text{if } I_{out} > 0 \\
P_{diss} = -V_{out}I_{out} & \text{if } I_{out} < 0
\end{cases}$$
(2)

where V_{cc} is the power supply voltage (5 V), and I_{out} is the cell emulator output current (positive if the current is sourced by the emulator). The worst cases occur if $V_{out} = 4.5$ V and $I_{out} = -0.5$ A, or when $V_{out} = 0.5$ V and $I_{out} = +0.5$ A. The OPA567 dissipates 2.25 W in these cases, and reaches a steady-state temperature around 125 °C with a room temperature of 30 °C. Figure 6a shows the amplifier temperature versus time during a test in which the cell emulator works in the worst case for about 12 min. The temperature was acquired by a FLIR i50 infrared camera. Figure 6b–d show the screenshots of the camera acquired before, after 10 s, and after 10 min from the application of power pulse, respectively. The experiment shows that the device reaches a temperature very close to the maximum limit allowed by the manufacturer.



Figure 6. OPA567 temperature, measured with a FLIR i50 infrared camera, during the worst case test in which the amplifier dissipates 2.25 W for about 12 min (**a**). Camera screenshots acquired before (**b**), after 10 s (**c**), and after 10 min (**d**) from the application of the power pulse.

If we take into account that the cell emulator is also provided with autonomous channels for the current and voltage measurements, the same tests were also used to characterize the emulator measurement system. The characterization is carried out by comparing the output voltage and current measured by the cell emulator circuit with the reference values measured by the sourcemeter. In particular, the voltage measurement error ($V_{measure_{err}}$) is obtained by subtracting to the reference value the mean value of the first 100 voltage samples (10 s) for each test step. This error is reported in the top plot of Figure 7. As we can note, the absolute value of the measurement error is always below 2 mV for every test conditions, showing a good performance of the voltage measurement circuit. Moreover, the bottom plot of Figure 7 reports the mean error value as a function of the output current. The mean error shows a rather linear behavior that can be approximated



with the function $aI_{out} + b$, where I_{out} is the output current value, a is $1.9 \text{ m}\Omega$ and b is -0.75 mV.

Figure 7. Characterization of the cell emulator measurement system with different cell current values. Error as a function of the output voltage for different output currents (**top**). Mean error as a function of the output current (**bottom**).

The same analysis is repeated to characterize the current measurement channel. The results are shown in Figure 8. The top plot shows the measurement error as a function of the output voltage for different current values. The bottom plot of Figure 8 shows the mean current error as a function of the current value. As we can note, the mean current error is rather constant for negative (sink to the emulator) current values. It is about -20 mA. Instead, it drops rather linearly with the current for positive current values, i.e. the emulator is sourcing the current. The linear fitting function $cI_{out} + d$ yields *c* and *d* equal to 0.051 and -23.8 mA, respectively.

Finally, the response time of the cell emulator to the request of a step change of the output voltage was evaluated by means of a Tektronix MSO56 oscilloscope. The scope acquired the SPI signals to the DAC, its output voltage, and the emulator cell voltage as a function of time. Two cell output voltage step transients from 0.5 V to 4.5 V and vice-versa were considered to measure the response time. Moreover, the step transients were carried out with three current values, -0.5 A, 0 and 0.5 A. The response time consists of two main contributions: the configuration time of the DAC and the time that the operational amplifier takes to set to the new voltage value. In particular, the configuration time of the DAC is the sum of the communication time over the SPI bus and the time needed to change the DAC output voltage. The latter is measured as less then 2 µs in all the tests. Instead, the communication time depends on the SPI speed chosen and the number of bits needed to configure the DAC, which are 100 kbit s⁻¹ and 24 bit, respectively. Therefore, the configuration time is about 240 µs with the parameters mentioned before. This time could strongly be reduced by increasing the DAC SPI speed that can reach a maximum of 30 Mbit s^{-1} .



Figure 8. Characterization of the cell emulator measurement system for different current values. Measurement error for different output currents (**top**). Mean current error as a function of the output current (**bottom**).

Instead, the settling time of the operational amplifier depends on the voltage and current values. However, it is lower than 100 µs for all the tests carried out. In conclusion, the measured response time of the cell emulator is always less than 340 µs, which corresponds to a maximum frequency for the voltage update of about 3 kHz. Even if this frequency could easily be increased, the value achieved is by far sufficient for the application that considers the emulator a tool for the HIL validation of a BMS.

5.2. Comparison of 4 Cell Emulator Instances

The characterization test was repeated for all the instances of the cell emulator that were realized. The aim was to verify, even if for a low number of items, the mismatches among the various elements. The results obtained from each sample of the cell emulator are very similar one to the other. The measured error trends are very similar with different coefficients of the approximating error functions introduced in the previous subsection. For example, the voltage setting errors measured on the four cells are reported in Figure 9. In particular, the top plot of the figure shows the mean voltage setting errors of the four cell emulators. The bottom plot shows the same error when the mean error value at zero current is subtracted to it. As we can note, the four emulator samples show very similar behaviors except for a noticeable offset difference among them. The voltage setting error can be modeled with an offset setting error of -2.5 ± 2.17 mV and a resistor in the range from $4.6 \text{ m}\Omega$ to $5.7 \text{ m}\Omega$.

The mean voltage and current measurement errors as a function of the output current are then reported in Figure 10 for the four cell emulator samples. As far as the voltage measurement error is concerned, all the samples show a behavior very similar one to

the other. The linear fitting parameters defined in the previous subsection are *b* equal to $-0.63 \pm 0.12 \text{ mV}$ and *a* in a range from 1.6 to $1.9 \text{ m}\Omega$. Instead, the current measurement error shows a significant offset value variation in the four cell emulators that goes from -30.8 mA for cell #2 to 8.17 mA for cell #4. Despite the offset variation, the shape of the current error function is similar for all the cell emulators, with a rather linear trend for positive current values.



Figure 9. Comparison of the voltage setting error measured on the four samples of the cell emulator. Error as a function of current (**top**). Error when the offset is corrected (**bottom**).



Figure 10. Mean voltage and current measurement errors as a function of the output current measured on the four samples of the cell emulator. Mean voltage error (**top**). Mean current error (**bottom**).

6. Discussion and Future Developments

The experimental results described in the previous section show that the cell emulator design proposed in this paper satisfies the constrains reported in Table 1 and that the design goals are fully achieved. In fact, the setting and measurement voltage errors are fully compatible with the application in which the emulator will be used, i.e., the development, validation and characterization of a BMS without a real battery in an HIL configuration. The offset error of the output current measurement and its variation with respect to the output current value are acceptable if the emulator is used to just check the basic BMS functionality. Instead, they seem too high if the cell emulator is used for the assessment of the BMS estimation algorithms. In this case, the emulator current measurement accuracy should be improved to constitute a reliable reference for comparison to the current measurements performed by the BMS itself. A more accurate current sensor could be used with the obvious drawback of an increased overall cost of the emulator. To improve the emulator flexibility and try to address the current accuracy issue, one unused input channel of the ADC was made available in the auxiliary connector of the board. This analog input can be used to acquire the output signal of an external more accurate current sensor. This sensor could be added when the application requires a measurement of the output current more accurate than the value available with the standard sensor mounted on the board.

Finally, the cell emulator described here is compared with other solutions presented in the literature to highlight strengths and weaknesses of the proposed solution. Table 2 reports the comparison of our cell emulator to a commercial one used in [5], and other two emulators presented in [9,10], that are based on an architecture similar to that adopted in our work. The comparison data come from the experiments described above in our case, whereas simulated or theoretical data are only reported in the other cases. Therefore, our solution is the only one that was subjected to a thorough experimental characterization. The weakest point of comparison for our emulator is the output current that shows the lowest value and the lowest accuracy. The latter comes from the choice of a very cheap current sensor that keeps the overall cost very low, one of the main features of our solution. Nevertheless, the emulator provides the possibility of adding an external current sensor with accuracy tailored to the application requirement. As far as the current value is concerned, a source/sink current of 0.5 A is sufficient to check most of the functionalities of the BMS. This current limit is due to the thermal design of the PCB that limits the maximum power dissipated by the output operational amplifier. A source/sink current up to 2 A can be achieved by simply increasing the size of the thermal pad of the operational amplifier, a correction that will be applied to the next release of the board. Another comparison parameter that seems to show a weaknesses of our solution is the measured set time. It consists of the 2 µs DAC setting time, the 240 µs communication time, and the 100 µs output setting time of the operational amplifier. The communication time can easily be reduced by increasing the SPI speed from 100 kHz up to 30 MHz. We end up with a set time of the order of one hundred of microsecond.

On the other hand, the comparison highlights very good results regarding the resolution and accuracy of the output voltage. It is worth reminding that the data reported in [9,10] are theoretical and simulated results, whereas we present experimental data. Moreover, our whole design is freely available to anyone who wants to build his own battery emulator. In conclusion, the cell emulator presented in this work stands for its low-cost and very good performance in voltage accuracy and resolution and its availability to the scientific community.

However, the characterization tests showed some design weaknesses of the emulator that should be addressed in the next improved version of the design. For example, the thermal management of the output power operational amplifier must be improved, because the device reaches a too high temperature when the cell emulator is used with large output voltage and current values. The thermal design is going to be revised and a larger thermal dissipation area will be provided in the next hardware version.

Work	[5] ⁴	[9]	[10]	Our Work
Cell Architecture	Commercial (dSpace HIL)	OPAMP μC with internal 12b DAC/ADC	OPAMP μC with external 16b DAC/ADC	OPAMP 16b DAC/ADC
Voltage resolution	120 µV	1.2 mV ²	$92\mu V$ 3	76 µV
Voltage accuracy	$\pm 1mV$	1.2 mV ²	$\pm 270\mu V^{3}$	± 2.17 mV 5
Max Current	2 A	3–5 A	3 A	0.5 A
Current accuracy	NS ¹	2 mA ²	$\pm 462\mu A^{3}$	\pm 19.6 mA ⁵
set time	31.25 µs	5 µs	1.26 µs	340 µs
cost	very high	low	medium	very low

Table 2. Comparison of our cell emulator with the literature.

¹ Not Specified; ² Theoretical data; ³ Spice simulation results; ⁴ Data from DSpace website; ⁵ With offset correction.

7. Conclusions

The design of a circuit that emulates a battery cell is described in this work. Four cell-emulator circuit prototypes are experimentally characterized. Their performance in terms of setting voltage error and resolution is reported. The performance of the emulator measurement voltage and current channels is also characterized by comparing the emulator measured data with those measured with a laboratory instrument reference. The experimental results show the very good performance of the voltage generation and the voltage measurement capability with a voltage resolution of 76 μ V, an accuracy of 2.17 mV, and a setting time of 340 μ s. Instead, the current measurement channel suffers the choice of a low-cost current sensor that is sufficient in most applications. However, it can easily be replaced with a more accurate one in applications demanding a higher current measurement accuracy.

The comparison with other emulators presented in the literature is also reported. It takes into account experimental data in our case and simulated or calculated data in the other cases. Our battery cell emulator includes voltage and current measurements in addition to the voltage generation. It stands for the very low cost and constitutes a very good trade-off between cost, performance, complexity and flexibility. Moreover, the project is fully characterized with laboratory experiments. Some design weaknesses, in particular the thermal design of the output power amplifier, are going to be addressed in the revised version of the hardware platform.

The emulator features fully satisfy the requirements needed in the development and the functional characterization of custom BMSs. Indeed, the cell emulator circuit is modular so that it can be series connected to form a "virtual" multi-cell battery. Thus, the hardware-in-the-loop approach can be applied to validate the BMS under test in a batteryless framework, with intrinsic safety improvement of the test. Finally, the battery cell emulator circuit described here is available to the scientific community as open hardware platform freely downloadable. It could be useful to small-size laboratories to self-produce low-cost battery emulators with good performance for the development and the functional test of custom BMSs.

Author Contributions: Methodology, R.D.R. and R.R.; data curation, A.V.; writing—original draft preparation, R.D.R; writing—review and editing, A.V., F.B. and R.S.; supervision, R.R.; project administration, R.S. All authors have read and agreed to the published version of the manuscript.

Funding: This research was partially funded by PAR FAS Toscana 2007–2013 (Bando FAR FAS 2014), under agreement n. 4421.02102014.072000022 Project SUMA, and supported by CrossLab project, University of Pisa, funded by MIUR "Department of Excellence" program.

Acknowledgments: The authors wish to thank Antonio Colicelli for his administrative support.

Conflicts of Interest: The authors declare no conflict of interest.

References

- 1. Wu, H. Hardware-in-loop verification of battery management system. In Proceedings of the 2011 4th International Conference on Power Electronics Systems and Applications, Hong Kong, China, 8–10 June 2011. [CrossRef]
- Barreras, J.V.; Fleischer, C.; Christensen, A.E.; Swierczynski, M.; Schaltz, E.; Andreasen, S.J.; Sauer, D.U. An Advanced HIL Simulation Battery Model for Battery Management System Testing. *IEEE Trans. Ind. Appl.* 2016, 52, 5086–5099. [CrossRef]
- Morello, R.; Baronti, F.; Tian, X.; Chau, T.; Di Rienzo, R.; Roncella, R.; Jeppesen, B.; Lin, W.H.; Ikushima, T.; Saletti, R. Hardwarein-the-loop simulation of FPGA-based state estimators for electric vehicle batteries. In Proceedings of the IEEE International Symposium on Industrial Electronics, Santa Clara, CA, USA, 8–10 June 2016; pp. 280–285. [CrossRef]
- Tschritter, C.D.; Wetz, D.A.; Turner, G.K.; Heinzel, J.M. Battery Management System (BMS) Test Stand Utilizing a Hardware-inthe-Loop (HIL) Emulated Battery. In Proceedings of the 2021 IEEE Electric Ship Technologies Symposium (ESTS), Arlington, TX, USA, 3–6 August 2021. [CrossRef]
- Bui, T.M.; Niri, M.F.; Worwood, D.; Dinh, T.Q.; Marco, J. An Advanced Hardware-in-the-Loop Battery Simulation Platform for the Experimental Testing of Battery Management System. In Proceedings of the 2019 23rd International Conference on Mechatronics Technology (ICMT), Salerno, Italy, 23–26 October 2019. [CrossRef]
- 6. Mishra, S.; Tamballa, S.; Pallantala, M.; Raju, S.; Mohan, N. Cascaded Dual-Active Bridge Cell Based Partial Power Converter for Battery Emulation. In Proceedings of the 2019 20th Workshop on Control and Modeling for Power Electronics (COMPEL), Toronto, ON, Canada, 17–20 June 2019. [CrossRef]
- Di Rienzo, R.; Roncella, R.; Morello, R.; Baronti, F.; Saletti, R. Low-cost modular battery emulator for battery management system testing. In Proceedings of the 2018 IEEE International Conference on Industrial Electronics for Sustainable Energy Systems (IESES), Hamilton, New Zealand, 31 January–2 February 2018; pp. 44–49. [CrossRef]
- 8. Van Sterkenburg, S.; Fleuren, T.; Veenhuizen, B.; Groenewegen, J. Design and test of a battery pack simulator. In Proceedings of the 2013 World Electric Vehicle Symposium and Exhibition (EVS27), Barcelona, Spain, 17–20 November 2013. [CrossRef]
- Collet, A.; Crebier, J.C.; Chureau, A. Multi-cell battery emulator for advanced battery management system benchmarking. In Proceedings of the 2011 IEEE International Symposium on Industrial Electronics, Gdansk, Poland, 27–30 June 2011; pp. 1093–1099. [CrossRef]
- Buccolini, L.; Orcioni, S.; Longhi, S.; Conti, M. Cell Battery Emulator for Hardware-in-the-Loop BMS Test. In Proceedings of the 2018 IEEE International Conference on Environment and Electrical Engineering and 2018 IEEE Industrial and Commercial Power Systems Europe (EEEIC/ICPS Europe), Palermo, Italy, 12–15 June 2018. [CrossRef]
- Bischof, S.; Kuecuek, C.; Blank, T.; Weber, M. A battery cell emulator for hardware in the loop tests of reconfigurable lithium-ion and post-lithium batteries. In Proceedings of the PCIM Europe 2018; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management, Nuremberg, Germany, 5–7 June 2018; pp. 245–251.
- Morello, R.; Zamboni, W.; Baronti, F.; Di Rienzo, R.; Roncella, R.; Spagnuolo, G.; Saletti, R. Comparison of state and parameter estimators for electric vehicle batteries. In Proceedings of the IECON 2015-41st Annual Conference of the IEEE Industrial Electronics Society, Yokohama, Japan, 9–12 November 2015; pp. 5433–5438. [CrossRef]
- 13. Zhang, M.; Wang, K.; Zhou, Y.T. Online state of charge estimation of lithium-ion cells using particle filter-based hybrid filtering approach. *Complexity* **2020**, 2020, 8231243. [CrossRef]
- 14. Li, Q.; Li, D.; Zhao, K.; Wang, L.; Wang, K. State of health estimation of lithium-ion battery based on improved ant lion optimization and support vector regression. *J. Energy Storage* **2022**, *50*, 104215. [CrossRef]
- 15. Modular Battery Emulator. Available online: https://github.com/batterylabunipi/Modular_Battery_Emulator (accessed on 18 February 2022).
- 16. Carloni, A.; Baronti, F.; Di Rienzo, R.; Roncella, R.; Saletti, R. Open and Flexible Li-ion Battery Tester Based on Python Language and Raspberry Pi. *Electronics* **2018**, *7*, 454. [CrossRef]
- 17. Morello, R.; Di Rienzo, R.; Roncella, R.; Saletti, R.; Baronti, F. Hardware-in-the-loop platform for assessing battery state estimators in electric vehicles. *IEEE Access* 2018, *6*, 68210–68220. [CrossRef]
- Vereb, S.; Balazs, G.G.; Kokenycsi, T.; Suto, Z.; Varjasi, I. Application Dependent Optimization of Balancing Methods for Lithium-ion Batteries. In Proceedings of the 2018 IEEE 18th International Power Electronics and Motion Control Conference (PEMC), Budapest, Hungary, 26–30 August 2018; pp. 223–228. [CrossRef]
- 19. Chen, M.; Rincon-Mora, G.A. Accurate Electrical Battery Model Capable of Predicting Runtime and I-V Performance. *IEEE Trans. Energy Convers.* **2006**, *21*, 504–511. [CrossRef]
- Tarascon, J.M.; Armand, M. Issues and challenges facing rechargeable lithium batteries. *Nature* 2001, 414, 359–367. [CrossRef] [PubMed]
- Di Rienzo, R.; Zeni, M.; Baronti, F.; Roncella, R.; Saletti, R. Passive balancing algorithm for charge equalization of series connected battery cells. In Proceedings of the 2020 2nd IEEE International Conference on Industrial Electronics for Sustainable Energy Systems (IESES), Cagliari, Italy, 1–3 September 2020; pp. 73–79. [CrossRef]

- 22. Ghotekar, A.A.; Kushare, B.E. Review paper on recent active voltage balancing methods for supercapacitor energy storage system. In Proceedings of the 2019 5th International Conference On Computing, Communication, Control And Automation (ICCUBEA), Pune, India, 19–21 September 2019. [CrossRef]
- 23. KiCad EDA-Schematic Capture PCB Design Software. Available online: https://www.kicad.org/ (accessed on 18 February 2022).