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A Band-Pass Instrumentation Amplifier Based on a Differential Voltage Current Conveyor for Biomedical Signal Recording Applications

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Abstract: Recently, due to their abundant benefits, current-mode instrumentation amplifiers have received considerable attention in medical instrumentation and read-out circuit for biosensors. This paper is focused on the design of current-mode instrumentation amplifiers for portable, implantable, and wearable electrocardiography and electroencephalography applications. To this end, a CMOS differential voltage second-generation current conveyor (DVCCII) based on a linear transconductor is presented. A new band-pass instrumentation amplifier, based on the designed DVCCII, is also implemented in this paper. The concept of the proposed differential voltage current conveyor and instrumentation amplifier is validated numerically and their predicted performance is presented. The simulation results of the presented circuits were tested for 0.18 µm TSMC CMOS technology in a post layout simulation level using the Cadence Virtuoso tool with a ±0.9 V power supply, and demonstrated that the designed DVCCII has a wide dynamic range of ±400 mV and ±0.85 mA and a power consumption of 148 µW. The layout of the DVCCII circuit occupies a total area of 0.378 µm^2. It is shown that the designed DVCCII benefits from good linearity over a wide range of input signals and provides a low input impedance at terminal X. Two versions of the proposed band-pass instrumentation amplifier using pseudo resistances were designed with different specifications for two different applications, namely for EEG and ECG signals. Numerical analyses of both designs show proper outputs and frequency responses by eliminating the undesired artifact and DC component of the EEG and ECG input signals.

Keywords: bio-potential signals; band-pass instrumentation amplifier; differential voltage current conveyor; ECG; EEG

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1. Introduction

Cardiovascular diseases and strokes remain the two biggest causes of death worldwide [1,2]. Thus, monitoring and recording electrocardiogram (ECG) and electroencephalogram (EEG), bio-potential signals from the heart and brain of patients, are essential in the analysis of various physiological parameters and diagnosis [3,4]. An effective method for monitoring these signals while patients are moving around to do their daily activities is to utilize non-invasive, wearable, and implantable systems [1,3–8].

Among various types of medical instrumentation and read-out circuits for biosignals, current-mode integrated circuits have recently gained considerable attention due to their numerous benefits, such as large bandwidth, wide dynamic range, high linearity, low power consumption, and simple circuitry. Therefore, various types of current conveyors are the most widely used current-mode active building blocks [9–14]. The second-generation current conveyor (CCII), one of the most versatile current mode building blocks, was introduced by Sedra and Smith in 1970 [15]. The CCII has proved to be an efficient building block

for application in numerous high frequency analog circuits, such as filters [6,15–20] and current-mode oscillators [21,22]. Recently, it has also been used in biomedical applications, such as instrumentation amplifiers [11,23–25]. One limitation of CCII is that the circuit has only one high-impedance terminal, which is not suitable for applications, such as the impedance converter or differential current-mode amplifiers where two high-impedance terminals are required. In order to address this limitation, the concept of a differential voltage current conveyor (DVCC) is proposed in [26,27]. As shown in Figure 1, a DVCC device is a four-terminal circuit, which has one low impedance input terminal X, two high-impedance input terminals Y_1 and Y_2, and one high-impedance output node Z.

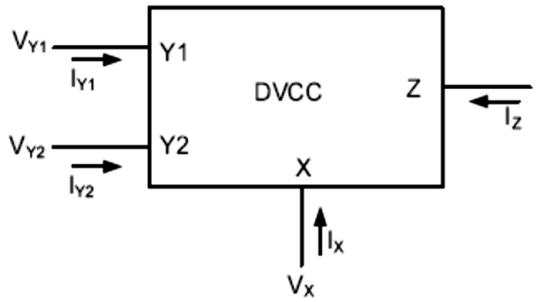


Figure 1. Differential voltage CCII block diagram.

The relation between the voltages and currents of the terminals is given by the following matrix:

$$\begin{bmatrix} I_{Y1} \\ I_{Y2} \\ V_X \\ I_Z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 1 & -1 & 0 & 0 \\ 0 & 0 & 1 & 0 \end{bmatrix} \begin{bmatrix} V_{Y1} \\ V_{Y2} \\ I_X \\ V_Z \end{bmatrix}$$

where,

$$V_X = V_{Y1} - V_{Y2}, I_Z = I_X$$

The differential voltage between two input terminals, Y_1 and Y_2, appears at the terminal X, and the current injected into terminal X is being replicated to the output terminal Z. Thus, in an ideal DVCC the input resistance at terminal X is zero, and the resistance at terminal Z and both Y terminals is infinity. Therefore, a current flowing through Y_1 and Y_2 terminals is ideally zero. In practice, however, the input resistances and currents in DVCCs are different from the ideal case. Another desirable characteristic is the linearity of the device.

To address these issues, in this paper, a new design of a DVCCII with good linearity and low input and output impedance is presented. In addition, in the following, an instrumentation amplifier based on the designed DVCCII is presented. Instrumentation amplifiers (IAs) have found many applications in medical instrumentation: the read-out circuit of biosensors, electrocardiography, data acquisition, etc. [8,28–33]. To extract the low-value differential signals in the presence of large-value unwanted common-mode signals and noise, IAs with a high common-mode rejection ratio (CMRR) are required. For many years, voltage-mode instrumentation amplifiers (VMIAs) with three operational amplifiers (op-amps) and seven resistors were used for this purpose [8,34]. These circuits suffer from high power consumption due to the use of three op-amps and resistors, relatively complicated circuits, and limited bandwidth (BW). In addition, they require precise resistor matching to achieve high CMRR. After the introduction of the current-mode design to solve major problems associated with conventional VM, CM instrumentation amplifiers received considerable attention [11,32]. Instead of VM op-amps, CM building blocks, such as second-generation current conveyors (CCIIs), operational floating current conveyors (OFCC), differential voltage current conveyors (DVCCs), etc., are employed to design a new class of instrumentation amplifiers [11]. Compared with conventional VMIAs, CMIAs

do not require matched resistors to provide a high CMRR. They also offer the extended differential mode gain independent of bandwidth [11,25,32].

Moreso, note that in the context of EEG and ECG signals, wideband performance is not required. Therefore, this study has been focused on the application of CMIAs to benefit from other advantages of current-mode amplifiers, such as a simpler circuitry, smaller on-chip area, low power consumption, and higher linearity. These are important features, especially in portable devices such as implantable and wearable biomedical microsystems, where the size and avoiding passive off-chip elements, weight, and power consumption—due to the limitation of battery usage—are critical issues. This study was not aimed at achieving a wide bandwidth, however, this feature has been achieved as a byproduct.

The structure of the paper is as follows. The proposed DVCC circuit is presented and discussed in the next section. In order to validate the DVCC design, simulation results using CAD tools in a post layout level and the realization of a DVCC-based instrumentation amplifier are also provided in the methods section. The applications of the proposed instrumentation amplifier for ECG and EEG signal filtering and amplification are presented in the results section. Finally, the achievements of the study are highlighted in the conclusion.

2. Methods

2.1. DVCCII Circuit

The schematic of the designed DVCCII, which is based on two wide linear range transconductor stages, is depicted in Figure 2. The pair of transconductors are formed by transistors M_1 to M_{10}. These two stages should have equal output currents. The voltage follower stage is connected to the outputs of these two identical transconductors, such that the I3 and I4 currents are equal in magnitude. Thus:

$$I_1 = I_2, \text{ therefore : } I_3 + I_4 = 0$$

Using this configuration, since the transconductor stages are identical (with the same transistor sizing) and one of the inputs of the second transconductor (gate of M_3) is grounded, the voltage at terminal X follows the voltage difference of the terminals Y_1 and Y_2. Note that this is valid, as long as both output currents are linear and M_1–M_4 are in saturation.

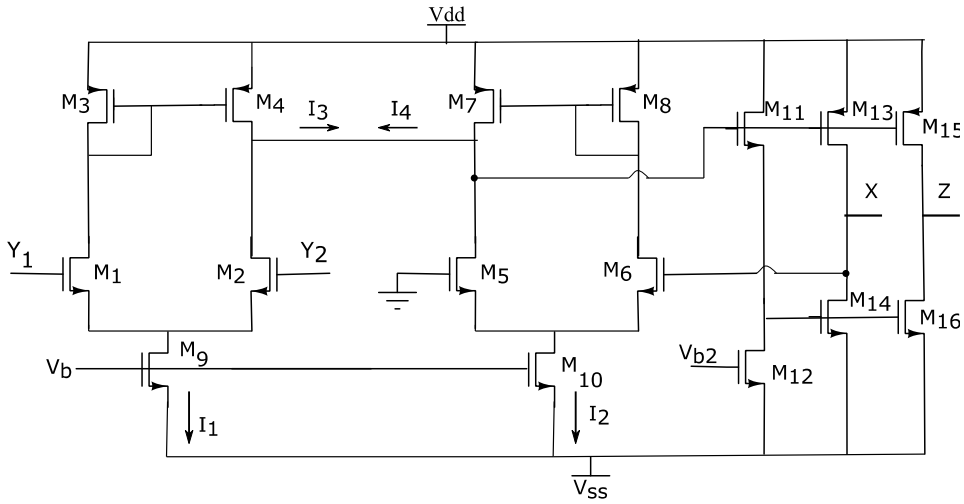


Figure 2. CMOS realization of the designed DVCC. The differential voltage between two input terminals, Y1 and Y2, appears at the X terminal and the current injected at X terminal is being replicated to the output.

The output stage is formed by a Class-AB CMOS push–pull network that guarantees high current driving capability and low standby current. The current at terminal X is transferred to terminal Z through transistors M_{15} and M_{16}. Thus, for achieving unit current

gain, M_{15} and M_{16} must be matched with M_{13} and M_{14}, respectively. All transistors are sized to operate in the saturation region. The size of the transistors is listed in Table 1.

Table 1. Transistor sizing of the designed DVCC.

Transistors	W (μm)	L (μm)
M1–M4	1.8	3
M5–M8	0.9	0.8
M9–M10	9.5	1.4
M11–M12	0.5	0.3
M13–M16	5	0.2

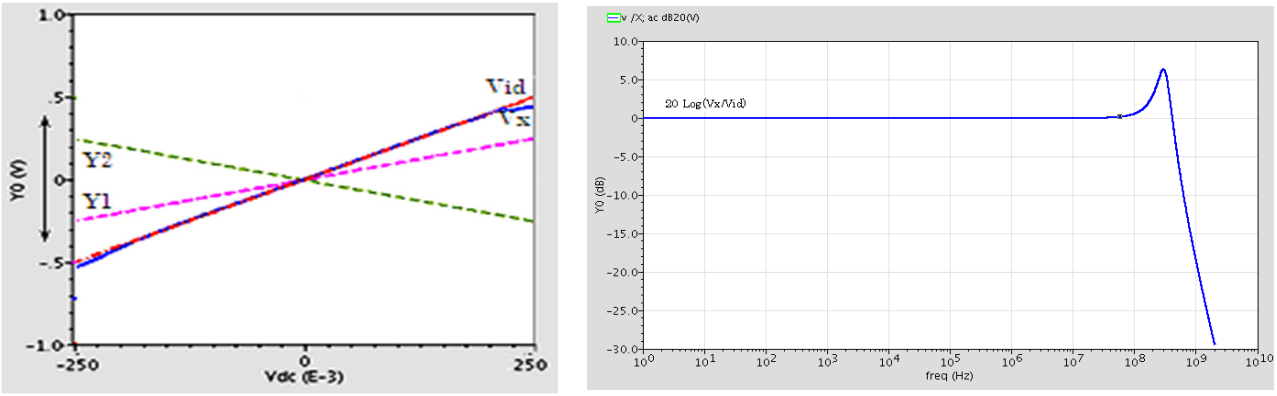
2.2. Post Layout Simulation Results

In order to validate the proposed DVCC, it was simulated using Cadence. TSMC 0.18 μm standard CMOS technology was used for the simulation. Transistor sizes that were used in the simulation correspond to those listed in Table 1. The utilized power supply was ±0.9 V.

Since the ports X and Z have unity current gains, in order to calculate the currents I_x and I_z to depict the $\frac{I_z}{I_x}$ curve, both ports are terminated with 5 KΩ resistances. Moreso, note that port X is an output voltage port that has a small output resistance. Therefore, it should be loaded with a relatively large resistor. A 5 KΩ resistor seems to be large enough for this purpose.

In order to investigate the linearity of the proposed circuit, the variations of the output voltage at terminal X versus variations in $V_{id} = V_{Y1} - V_{Y2}$ are depicted in Figure 3a. The figure shows good linearity for differential input voltages between ±0.4 V. The offset voltage is also measured 2.24 mV and it is small enough. The offset voltage is the voltage of terminal X when V_{id} is equal to zero or is grounded.

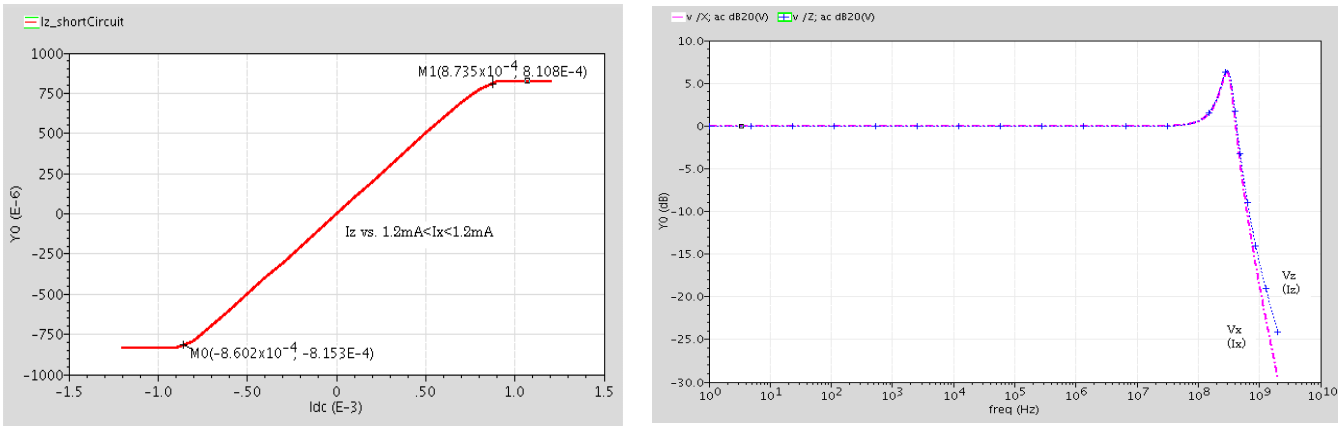
Figure 3b shows the voltage frequency response of the DVCC. It shows a flat response with a unity voltage gain (V_x/V_{id}) of 80 MHz and a 3 dB bandwidth of 450 MHz.



(**a**) (**b**)

Figure 3. (**a**) The X terminal output voltage versus changes of V_{id}. (**b**) Frequency response of the DVCC.

The output current at terminal Z versus the input current at terminal X, when terminal Z is shorted and the I_x current source is injected into terminal X, is shown in Figure 4a. The figure shows a ±0.85 mA linear range. Figure 4b shows the current frequency response of the DVCC. As seen, this DVCC has a good flat I_z/I_x response with a unity gain up to about 80 MHz and its 3 dB bandwidth is equal to 450 MHz.



(**a**) (**b**)

Figure 4. (**a**) Output current of terminal Z versus terminal X input current, when terminal Z is shorted. (**b**) Current frequency response (I_z/I_x) of the DVCC.

The simulated input impedance of terminal X, i.e., R_X, is smaller than 20 ohm at DC and low frequencies. Variations of R_x versus frequency is depicted in Figure 5. The value of Rx is also lower than 1 KΩ up to 3 dB frequency, demonstrating that port X can operate as a low impedance output port.

All results are summarized in Table 2. The table shows this design has proper characteristics for a DVCC.

The layout of the proposed DVCCII using the Cadence tool with TSMC 0.18 µm standard CMOS technology is depicted in Figure 6. The on-chip area with this layout is estimated to be equal to 378 μm^2.

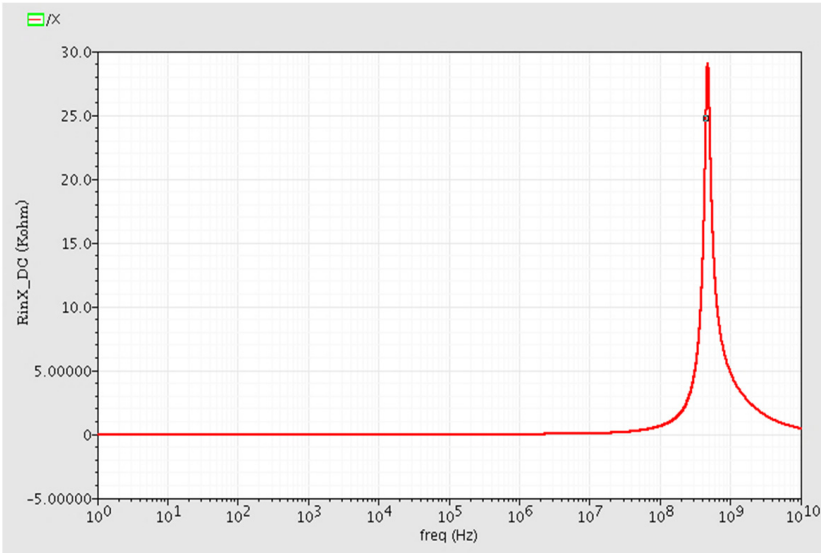


Figure 5. The X terminal input resistance R_X versus frequency changes. It is measured less than 20 ohm in low frequency and DC operation regions.

Table 2. Simulation results of designed DVCCII.

Parameter	Value
Technology	0.18 μm TSMC CMOS
Power Supply	±0.9 V
Linear Dynamic Range for V_x vs. V_{id}	±400 mV
X Terminal Offset Voltage	2.24 mV
Linear Dynamic Range for I_z vs. I_z	−0.85 mA~0.87 mA
X Terminal Voltage BW, f_u	BW = 450 MHz, f_u = 80 MHz
Z Terminal Current BW, f_u	BW = 450 MHz, f_u = 80 MHz
RinX (X Terminal Input Resistance)	f < 1 MHz: R = 20 ohm f up to 100 MHz: R < 600 ohm
On-chip area	378 μm^2
Total Power Dissipation	148 μW

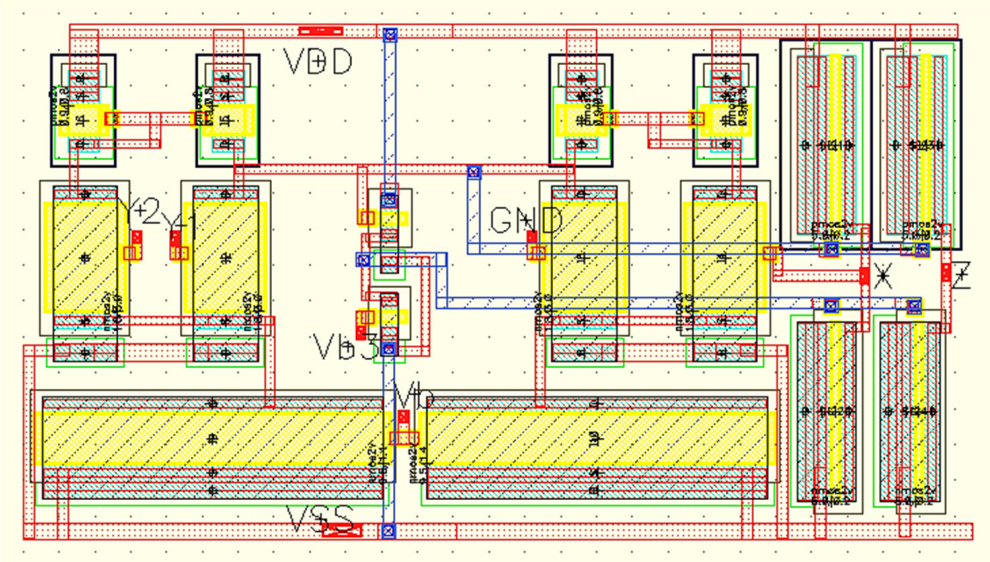
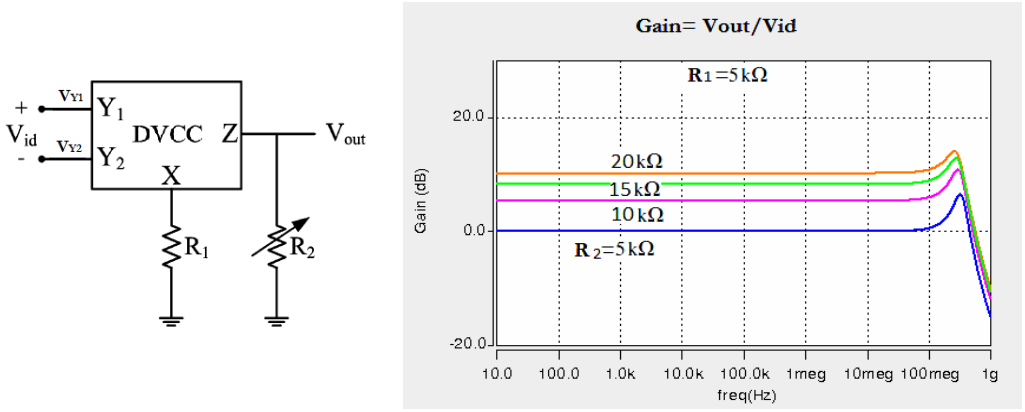


Figure 6. The layout of the proposed DVCCII using Cadence with TSMC 0.18 μm standard CMOS technology.

It is worth mentioning, that by decreasing the supply and bias voltages, the linear dynamic range of the output voltage is restricted to ±0.3 V, and the frequency band of flat response with a unity voltage gain is reduced to about 38 MHz, but, consequently, the power consumption will be reduced to about 39 μW.

2.3. Design of DVCC-Based Instrumentation Amplifier

This section is devoted to the design of an instrumentation amplifier using the presented DVCC and its application in the amplification and filtering of low frequency biomedical signals. The block diagram and related voltage gains of the circuit for different values of resistance R_2 are depicted in Figure 7. The gain of the instrumentation amplifier is given by $Av = \frac{V_{out}}{V_{id}} \approx \frac{R_2}{R_1}$.



(**a**) (**b**)

Figure 7. (**a**) The block diagram of the instrumentation amplifier implemented using the presented DVCC, (**b**) Voltage gains for different resistances at the output of this instrumentation amplifier.

Features of the designed CMIA are presented in Table 3. The table also highlights the advantages of the proposed amplifier in terms of power consumption, on-chip area, bandwidth, etc., compared to other studies.

Moreso, note that the designed CMIA also benefits from a large BW as a byproduct. To limit the bandwidth to the required frequency band, we then used a filter. The proposed configuration for filtering specified frequency bands, which leads to forming a band-pass instrumentation amplifier, is shown in Figure 8. However, note that in addition to the application in EEG/ECG recordings, the designed DVCC and CMIA are general designs that can be used for many applications with a wide BW up to 450 MHz.

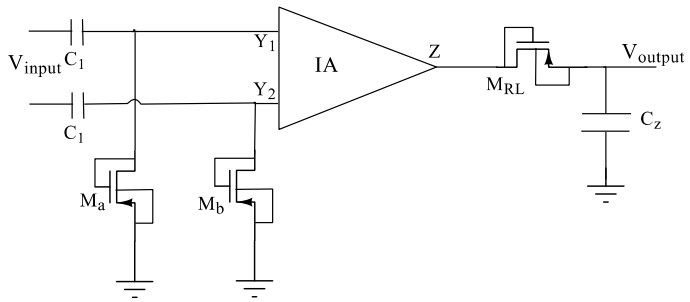


Figure 8. The schematic of the proposed configuration for separating the required frequency bands for various biomedical signals through the IA.

Furthermore, note that typically biomedical signals have very small amplitude and are at relatively low frequencies. For instance, the amplitude of an EEG signal is normally below 100 µV when measured on the scalp, and about 1–2 mV when measured on the surface of the brain. The frequency band of these signals is from under 1 Hz to about 50 Hz, as demonstrated in Figure 9. Similarly, the spectrum of an ECG signal is mostly distributed between 0.1 Hz to 160 Hz and its amplitude is typically below 5 mV. Thus, filtering of these signals requires filters with very small low cut-off frequency. As a result, the filter requires a very large capacitor or resistor which is hard to achieve on a limited on-chip area. To address this issue, MOS pseudo resistance with a resistance in the order of tera-ohms is used in the proposed circuit [5,29,35]. Using this technique, drastically reduces the required on-chip area to realize the capacitors and resistors of the filter.

Table 3. Features of the designed CMIA compared to other works.

Parameter	Technology	Power Supply	Gain	BW (−3 dB)	On-Chip Area	Power Dissipation
[11]	0.18 µm CMOS	±0.9 V	25–27.6 dB	100 MHz	NA	1.15 mW
[25]	0.18 µm CMOS	±1.2 V	19 dB for R_L = 8 KΩ	18.1 MHz	NA	383.4 µW
[33]	0.5 µm CMOS	±1.5 V	9–23 dB	20 MHz	NA, Large size, due to use 7 off-chip resistors	3.99 mW
[36]	0.18 µm CMOS	1.8 V	Maximum of 40 dB	2 KHz	0.087 mm^2	39.6 µW
This work	0.18 µm CMOS	±0.9 V	10 dB for R_L = 20 KΩ	450 MHz	460 μm^2	148 µW *

* The power consumption is reduced to about 39 µW by decreasing the supply and bias voltages. In this case, the linear dynamic range of the output voltage is restricted to ±0.3 V, and the frequency band of the flat response with a unity voltage gain is reduced to about 38 MHz.

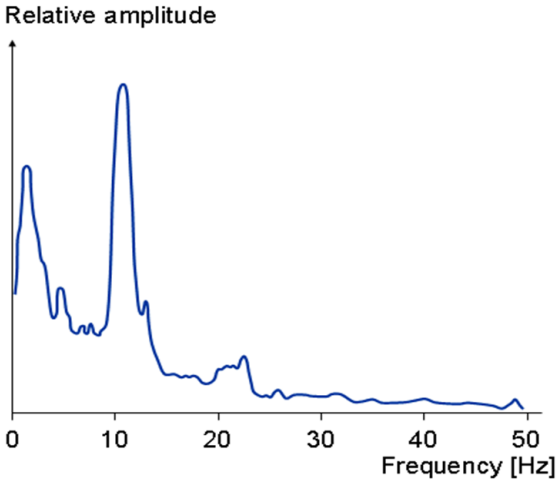


Figure 9. The frequency spectrum of normal EEG.

Equations (1) and (2) are used to estimate the cut-off frequencies, f_L and f_H of the circuit. The resistance Rinc produced by the MOS-pseudo resistors (Ma, Mb, and MRL) is about tera-ohm. Thus, very small C_1 and C_Z are required to achieve the small cut-off frequencies f_L and f_H, respectively.

$$\omega_L = 2\pi f_L = \frac{1}{R_{inc-a,b}.C_1} \quad (1)$$

$$\omega_H = 2\pi f_H = \frac{1}{R_{inc-RL}.C_Z} \quad (2)$$

3. Results

In order to validate the proposed filtering instrumental amplifier, two versions of the proposed circuit, one for filtering EEG signals and one for filtering ECG signals, are designed. Considering the typical frequency band of EEG signals (shown in Figure 9), the first circuit was designed to pass the frequency band of 0.2–30 Hz with a voltage gain of about 24.3 dB. To achieve this frequency band, the values of capacitors C_1 and C_z are set to 1 pF and 1.5 pF, respectively, and W/L sizing of the MOS pseudo resistors M_a, M_b, and M_{RL} are set to $\frac{0.5\ \mu m}{5\ \mu m}$ and $\frac{15\ \mu m}{0.5\ \mu m}$, respectively. The frequency response of the designed band-pass IA is shown in Figure 10A. An input EEG test signal, which was recorded at the Neuro-Technology Lab in the Biomedical Engineering Department, the University of Isfahan, during the eyes-closed condition, followed by the eyes-open resting condition, was used to validate the designed circuit.

The original EEG input signal (Vinput in Figure 8), is depicted in Figure 10B. This EEG signal was recorded at a resting-state under the eyes-open condition for about the first 30 s and then from second 30 up to second 60, it is recorded at the eyes-closed resting condition. The DC offset and baseline drift artifacts caused by the electrodes are removed at the inputs of the instrumentation amplifier at points Y_1 and Y_2. After removing the DC component, the signal is filtered and amplified in the desired frequency band and then appears at the Voutput.

The filtered and amplified output signal is shown in Figure 10C. It can be seen that the sample EEG input signal is a low-quality noisy signal with a DC level and drift. The results show that the proposed circuit proves its proper performance by eliminating the undesired artifact and DC component of the EEG input signal. Figure 10D shows the PSD (power spectral density) plots for the EEG signals under eyes-open and eyes-closed conditions. As we already know, the Alpha waves are reduced with open eyes, drowsiness, and sleep. The obtained results shown in the PSD plots confirm the proper work of the proposed circuit, showing the expected substantial difference in the Alpha rhythm of the EEG wave when the eyes are open compared to the eyes-closed condition.

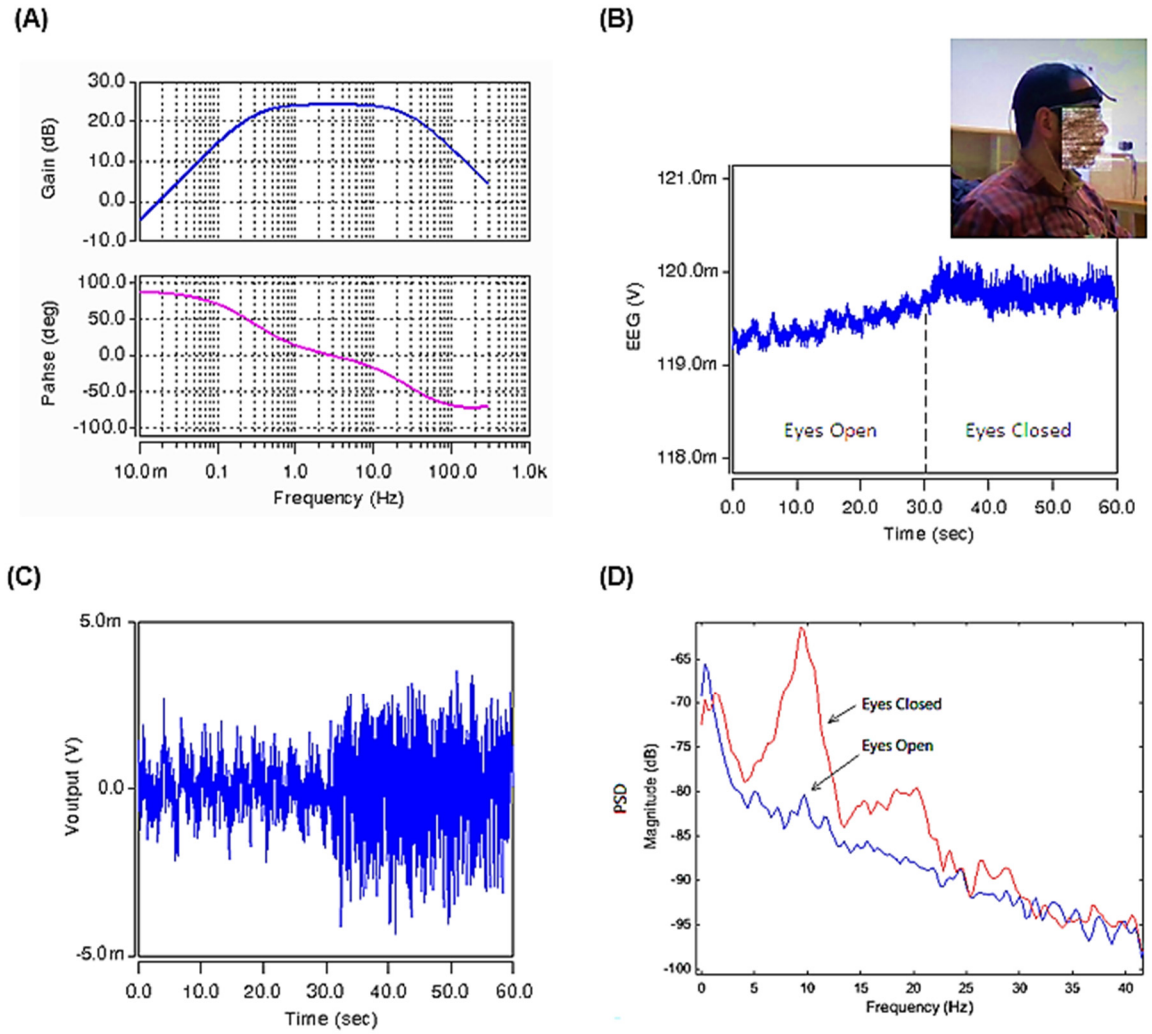


Figure 10. (**A**) The frequency response of the gain and phase of the band-pass bioamplifier. (**B**) The original EEG input signal (Vinput). (**C**) The EEG output signal after amplification and filtering using the designed circuit of Figure 8. (**D**) Power spectral density plots under eyes-open and eyes-closed conditions for the EEG recordings.

The circuit is then redesigned by changing capacitor C_z to 0.25 pF and the W/L ratio of Ma and Mb to $\frac{0.5\ \mu m}{10\ \mu m}$, to pass the frequency band of 0.13–160 Hz (Figure 11A) for ECG applications. Again, an ECG sample input, recorded at the Biomedical Instrumentation Lab in the Biomedical Engineering Department, the University of Isfahan, was applied and the output signal is shown in Figure 11B. Again, the quality of the output ECG signal proves the performance of the redesigned circuit for ECG recordings.

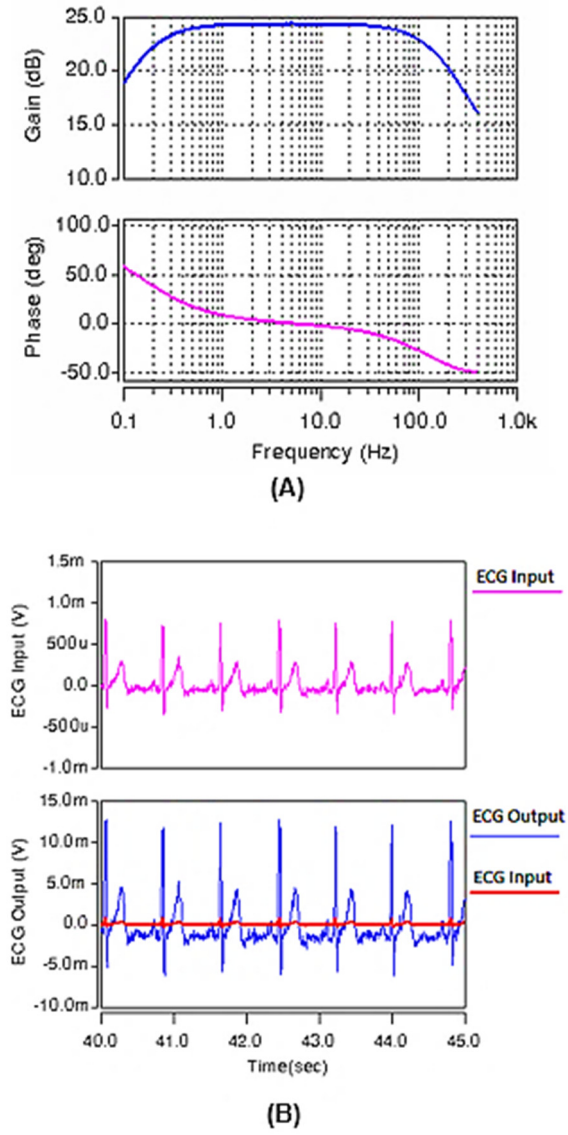


Figure 11. (**A**) The frequency response of the gain and phase of the band-pass amplifier for ECG recording. (**B**) The ECG input and its related output signal after amplification and filtering using the designed circuit of Figure 8.

In order to investigate the distortion level of the proposed band-pass instrumentation amplifier, THD (total harmonic distortion) analysis was conducted. The analysis shows a THD of about 0.97% for a sinusoid input signal with an amplitude of 0.8 $mV_{p\text{-}p}$ and a frequency of 10 Hz. It is worth mentioning that this THD is small enough, and the existence of this level of distortion in a large amplitude of an ECG signal is not an issue for the diagnoses of cardiac arrhythmia and other illnesses.

4. Conclusions

In this paper, a wide range CMOS DVCC based on a wide linear range transconductor has been presented. The proposed DVCC has a wide dynamic range of ±400 mV and ±0.85 mA. Its voltage frequency response has a flat unity voltage gain (V_x/V_{id}) of 80 MHz. The power consumption of 148 μW was measured by a post layout simulation. The layout of the DVCC circuit occupies a total area of 0.378 μm^2. In the following, using the presented DVCC, an instrumentation amplifier has been implemented and a new configuration has been presented to realize a band-pass amplifier using IA. In order to validate the proposed band-pass amplifier, two versions of the circuit with different specifications have been designed and recorded EEG and ECG signals have been successfully amplified and filtered. The proposed current-mode band-pass instrumentation amplifiers have applications in improving the quality of various biomedical signals for clinical diagnosis, including electrocardiography and electroencephalography.

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