electronics

MDPI

Review

Review of Ka Band Power Amplifier

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Abstract: With the increase in the demand for high-speed transmission communication, satellite communication is developing rapidly. Because of the bandwidth capacity, the K/Ka band is considered the mainstream frequency band of satellite communication. The performance of a power amplifier (PA) directly affects the power of the transmitter, so the application of a power amplifier in Ka band satellite communication is very important. A review of the state-of-the-art PA in the Ka band is presented in this article. The structure of the PA introduced includes common source, cascode, stacked field-effect transistor (FET), power combining, and Doherty PA, highlighting the advantages and disadvantages. The main solid-state technologies are outlined, including Si, SiGe, GaAs, and GaN, emphasizing Si complementary metal–oxide–semiconductor (CMOS) due to low price and high integration.

Keywords: power amplifier; Ka band; satellite communication

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1. Introduction

Satellite communication has the characteristics of wide coverage, large capacity, and long communication distance, and is not limited by the geographical environment. It is widely applied in broadband multimedia communications, personal mobile communications, military communication, and other fields. In the long-term development process, satellite communication and mobile communication form complementary relationships, playing an irreplaceable role [1].

At present, the frequency bands used in satellite communication mainly include the L band, S band, C band, Ku band, and Ka band. In the past decade, with the continuous development of the satellite application field, spectrum congestion has occurred in the conventional frequency bands L band, S band, and C band allocated by satellite services [2]. Limited by bandwidth, the communication rate of these satellites is becoming more and more difficult to meet the needs of information society for high-speed data transmission. In this case, Ka band broadband communication satellite technology has entered the field of vision of various countries and become the research goal of various countries because of the wide available frequency band (26.5 GHz~40 GHz) and few interference signals.

In 1997, the U.S. Federal Communications Commission (FCC) issued Ka band satellite communication licenses to more than a dozen companies to promote the development of Ka band satellite communication technology. These high-tech companies include Motorola's Celestri system, Lockheed Martin's Astrolink system, GE Americom's Ge star system, and others [3]. After years of development, the Ka band broadband multimedia communication satellite in the United States has been put into commercial use, which can provide high-speed broadband Internet access services for rural families in remote areas and airliners.

Because the rain attenuation of the Ka band is greater than that of the Ku band, the requirements for devices and processes are higher, and satellite communication in the Ka

band developed slowly in the past [4]. With the improvement in the hardware manufacturing level, Ka band microwave circuits have developed rapidly over the past 10 years.

In October 2011, the full Ka band communication satellite ViaSat-1 of VIASAT was successfully launched [5]. The total communication capacity of ViaSat-1 exceeds 140 Gbps, which is more than 70 times that of any Ku-band satellite at that time [6]. In particular, with the launch of the new generation satellite ViaSat-1, the concept of the high price and narrow bandwidth of traditional satellites has been changed. The transmission speed provided by the satellite is higher than that of terrestrial digital subscriber line DSL and wired cable, but the service price of users is almost the same [7]. In 2012, ViaSat-1 was officially put into commercial use, opening a new era of Ka band satellite communication [8].

In addition to the field of satellite communication, the next generation mobile communication technology 5G is also likely to use the communication technology of the Ka band. Regarding 5G, the Third-Generation Partnership Project (3GPP) determined the millimeter-wave band 26 GHz/28 GHz/39 GHz as the 5G band to be deployed first in the world [9].

In recent years, many high-tech companies in the United States and South Korea have successively completed the verification test of the 5G communication prototype based on a 28 GHz band [10]. Whether for 5G or broadband communication satellites in the future, Ka band applications can provide high-speed communication services. With the maturity and promotion of these technologies, there will be a lot of demand for Ka band communication systems in the future.

As an important part of the transmitter in the communication system, the performance of the power amplifier plays a decisive role in the performance of the whole system. Figure 1 is a block diagram of a communication system transmitter. Usually, the power amplifier is located at the end of the transmitter of the whole communication system. After the signal passes through the modulator, mixer, and band-pass filter, it is amplified to a certain power level through the power amplifier and transmitted through the antenna. Among these modules of the communication system, the power amplifier is a core module. Its linearity directly determines the transmission signal quality of the transmitter, its efficiency determines the power consumption of the transceiver, and its output power determines the distance of communication. Therefore, designing a power amplifier with good performance is the key to determine the quality of wireless communication. Therefore, the research of the power amplifier is very important.

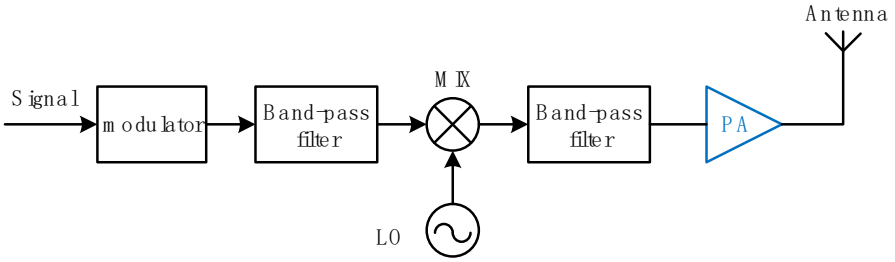


Figure 1. A block diagram of a communication system transmitter.

This article will discuss the mainstream technologies for Ka band PA, focusing on Si complementary metal–oxide–semiconductor (CMOS) because of its low cost and high integration. The structure of the state-of-the-art PA is presented, including common source, cascode, stacked FET, power combining, and Doherty PA, highlighting the advantages, disadvantages and a comparison with them.

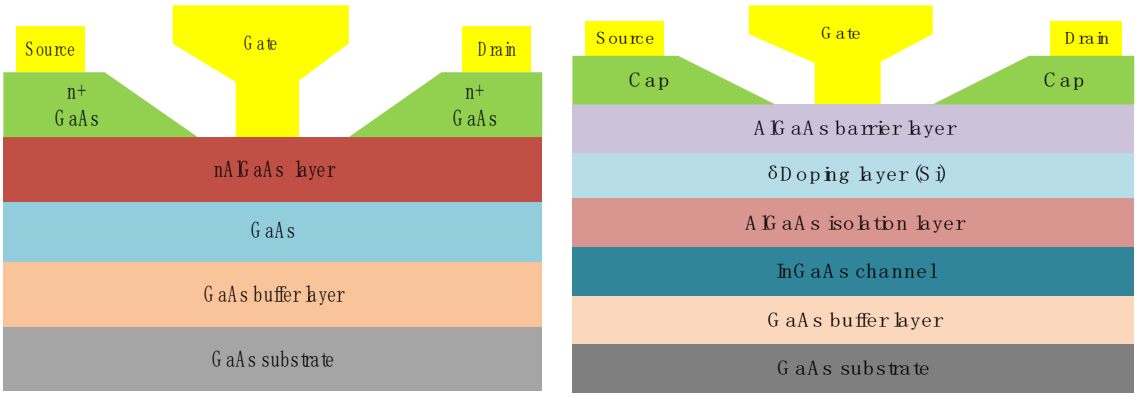
The whole paper is arranged as follows: Section 2 briefly introduces the technology which can be used in Ka band power amplifiers. Section 3 describes the topologies of the

common PA and summarizes its advantages and limitations. Finally, Section 4 summarizes the conclusion of this paper.

2. Technology

There are several semiconductor processes that have been demonstrated for power amplifiers at the Ka band. They are gallium arsenide pseudomorphic high electron mobility transistors (GaAs pHEMT) [11], gallium nitride high electron mobility transistors (GaN HEMT) [12], indium phosphide heterojunction bipolar transistor (InP HBT) [13], silicon complementary metal–oxide–semiconductor (Si CMOS) [14], silicon and germanium bipolar complementary metal–oxide–semiconductor (SiGe BiCMOS) [15] and silicon on insulator complementary metal–oxide–semiconductor (SOI CMOS) [16].

In the late 1970s and early 1980s, the HEMT structure was proposed and developed [17,18]. During this period, a number of research groups around the world proposed the AlGaAs/GaAs crystal structure, collectively known as HEMT. The traditional GaAs HEMT structure profile is shown in Figure 2a [19].



(**a**) (**b**)

Figure 2. (**a**)Traditional GaAs HEMT structure profile, (**b**) GaAs pHEMT structure.

However, there exists a deep donor state trap DX center in the AlGaAs/GaAs heterojunction, which causes device degradation at low temperatures [20]. To solve this problem, pHEMT was invented.

In 1986, A. Ketterson first fabricated the AlGaAs/InGaAs/GaAs pHEMT structure on a GaAs substrate [21]. The GaAs pHEMT structure is shown in Figure 2b.

GaAs pHEMT solves the above problems by introducing the AlGaAs isolation layer, which is used to isolate the two-dimensional electron gas (2DEG) layer and doping layer [22]. Compared to HEMT devices, pHEMT greatly improves electronic transport characteristics. The electron mobility velocity of GaAs is 5 or 6 times that of Si and has higher drift velocity and better high frequency characteristics [23]. In recent years, pHEMT's cut-off frequency f_T and maximum frequency f_{MAX} reached 360 GHz and 400 GHz, and they are widely used in millimeter-wave frequencies [24]. However, GaAs has high thermal resistance and low breakdown voltage, which limits its application in high voltage and high power. In 2018, Aviv Barabi presented a PA targeting more than 25 dB gain and 27.3 dBm output power between 96 and 98 GHz adopting 0.1 µm GaAs pHEMT [25]. In 2020, Ref. [26] proposed a 3-stage CS PA in 65 nm CMOS, achieving 13.4 dBm saturated output power (P_{sat}) with peak PAE of 11.3% in the 85–101 GHz range. Compared with CMOS process, the GaAs process has the advantage of high output power at higher frequency.

GaN HEMT and GaAs pHEMT devices operate on a similar principle and are both high electron mobility transistors operating through 2DEG [27]. However, due to GaN's

special spontaneous polarization, GaN HEMT can also produce 2DEG without doping. The profile of GaN HEMT is shown in Figure 3a.

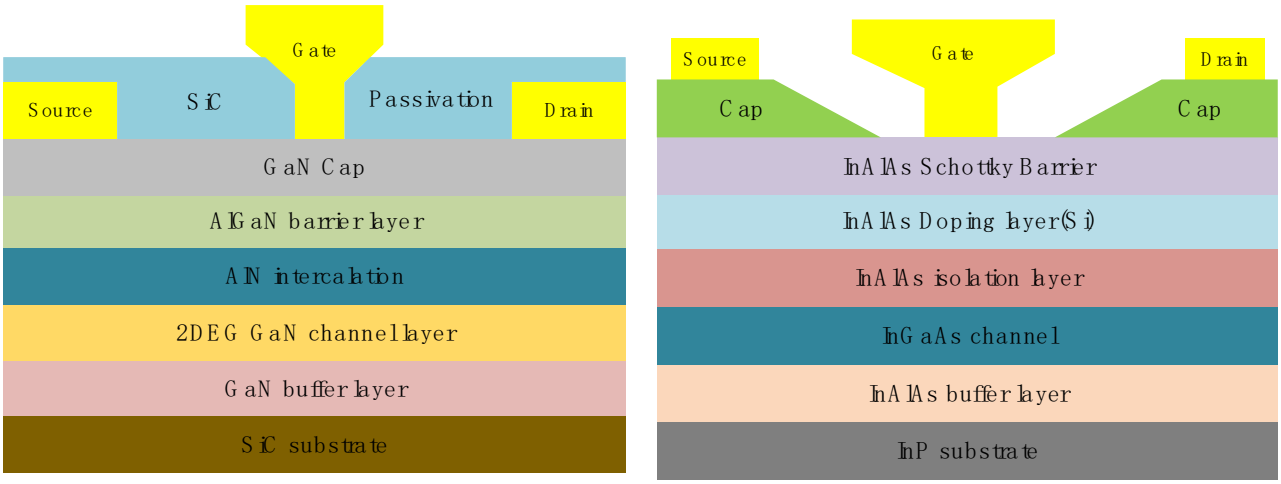


Figure 3. (**a**) GaN HEMT structure profile, (**b**) InP HEMT structure profile.

GaN and GaAs have similar frequency characteristics, but due to the special spontaneous polarization of GaN, the concentration of 2DEG is one order of magnitude higher than that of GaAs [28]. Therefore, GaN has high current density and outputs high power at high frequency. In 2018, M. Roberg presented a GaN MMIC PAs using Qorvo's QGaN15 released process. The output power of the reported PA is approximately 46.2 dBm at 27.5–29.5 GHz [29]. The substrate selection of GaN is a key problem. GaN devices grown on a SiC substrate can obtain higher performance, but the cost is very high. Therefore, several research groups regard GaN on the Si substrate as a feasible solution for the large-scale market application, and massive commercial products have been designed and manufactured. However, compared with the SiC substrate, the Si substrate has worse electrical and thermal properties [30]. The cost and performance must be considered comprehensively to select a more appropriate scheme. In a word, the GaN process can bring some advantages of III-V technology (III-V compound semiconductor technologies include GaAs, GaN, InP, etc.) and its price is lower than the GaAs technology due to the possibility of integration on the Si substrate.

In the research of high frequency electronic devices, the transistors using InP materials are adopted in HEMT and HBT technology. The InP HEMT device is a vertical device, which has better noise characteristics than the InP HBT device. It is often used to design low-noise amplifiers. Its profile is shown in Figure 3b.The InP HBT device is a transverse device. Compared with InP HEMT, its breakdown voltage is higher, and its power capacity is larger. It is often used to design power amplifiers.

InP HBT is mainly divided into a single heterojunction bipolar transistor (SHBT) and a double heterojunction bipolar transistor (DHBT). On the one hand, the band gap of the InP DHBT collector material is greater than that of the InP SHBT collector material, so its collector has higher voltage resistance, and it is conducive to high power output; on the other hand, the collector material of InP DHBT has high thermal conductivity, so it has better heat dissipation performance and is more suitable for high-current and high-power circuit design.

InP-based technology is the only technology that can provide PAs with >20 dbm output power over 200 GHz [31,32]. DHBT 500 nm and 250 nm technology nodes provide about 330 GHz and 400 GHz f_T respectively, and the latter's f_{MAX} is up to 700 Ghz. Compared with traditional CMOS FET, the InP DHBT process has the advantages of large

breakdown voltage, small parasitic capacitance and low substrate loss. The main limitation of InP is its cost because it is difficult to purchase and is a very fragile material, which makes its manufacturing and handling extremely dangerous.

With the increase in the operating frequency of PAs, the CMOS process node decreases to several nanometers or tens of nanometers [33]. The reduction in the MOS transistor size will reduce the breakdown voltage threshold of the gate oxide layer, and the power supply voltage will also decrease with the increase in the process nodes. Silicon has low electron mobility and poor high frequency characteristics, which limits the application of silicon technology in the higher frequency band. The lower breakdown voltage also limits the output power of the power amplifier.

However, due to the extremely rich content of silicon in nature, it is easy to purify and grow a single product. The cost of silicon technology is much lower than that of III-V technologies (when mass produced). In addition, the integration of silicon technology is very high, and multi-layer metal layers can make very complex circuits. In 2021, J. Park proposed a 2-stage cascode PA in 60 nm CMOS. The PA achieved 17.1 dBm output power and the PAE remained above 38.2% in the area of 0.16 mm² [34]. When the performance requirements are not too strict, the silicon process can be realized in a small area, and the cost is very low. Therefore, silicon technology is one of the important processes for making the Ka band power amplifier.

With decades of development, bulk silicon CMOS technology has become more and more mature. However, with the continuous reduction in device feature size, many new problems still appear, such as the short channel effect. SOI (silicon on insulator) technology refers to the process of forming a layer of semiconductor monocrystalline silicon thin film material on the insulating material layer, and then manufacturing integrated circuits on monocrystalline silicon. The main difference between the traditional bulk CMOS process and SOI technology is that SOI CMOS have a buried oxide layer, which separates the device from the substrate [35]. Its profile is shown in Figure 4. In SOI CMOS, each device is surrounded by an oxide layer, which is completely isolated from the surrounding devices and fundamentally eliminates the latch-up effect [36]. At the same time, the buried oxygen layer also increases the thickness of the insulating layer between the interconnect and the substrate, which greatly reduces the parasitic capacitance of the interconnect [37]. Reducing the capacitance is helpful to improve the speed of the circuit and reduce the power consumption of the circuit. IBM 45 nm CMOS SOI technology has been widely used in the development of millimeter-wave power amplifiers [38–40]. It provides SOI CMOS transistors with very high f_T and f_{MAX} (>400 GHz) [41]. The excellent performance of SOI MOSFET makes the SOI CMOS circuit more suitable for working in harsh environments, such as aerospace and high temperature.

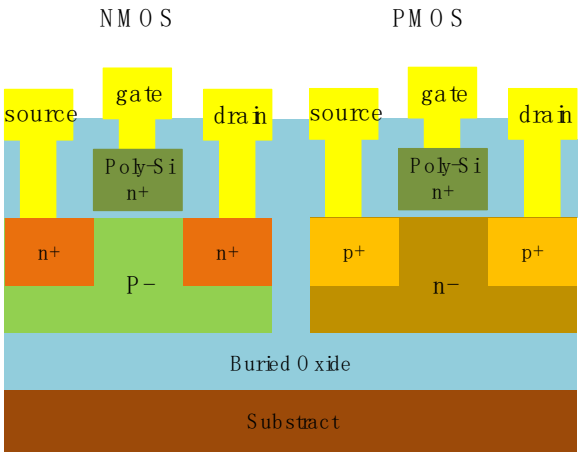


Figure 4. SOI CMOS structure profile.

However, SOI CMOS process technology cannot replace bulk silicon CMOS technology, mainly because the SOI CMOS process is not as mature as the bulk silicon CMOS process. The quality of the silicon film of SOI material is not as good as that of bulk silicon material. In addition, the cost of SOI CMOS is higher than that of bulk silicon CMOS.

The development of SiGe devices is mainly promoted by IBM and other companies. The BiCMOS process is adopted, which can be used as an alternative to CMOS. BiCMOS technology is a new technology that integrates bipolar transistor (BJT) and field-effect transistors (FET) on the same chip. Compared with CMOS, under the same scale, the performance and cut-off frequency of the SiGe device are greatly improved, and it is better than the silicon-based CMOS device in withstanding voltage and the current processing ability, so it is also suitable for medium power applications. As shown in Figure 5, SiGe BiCMOS combines SiGe HBT applied to the RF circuit and SiGe CMOS applied to digital circuit, combining the digital and analog on one chip. Compared with traditional Si BiCMOS, SiGe BiCMOS is more conducive to integration. In the past 10 years, SiGe BiCMOS technology has been greatly developed, breaking through the technical barriers of 0.35, 0.18 and 0.13 um. The cut-off frequency f_T of SiGe HBT has reached 40~350 GHz, and the maximum operating frequency can almost reach the level of GaAs [42]. It has strong competitiveness and wide application prospects in the RF field.

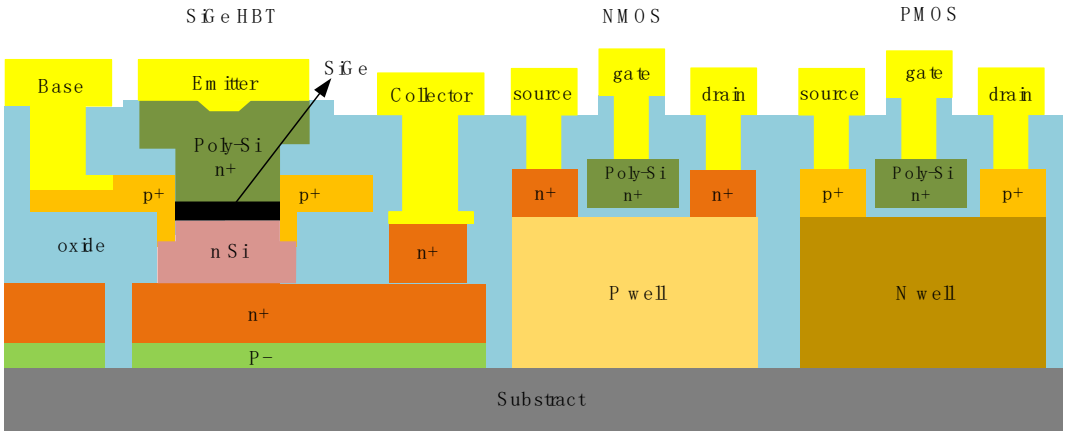


Figure 5. SiGe BiCMOS structure profile.

In the author's opinion, GaN and GaAs materials have power advantages for chips with an operating frequency not higher than 100 GHz. If frequency is the primary consideration of the device, the frequency of the power amplifier made of the InP device can be higher than 500 GHz. Of course, for industrial manufacturing, the product cost is also an important factor in the power amplifier design and mass production. Especially for consumer electronics, CMOS is conducive to system-on-chip integration, so it has a cost advantage. In addition, the loss of performance or quality factors of passive components are quite competitive [43].

3. Topologies

3.1. Common Source

Common source (CS) is one of the three basic configuration circuits of the field-effect tube amplifier. The input and output circuits of the common source circuit contain the MOS tube source; the input signal is input from the gate, and the output signal is output from the drain. A typical basic CS amplifier is shown in Figure 6. In the practical design and application of the common source amplifier, multistage circuit is usually used to obtain high gain [44].

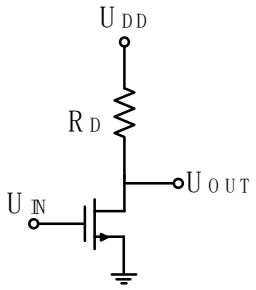
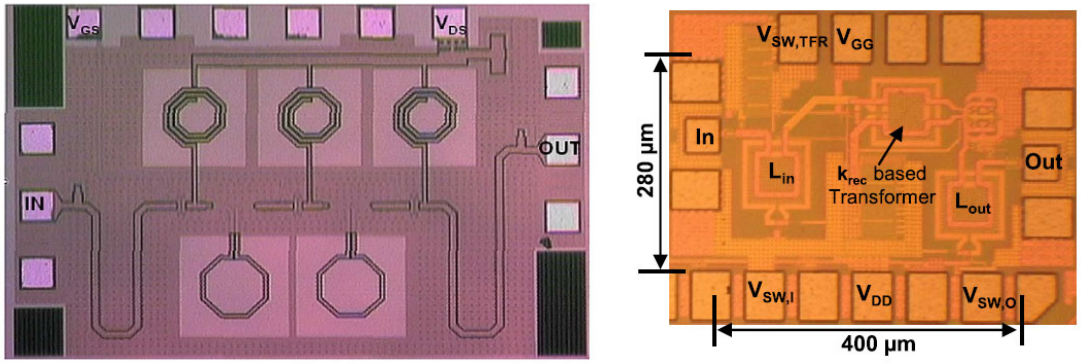


Figure 6. CS amplifier circuit schematic diagram.

In 2008, J. Lee et al. proposed to use 180 nm CMOS design to produce 3-stage CS PA [45]. In order to reduce the loss of a conductive silicon substrate, a substrate-shielded microstrip line is used as the matching network in the amplifier (see Figure 7a). The three-stage amplifier achieved a record gain of 14.5 dB for the Ka band power amplifier using CS transistors, with a corresponding efficiency of 13.2% and output power of 14 dBm.



(**a**) (**b**)

Figure 7. (**a**) Three-stage CS amplifier in 180 nm CMOS [45]. (**b**) One-stage CS amplifier in 60 nm CMOS [46].

In [46], S. N. Ali et al., on the basis of the one-stage CS circuit, proposed a frequency reconstruction matching network and reconfigurable coupling-coefficient-based transformer (see Figure 7b). These technologies make efficient PA possible in 60 nm CMOS, which is working at 24 GHz and 28 GHz with better than 40% power added efficiency (PAE). However, only a one-stage CS amplifier is used, resulting in a relatively low gain of less than 9.1 dB at 24 and 28 GHz, and P_{sat} of 14.7 dBm at 24 GHz.

In 2021, work [47] proposed a 3-stage CS PA in 90 nm CMOS, achieving high gain and good back-off PAE at 28 GHz. Y. T. Chang et al. presented three techniques to improve 1 dB compression point output power (P_{1dB}) efficiency at low-, medium- and high-power regions, respectively. The three techniques are adaptive bias network (ABN), predistortion linearizer (LIN) and g_m compensation technique (the cross-couple pair for the g_m compensation technique). These techniques have an obvious effect, the efficiency of P_{1dB} approaches the efficiency of P_{sat}. The measured P_{1dB} and P_{sat} are 16.73 and 17.68 dBm at 28 GHz, and gain is 28 dB.

A summary comparison with CS PA measurements is given in Table 1.

Table 1. Comparison of the measurement results with the CS PA.

Ref.	Tech	Frequency (GHz)	Gain (dB)	P_{sat} (dBm)	P_{1dB} (dBm)	PAE_{peak} (%)	Area (mm^2)	Topology
[45]	180 nm CMOS	24	14.5	14	/	13.2	0.84	3-stage CS
[46]	65 nm CMOS	24/28	9.1/8.1	14.7/14.4	13.9/13.6	42.6/40.1	0.11	1-stage CS
[47]	90 nm CMOS	28	21.3	17.7	16.7	23.6	0.49	3-stage CS

As can be seen from Table 1, the area of CS PA in CMOS is small. Among them, Ref. [46] achieved high PAE and gain with an area of 0.11 mm^2. However, silicon-based PAs have narrow bandwidth and lower efficiency at the Ka band.

3.2. Cascode

The cascode structure is the most widely used circuit structure in amplifier circuit design, and it is an improvement of the common base amplifier circuit. Its simple circuit schematic diagram is shown in Figure 8.

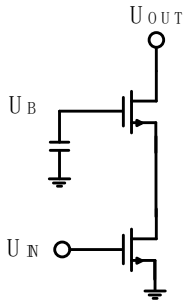


Figure 8. Cascode amplifier circuit schematic diagram.

The most important characteristic of the cascode structure is that it greatly increases the input impedance on the basis of maintaining the excellent frequency characteristics of the common base amplifier circuit, which is very effective for improving the small signal gain. In addition, the application of the cascode structure in PA design can increase the maximum output voltage by about 1.5 times, effectively reduce the requirements of the amplification stage for the maximum output current, reduce the size of the transistor, and improve the output efficiency. Compared with the common source structure, the input and output ports of the cascode power amplifier structure have a better isolation effect and better stability.

In 2004, A. Komijani and A. Hajimiri presented a fully integrated 2-stage cascode power amplifier in 180 nm CMOS [48]. A shielded-substrate coplanar waveguide structure was designed in the amplifier to reduce the substrate-induced losses. Experimental results for the power amplifier demonstrate up to 14.5 dBm output power and gain of 7 dB at 24 GHz.

In Ref. [49], a high linearity PA with ultra-wide video bandwidth for 5G wireless communication was proposed. With the increase in operating frequency, the output power, efficiency and linearity of PAs decrease sharply because of the sideband asymmetry of PAs caused by the memory effect [50]. Since third-order intermodulation distortion (IMD3) is generated by the mixing of fundamental wave and envelope nonlinear term, when the impedance at the envelope frequency is not zero, there is a large IMD3 on one side of the signal, resulting in an asymmetric IMD3 sideband [51]. To suppress the memory effect, an efficient low drop out (LDO) regulator is proposed. The fast load regulating LDO guarantees that the output impedance at the envelope frequency is less than 5 Ω in the frequency range up to 1 GHz. The output impedance is low enough to eliminate the envelope voltage component and suppress the memory effect. The 3-stage

CS cascode PA in 65 nm CMOS achieved the gain of 22 dB, P_{sat} of 14 dBm, the linear output power is 9.5 dBm with the IMD3 of -30 dBc and peak PAE of 21.8% at 28 GHz. The presented PA and LDO are shown in Figure 9a. The core area of PA is 0.19 mm² and LDO is 0.34 mm².

In order to improve the efficiency of PAs, a dual-mode switched capacitor PA was reported [52]. The PA can operate in both high- and low-power modes by controlling the switching capacitance to modulate the output impedance. The measured results demonstrate 25.8% peak PAE at 19.9 dBm P_{sat} in high-power mode and 22.8% peak PAE at 17 dBm P_{sat} in low-power mode.

In addition to the memory effect, the nonlinear capacitance gate-to-drain capacitances (C_{GD}) and drain-to-source capacitances (C_{DS}) of power transistors is also one of the reasons for the poor linearity of RF CMOS PA [53]. For further improving linearity, G. Cho et al. proposed a simple but effective resistive body network, reducing the gate capacitance changes of the power transistor [54] (see Figure 9b). As a result, the presented PA, composed of 2-stage differential cascode, achieves linearity PAE of 25% at output power of 20.25 dBm at 28 GHz. Compared with the LDO proposed in [49], the body network is so simple that it is suitable for most millimeter-wave amplifiers.

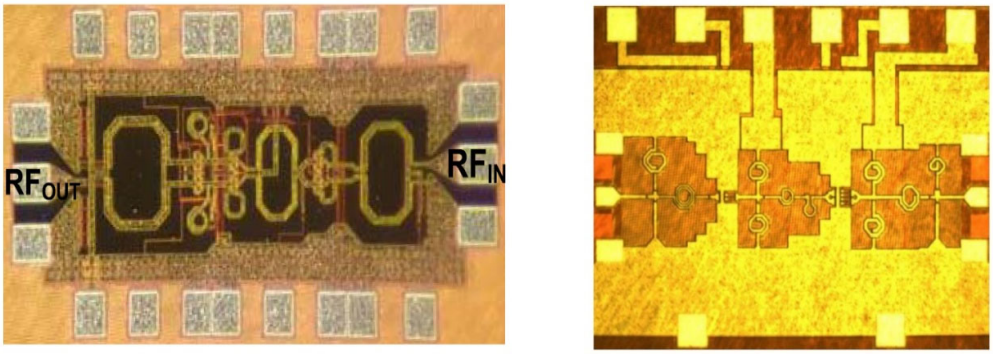
(**a**) (**b**)

Figure 9. (**a**) **The** 3-stage CS cascode PA in 65 nm CMOS and LDO [49], (**b**) 2-stage differential cascode PA in 40 nm CMOS [54].

A Class AB cascode PA in 130 nm SiGe with noninverting transformer for mobile satellite communication (SATCOM) was reported [55]. The 1-stage cascode power amplifier achieved P_{1dB} of 12 dBm, P_{sat} of 14 dBm and peak PAE of 25% at 28 GHz.

In the latest study, J. Park proposed a cold-FET-based interstage matching network to improve the linearity and efficiency, which is designed in 60 nm CMOS (see Figure 10a) [34]. This matching network improves the linearity of the 2-stage cascode PA by providing the PA gain-expansion and phase-lag characteristics. The PA achieved 17.1 dBm output power and the PAE remained above 38.2%.

Since the beginning of the 21st century, the demand of PA covering multi-frequency band has been growing faster and faster [56]. C. Huynh proposed a concurrent dual-band PA in 180 nm SiGe BiCMOS with a new synthetic matching network technique (see Figure 10b) [57]. The technique works by combining two separate single-band matching networks into a single network, so the PA can work in single-band mode (25.5 or 37 GHz), as well as concurrent dual-band mode (25.5 and 37 GHz). The PA, composed of 2-stage common-emitter (CE) cascode, achieves peak PAE of 7.1% and more than 17 dB gain at dual-band mode.



(**a**) (**b**)

Figure 10. (**a**) The 2-stage cascode PA in 60 nm CMOS [34] (**b**) 2-stage CE cascode PA in 180 nm SiGe BiCMOS [57].

A summary comparison with cascode PA measurements is given in Table 2.

Table 2. Comparison of the measurement results with the coscode PA.

Ref.	Tech	Frequency (GHz)	Gain (dB)	P_{sat} (dBm)	P_{1dB} (dBm)	PAE_{peak} (%)	Area (mm^2)	Topology
[48]	180 nm CMOS	24	7	14.5	/	/	1.26	2-stage cascode
[49]	65 nm CMOS	28	22	14	/	21.8	0.53	3-stage CS cascode
[52]	65 nm CMOS	34	13.8/10.5	19.9/17	17/14	25.8/22.8	0.365	2-stage cascode
[54]	40 nm CMOS	28	20.1	20.3	18.3	25	0.214	2-stage Differential cascode
[55]	130 nm SiGe	28	/	14	12	25	0.14	1-stage cascode
[34]	65 nmCMOS	31	18.9	20.3	/	38.2	0.345	2-stage cascode
[57]	180 nm SiGe BiCMOS	25.5/37	20.5	14.6	13.1	35.8	0.3	2-stage CE cascode

The breakdown voltage of the power amplifier in the CMOS process is low, but the cascode structure can greatly improve the power supply voltage and reduce the device sizes. As can be seen from Table 2, all chips have high integration and small area. However, the cascode structure also introduces large parasitic capacitors, resulting in low gain and efficiency compared with other structures.

3.3. Stacked FET

In the traditional power amplifier design, the output matching network needs to convert 50 Ω to the optimal load impedance of the output transistor to obtain the maximum output power. According to engineering experience, for a lossy matching network, generally speaking, the greater the impedance transformation ratio, the greater the insertion loss of the matching network, and the more difficult it is to realize broadband impedance matching. Therefore, improving the optimal load impedance helps to reduce the loss of the output matching network, improve the output power and efficiency, and it is easier to achieve broadband output matching. Stacked power amplifiers can meet this demand.

In the traditional stacked FET structure, the source stage and drain of multiple transistors are connected sequentially. Figure 11 shows an n-layer stacked-FET structure. By adjusting the gate input and bias voltage of the transistor, ideally, the bias voltage between the drain stage and the source stage of each transistor can be the same. The external gate grounding capacitance makes the voltage between the drain stage and the source stage of each transistor the maximum voltage swing of the transistor. Each transistor is directly coupled, the total swing of the output voltage is n times that of the single-tube structure, and the output power is n times that of the single-tube structure. In addition, another advantage is that the optimal load impedance is also n times that of the single-tube structure, which provides the basis for broadband performance and low matching loss [58]. As described above, transistor stacking is a promising method to improve the output power and bandwidth of PAs in modern semiconductor technology, because although the breakdown voltage is low, it is still possible to obtain a high output voltage swing.

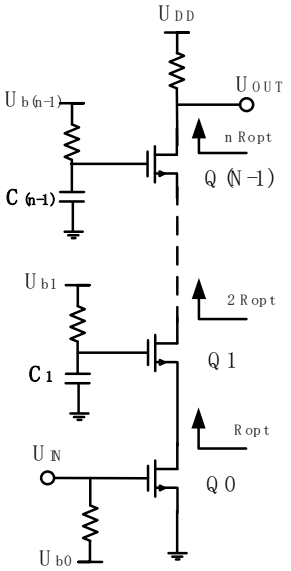
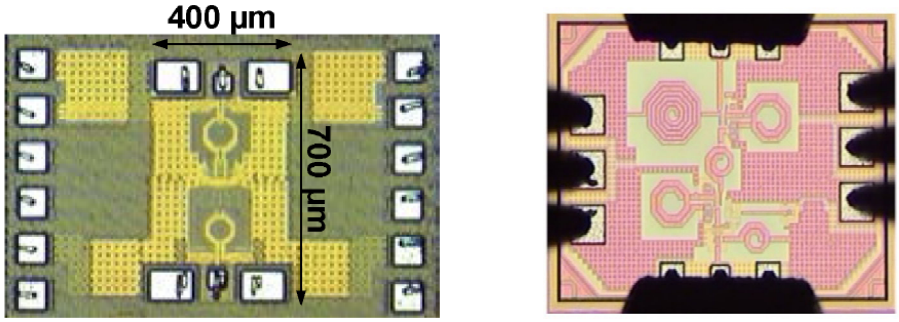


Figure 11. The n-layer stacked-FET amplifier circuit schematic diagram.

However, due to the process error and load impedance design problems, the phase and amplitude of the output voltage of each layer of the transistor will have a certain deviation, which will affect the power synthesis efficiency and linearity of the stacked-FET amplifier.

In [59], B. Park designed the 1-stage differential CS and 1-stage 2-stack PA in the same area (0.28 mm²) (see Figure 12a). Through the comparison of results, the 2-stack PA had higher gain and output power than the differential CS. The differential CS/2-stack achieved a gain of 10/13.6 dB, P_{sat} of 10.1/15.1 dBm and PAE of 36.5/43.5%.

In 2016, an ultra-compact watt-level stacked-FET GaAs PA was reported [60]. The power amplifier has more than 33% PAE and 31.5 dBm output power, with an area of 2 mm².



(**a**) (**b**)

Figure 12. (**a**) 1-Stage 2-stack PA in 28 nm CMOS [59], (**b**) 3-stack PA in 90 nm CMOS [61].

In 2017, Y. Lee first proposed a high efficiency high gain 3-stacked PA without an output matching network by selecting appropriate transistor size (see Figure 12b) [61]. Fabricated in 90 nm CMOS process, the PA chip achieves gain of 17.2 dB and with an adaptive bias network.

In 2018, Q. Zhou proposed a stacked cascode broadband PA in 180 nm SiGe BiCMOS [62]. It is known that high-order matching networks can achieve broadband. This paper proposed a broadband PA based on 6 order LC input matching network and interstage neutral capacitance. The PA achieved P_{1dB} of 23.6 dBm and peak PAE of 31.7%. The fractional bandwidth of the PA is 63.3%, covering the whole Ka band (26.5 to 40 GHz).

A fully integrated 3-stage stacked PA with neutralization technique for 5G applications was reported [63]. The neutralization technique keeps the output voltage of each transistor the same. The 3-stage stacked PA targeted 24.8 dBm output power and 17.5 dB gain at 38 GHz, adopting its 65 nm CMOS process.

In 2020, S. M. A. Ali first proposed a 2-stage 2-stacked HBT Class-F^{-1}PA in the 130 nm SiGe BiCMOS [64]. The PA, composed of a Class-F driving stage and a Class-F^{-1} power stage, achieved 30.1% PAE and 22.1 dB gain while maintaining output power higher than 21.2 dBm.

A summary comparison with stacked-FET PA measurements is given in Table 3.

Table 3. Comparison of the measurement results with the stacked-FET PA.

Ref	Tech	Frequency (GHz)	Gain (dB)	P_{sat} (dBm)	P_{1dB} (dBm)	PAE_{peak} (%)	Area (mm^2)	Topology
[59]	28 nm CMOS	28	10/13.6	10.1/15.1	14/18.6	36.5/43.3	0.28#	1-Stage CS differential /2-stage stacked
[60]	150 nm GaAs	26–31	16.7	31.5	/	33	2.08	3-stage stacked
[61]	90 nm CMOS	32	17.2	17.6	13.2	25.3	0.3 #	3-stage stacked
[62]	180 nm SiGe BiCMOS	26.5–40	20.1	25.3	23.6	31.7	1.26	cascode stacked
[63]	65 nm CMOS	38	17.5	24.8	21.7	24.3	0.146 #	3-stage stacked
[64]	130 nm SiGe BiCMOS	38	22.1	21.2	17.5	30.1	0.75 *	2-stage Class-F^{-1} stacked

Core area. * Without pad.

Stacked-FET amplifiers connect transistors in series so that the output power of the power amplifier is high and has a compact area. As we can see from Table 3, the maximum area of the stacked-FET amplifier is 2.08 mm^2, using the GaAs process. Because the Si

process has a higher degree of integration, the minimum core area of CMOS is only 0.146 mm² in the case of 3-stacked structures. The PAE of all the chips mentioned above basically exceeded 25%, with the highest reaching 43.4%, and the highest output power of GaAs and SiGe reached 31.5 and 25.3 dBm.

3.4. Power Combining

For some occasions requiring high power, such as space communication and base stations, the power amplifier of single power cell is often unable to meet the demand, so it is necessary to adopt power synthesis technology [65]. The general power combining topology is shown in Figure 13.

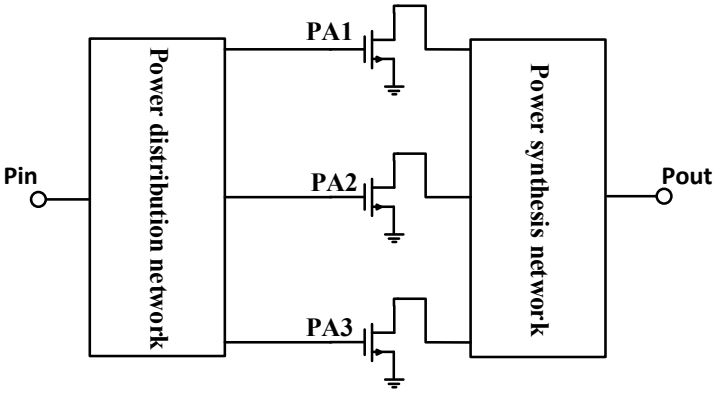


Figure 13. Three-way power amplifier circuit schematic diagram.

The input signal is divided into N signals through the power distribution network, and each path can be equally distributed or non-evenly divided. The power distribution network can be a binary cascade network (binary power synthesis network) or non-binary power splitter (non-binary power synthesis network). The input signal is amplified by an amplifier and then combined with the output through a power synthesis network.

In the binary power synthesis network, Wilkinson synthesizer [66], 90° orthogonal branch line [67] and rat-race hybrid ring [68] can be used as power synthesizers. In the non-binary power synthesis network, microstrip lines [69], coaxial lines [70] and waveguide couplers [71] can be adopted in the power synthesizer. Power combination technology can also be divided into corporate combiner, balanced amplifier and differential amplifier.

3.4.1. Corporate Combiner

Generally speaking, when other external conditions remain unchanged, the output power of microwave power amplifier is directly proportional to the gate width of the transistor or FET. Theoretically, the output power can be increased by adding a single transistor, but this method will cause difficulties in matching and the problem of reducing the cut-off frequency in practical application, because the input and output impedance of the transistor is too low. When a single transistor cannot meet the output power index of microwave power amplifier, the most common method is to use binary arrangement to improve the output power. However, after inserting the power synthesizer, the efficiency and working bandwidth of the amplifier will be reduced. Ref. [72] showed that under the condition of multi-tube synthesis, the PAE of the power amplifier is reduced to about half of that of a single tube.

Corporate combiner is a form of parallel (or current) combining. In general, the corporate combiner is a binary arrangement, which is most common in III-V technology, and also used in Si and SiGe. Generally, the power synthesis technology using binary mode has a wide range of applications and can flexibly select the number of channels to

be synthesized. Therefore, it is the preferred way to realize high power output in commercial chips. The general corporate combiner power amplifier topology is shown in Figure 14.

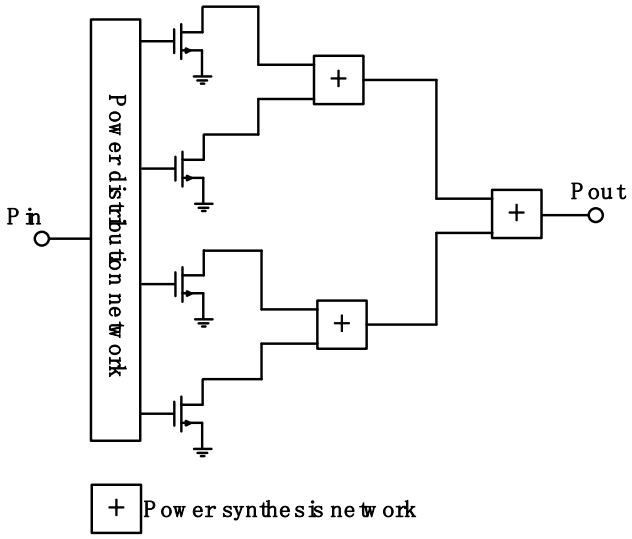


Figure 14. Corporate combiner power amplifier circuit schematic diagram.

In 1986, B. Kim et al. proposed the first monolithic microwave integrated circuit (MMIC) PA on 44 GHz [73]. The output power of 17.8 dBm and the power density of 0.2 W/mm were achieved by using the parallel combination of single-ended transistors with a gain of over 10 dB.

In 2000, K. Matsunaga proposed a power amplifier in 0.35 nm GaAs FETs, consisting of four fully matched parallel MMIC with an output power of more than 30 dBm [74]. The measured results demonstrate that P_{sat} is 34.8 dBm at 28 GHz, which proves that multi-MMIC chip combined technology topology is valid.

In [75], C. F. Campbell presented a 3-stage PA MMIC in 150 nm GaAs pHEMT (see Figure 15). Sixteen parallel 8 × 50 um FET were used for the output stage to improve the thermal properties and performance. The PA achieved 30% PAE and 23 dB gain while maintaining an output power higher than 37.2 dBm.

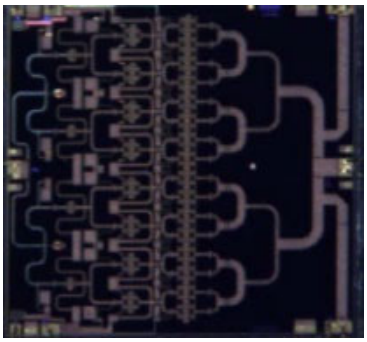
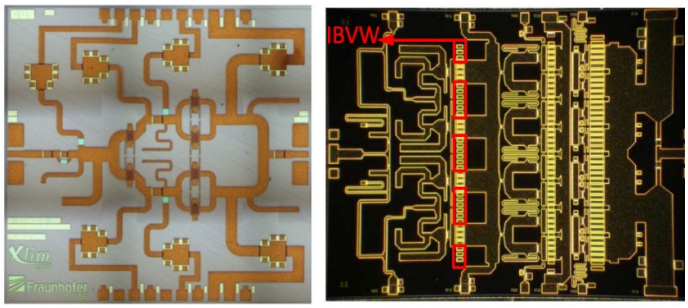


Figure 15. The 3-stack 16-combined PA150 nm GaAs pHEMT [75].

The 3-stage combined PA is common in power combining topologies, where desired performance can be achieved under an appropriate area. In [76–79], the 3-stage amplifiers composed of different unit amplifiers were presented, among which the maximum output power reaches 40 dBm [77] and the area is 15.75 mm².

In [80], three PA MMICs in 100 nm GaN HEMT at Ka band were reported. In order to evaluate the performance of GaN HEMT process, a single-stage PA (MMIC1) made up of a single HEMT is designed. The second PA (MMIC2) consists of two parallel MMIC1. Finally, a 2-stage power combination PA is designed (MMIC3), the input stage is two parallel HEMT drive output stage, which consists of 2 × 2 parallel HEMTs (see Figure 16a). The measured results of MMIC1/MMIC2/MMIC3 demonstrate that PAE and P_{sat} are 41%/33%/28% and 31.5/33.8/36.7 dBm, from 29 to 31 GHz.

Ref. [81] also demonstrated the method of combining two identical MMIC2 in parallel to form a new MMIC1, with an output power of 40 dBm and a PAE of 36%, respectively. In 2016, Hosseinzadeh, Navid proposed a method of placing isolating backvia wall (IBVW) between input stages to increase isolation and improve the stability of the system (see Figure 16b) [82]. Fabricated in the 100 nm GaAs pHEMT process, the compact-size wideband PA chip achieves P_{sat} and peak PAE of 37 dBm and 26%, respectively.



(**a**) (**b**)

Figure 16. (**a**) The 2-stage PA in 100 nm GaAs HEMT [80]. (**b**) Combining PA with IBVW in 100 nm GaAs pHEMT [82].

3.4.2. Balanced Amplifier

The balanced amplifier (BA) consists of two similar single-ended amplifiers in parallel and two 90° couplers as shown in Figure 17. The input signal is divided into two signals with the same amplitude and 90° phase difference through the input 90° coupler. These two signal components are amplified by PA1 and PA2, respectively. The amplified signal is then recombined through the reverse 90° phase of the 90° output coupler to obtain the final output power.

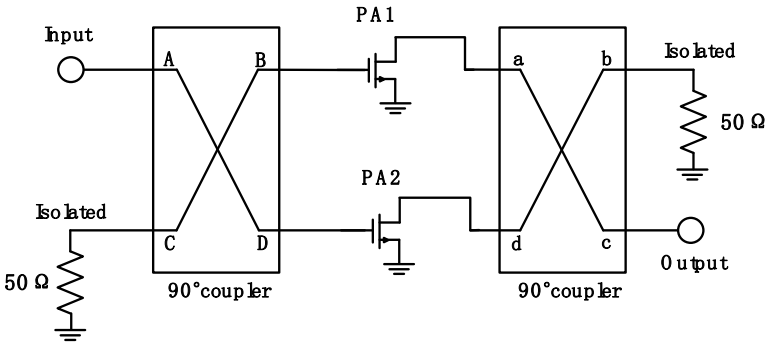


Figure 17. Balanced amplifier circuit schematic diagram.

Compared with single-ended amplifier, the balanced amplifier will consume higher DC power and occupy a larger chip area, but it cannot be ignored that it can provide higher output power and stability. After one branch of the balance amplifier is damaged, the other branch can work without stopping the amplifier.

In [83], D. L. Ingram proposed a 2-stage architecture amplifier, in which the power stage and the driver stage were both balanced amplifiers combined in parallel with an eight-way Wilkinson combiner (see Figure 18). Fabricated in 150 nm GaAs HEMT, the PA chip achieves peak PAE and P_{sat} of 28% and 35.4 dBm, respectively.

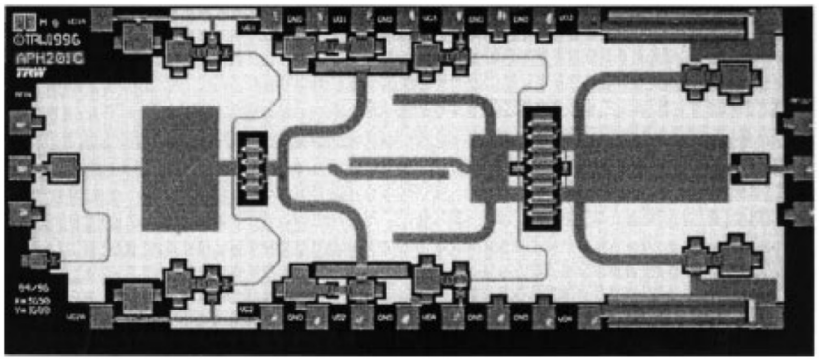
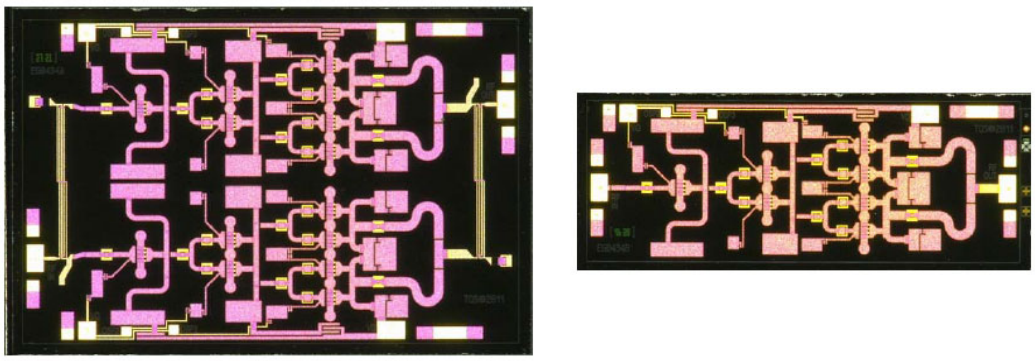


Figure 18. The 2-stage balanced PA in 150 nm GaAs HEMT [83].

The following year, in 1998, M. K. Siddiqui presented a two-stage balanced power amplifier using a 150 nm GaAs PHEMT process operating from 27.5 to 29.5 GHz for LMDS [84]. The measured results demonstrate P_{sat} and PAE are 30 dBm and 43%, respectively, at a lower operating voltage.

In 2005, N. Kinayman used three cascaded common-emitter (CE) Class-A balanced amplifier stages and a lumped elements matching network to achieve 18 dB gain and 12 dBm P_{sat} at 24 GHz [85].

C. F. Campbell proposed two amplifiers in [86]. First, a single-ended amplifier was designed and named MMIC2, and then MMIC1 was realized by balancing two MMIC2 devices with improved Lange coupler impedance and bond-wire inductance (see Figure 19). At a similar frequency, the MMIC1/MMIC2 attained output power 39.4/37 dBm and 26/30% PAE with gain of 28.5/29 dB. The output power of MMIC1 is nearly double that of MMIC2, but the PAE is reduced. Ref. [87] adopted the same design method and combined two third-order PA to achieve 37.1 dBm P_{sat} and 33% PAE in an area of 9.9 mm².



(**a**) (**b**)

Figure 19. (**a**) Balanced PA, (**b**) single-ended PA in 150 nm GaN HEMT [86].

3.4.3. Differential Amplifier

The traditional differential circuit is one that can amplify the difference between two input voltages. The circuit structure is shown in Figure 20. The circuit is generally symmetrical, with two inputs and two outputs.

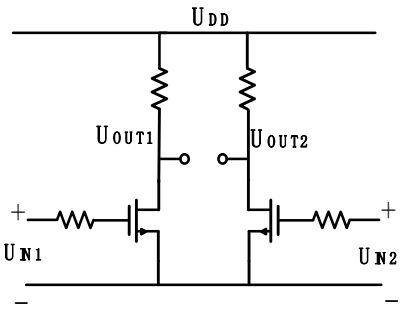


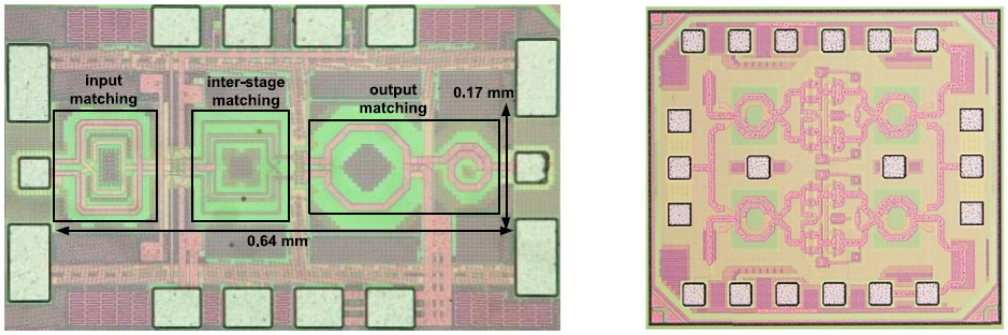
Figure 20. Differential amplifier circuit schematic diagram.

The most important advantage of using a differential structure is that the maximum output power of PA can be improved. When the input U_{IN1} and U_{IN2} are signals of equal amplitude and opposite phase, the input mode is a differential mode input. The final differential output voltage swing is two times the output voltage swing of the single-ended PAs. However, most systems require single-port outputs, a balun transformer and a power combiner, which introduce additional losses.

In Ref. [62], a 6-order LC input matching network was presented to expand the bandwidth. At the same time, H. Jia and C. C. Prawoto presented a 2-stage CS differential broadband PA based on a fourth-order magnetically coupled resonator (MCR) matching network (see Figure 21a) [88]. Compared with [62], both PAs cover the full Ka band, have similar gain and PAE, but the P_{sat} and P_{1dB} of [88] and [62] are significantly different, which are 15.3/ 25.3 and 12.9/23.6, respectively.

A fully integrated power amplifier with a capacitor-based neutralization technique and transformers and current-combining topology was proposed [89]. A transformer-based power synthesizer is used to combine two differential PA cells which consist of two CS to increase the output power. Fabricated in 28 nm CMOS process, the PA chip achieves P_{sat} of 17.9 dBm, peak PAE of 40.7% and output power density of 513.8 mW/mm^2.

At the same time, W. Huang presented an inductive neutralization technique implemented in the differential PA in 90 nm CMOS [90]. Four cascode cells are combined as differential power cells. The inductance neutralization structure combined with capacitance neutralization can solve the overall stability problem of the system without reducing the output power. This paper also uses current-combining topology, but current-combining topology will cause a phase imbalance [91]. To solve this problem, a new type of asymmetrical transformers is designed to further compensate the phase imbalance (see Figure 21b). The measured results demonstrate P_{sat} of 26 dBm, peak PAE of 34.1% at 28 GHz, and record output power density of 992.8 mW/mm^2.



(**a**) (**b**)

Figure 21. (**a**) The 2-stage CS differential PA in 60 nm CMOS [88] (**b**) 2-stage cascode differential PA in 60 nm CMOS [90].

In [92], it is mentioned that the cold-FET-based interstage matching network can improve the linearization. In order to enhance the linearity and suppress sideband, cold-mode linearizer with additional transmission line was proposed. The PA, composed of 2-stage CS differential amplifiers, achieves 33.6% PAE and 19.7 dB gain while maintaining an output power higher than 16.8 dBm.

A summary comparison with power combining PA measurements is given in Table 4.

Table 4. Comparison of the measurement results with the power combining PA.

Ref.	Tech	Frequency (GHz)	Gain (dB)	P_{sat} (dBm)	P_{1dB} (dBm)	PAE_{peak} (%)	Area (mm^2)	Topology
[74]	350 nm GaAs	26.5–28.5	/	34.8	/	/	84.0	4-MMICs parallel combined
[75]	150 nm GaAs	35	23	37.2	/	30	14.7	3-stage combined
[76]	150 nm GaN	28	10.6	39.9	/	35	8.5	3-stage combined
[77]	100 nm GaN/Si	29–33	25	40	/	30	15.75	3-stage combined
[78]	100 nm GaN/SiC	26–33	22	38	/	25	15.8	3-stage combined
[79]	150 nm GaN/SiC	28–39	15	38.2	/	26.1	14.0	3-stage reactive combined
[80]	100 nm GaN/SiC	29	14	36.7	/	28	9.0	2-stage combined
[81]	200 nm GaN	31.5	25	40	/	36	16.7	2-stage combined
[82]	100 nm GaN	31–40	20	37	35	28.2	11.9	Combined with IBVW
[83]	150 nm GaAs	33	11.5	35.4	/	28	6	2-stage MMIC balanced
[84]	150 nm GaAs	28	16	32	/	35	/	2-stage balanced
[85]	80 GHz-f_T SiGe	24	18	12	/	/	/	3-stage CE balanced
[86]	150 nm GaN	28.5/29	24/25	39.4/37	/	26/30	9.7/4.8	2-stage/4-stage balanced
[87]	150 nm GaN	38	13	37.1	/	33	9.9	Two 3-stage balanced combined

[88]	65 nm CMOS	32	20.8	15.3	12.9	32.6	0.11 #	2-stage CS differential
[89]	28 nm CMOS	27	13.1	17.9	14.7	40.7	0.12	1-stage CS differential
[90]	90 nm CMOS	28	16.3	26	23.2	34.1	0.401	2-stage cascode differential
[92]	65 nmCMOS	38	19.7	16.8	14.2	33.6	0.31	2-stage CS differential

Core area.

As can be seen from Table 4, the P_{sat} of the power-combined PA is very high, especially in GaAs and GaN technologies. In the above data, the saturated output power of basically all PA in III-V technologies reached 35 dBm, and the highest reached 40 dBm. Although higher power can be obtained, PA has a large area and is widely used in 5G communication technology.

In particular, the performance of power amplifier in GaN/SiC was significantly improved. Despite the high cost and limited availability of SiC substrates, they can achieve complete modules with superior performance. It is suitable for applications where performance is more important than cost, such as military and satellite.

The corporate combiner power amplifier selects III-V technologies to alleviate the reduction in efficiency and PAE with the increase in synthesis number, and its effect is obvious. However, we also find that the area of the corporate combiner power amplifier is large and changes sharply with the increase in the synthesis order.

The differential power combining technique is normally used in bulk CMOS due to its multilayer metal layer. Transformers are one of the most common methods to combine power in CMOS. Multiple metal layers can realize 3D wide side transformer and reduce parasitic capacitance for better performance. As can be seen from the data in [88–90,92], PA can maintain a high PAE while maintaining a not low output power and gain.

3.5. Doherty Power Amplifier

With the development of satellite communication technology, in order to obtain a higher transmission rate, the signal contains multi-channel subcarriers with variable phase and amplitude, but also makes the signal peak-to-average-power ratio (PAPR) larger. Signals with high PAPR require power amplifiers with higher efficiency and linearity. The Doherty power amplifier (DPA) has been widely used because of its relatively simple implementation and obvious efficiency improvement [93,94].

A conventional DPA typically includes a power splitter, carrier amplifier, peaking amplifier and load modulator. Among them, the carrier amplifier is also the main amplifier, which is in the class AB bias, and the peak amplifier is also the auxiliary amplifier, which is in the class C bias. The Doherty PA circuit schematic diagram is shown in Figure 22.

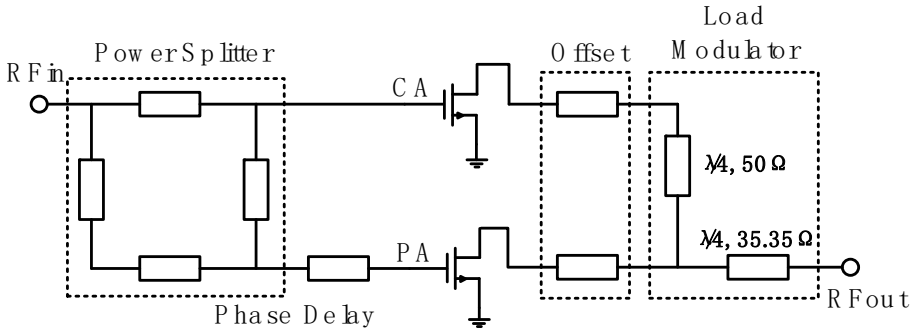


Figure 22. Doherty PA circuit schematic diagram.

The input signal is divided into two signals of equal amplitude and phase through the power splitter, which enter the carrier amplifier and peaking amplifier, respectively. After amplifier amplification, the output is synthesized by the load modulation network. Load modulation networks are generally composed of a $\lambda/4$ transmission line to match the output impedance of the carrier amplifier and peak amplifier to 50 Ω through impedance transformation.

Generally, carrier amplifiers and peak amplifiers use the same device, but due to the low input bias of the peak amplifier, the output current of the peak amplifier cannot be the same as that of the carrier amplifier. Therefore, the optimal load modulation cannot be realized, resulting in low output power and efficiency. To solve the problem of low output power and efficiency of DPA, the common solutions use asymmetric DPA topology, using new load modulation scheme to realize the full modulation, etc.

Asymmetrical DPA topologies include asymmetrical input splitter [95] and asymmetrical stack gate bias [96]. In 2013, a 32 GHz transformer-based Doherty PA with Wilkinson splitter was presented. The Wilkinson splitter distributes the input signal unequally to carrier amplifier and peaking amplifier, and matches the output impedance to 50Ω to improve the output power. The fabricated prototype exhibits measured P_{1dB} of 25.1 dBm, peak PAE of 38% and record PAE of 27% at 6 dB back-off power. In [96], D. P. Nguyen proposed a stack-FET DPA. The gate bias of the common-gate transistors in the stacked FET can control the current of peaking amplifier (see Figure 23). With higher gate bias, the peaking amplifier's higher current at saturation enhances efficiency. The experimental results demonstrate that the peak PAE is 37%, PAE at 6- dB back-off power is 27% and P_{1dB} is 28.2 dBm at 28 GHz.

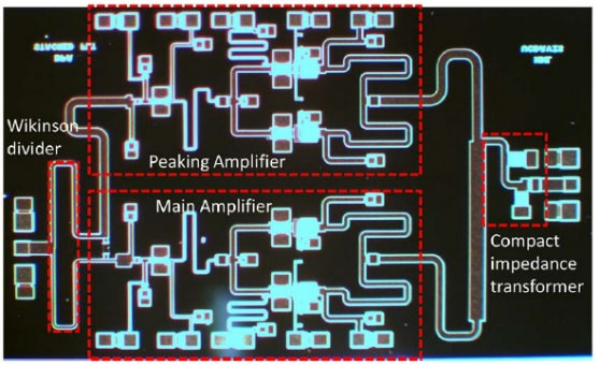


Figure 23. Stacked-FET MMIC DPA in 120 nm GaAs pHEMT [96].

In 2018, D. P. Nguyen presented a new load-pull-based design technique in order to choose an appropriate device size and the impedance of the $\lambda/4$ inverter to achieve the

highest PAE [97]. With this new method, the experimental results show PAE of 32% at 6 dB back-off and 28.5% at 8 dB back-off.

In addition to the above methods, the parallel series parallel power combination technology [98] commonly used in bulk CMOS technology is used to improve the output power, and the high turn ratio current source transformer [99] is used to improve the fallback efficiency (see Figure 24).

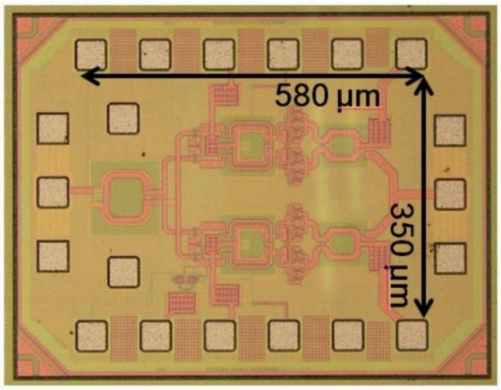


Figure 24. Transformer-based DPA in 90 nm CMOS [99].

In the GaAs process, in order to reduce the chip area, the methods mentioned are as follows: Lange coupler [100,101]; input broadside coupler [102]; removal of the offset line when the power ratio between the main and auxiliary PA is appropriate [103]; replacing the transmission lines and offset lines with LC elements [104], and so on.

The bulk CMOS technology is relatively small in area compared to the GaAs process, but the efficiency and P_{sat} of bulk CMOS are limited due to lossy and complex Doherty output networks. To address these challenges, some approaches have been proposed.

N. Rostomyan [105] proposed a combiner based on the analytical synthesis methodology, which performs the DPA impedance modulation and output matching simultaneously to achieve lower loss. Fabricated in 45 nm SOI CMOS process, the PA chip achieves P_{sat} and peak PAE at 22.4 dBm and 40%, respectively. In [106], a DPA with distributed-active-transformer (DAT) power combining is reported. The measured results demonstrate that P_{sat} and peak PAE are 28.3 dBm and 30.4% at 28 GHz.

A summary comparison with Doherty PA measurements is given in Table 5.

The Doherty power amplifier is an attractive option to improve back-off efficiency due to its structure. As we can see from Table 5, the 6 dB back-off PAE is much higher than its classical counterparts (10%~15%); the highest PBO factor in DPA was 32%. It is illustrated that the PAE and PBO of the PAs on GaAs are clearly much higher than that on Si and SiGe, but the area is also much larger than that on Si CMOS.

Table 5. Comparison of the measurement results with the Doherty PA in CMOS.

Ref.	Tech	Frequency (GHz)	Gain (dB)	P_{sat} (dBm)	PBO † (%)	PAE_{peak} (%)	Area (mm^2)	Topology
[95]	150 nm GaAs	26.4	10.3	25.3	27	38	25	Doherty PA
[96]	150 nm GaAs	25.5–29.5	15	/	27	37	4.93	Doherty PA
[97]	150 nm GaAs	28.5–31.5	10.5	/	32	38	4.59	Doherty PA
[98]	28 nm CMOS	32	6.7	19.8	/	21	1.87	Doherty PA
[99]	90 nm CMOS	28.7–41.9	19.8	20.7	13.1	32.7	0.203 *	Doherty PA
[100]	150 nm GaAs	38–46	7	21.8	17	/	2	Doherty PA
[103]	150 nm GaAs	29–31.8	/	25.7–26.8	21–32 ††	31–38	3.57	Doherty PA
[104]	150 nm GaAs	25.8	7	25.1	12.6	16.5	2.25	Doherty PA

[105]	45 nm SOI CMOS	28	10	22.4	28	40	0.63 *	Doherty PA
[106]	130 nm SiGe BiCMOS	28	20.5	28.3	27.8	30.4	4.19	Doherty PA

† 6 dB back-off PAE, unless other noted. †† 7 dB back-off PAE. * Without pad.

4. Conclusions

This paper reviewed the background, technologies and circuit topologies of the Ka band power amplifier for the satellite communication system. The Ka band power amplifier is a key component and hot research topic in broadband satellite communication systems with the rapid growth of low orbit Sat-COM application in recent years. The features, advantages, and trends of the different technologies and topologies of Ka band PA are summarized and discussed in detail. III-V technologies, such as GaAs, GaN, and InP HEMT, are traditionally used to implement the Ka band power amplifier, due to their advantage in high output power and linearity. However, the Ka band PA based on silicon technologies is growing rapidly due to their tremendous advantage of low cost and high level of integration. The circuit topologies adopted by the Ka band PA include common source, cascode, stacked field-effect transistor (FET), power combining, and Doherty structure. The common source topology is the simplest structure with a balance performance of gain, bandwidth, and power. The cascode topology shows good power gain, but a disadvantage on linearity due to the memory effect. The stacked-FET topology shows a very good voltage swing but decreased efficiency and linearity performance due to the imbalance on each layer of the stacked FET. The power combining method is a promising method to achieve the desired power level with limited voltage swing, and the power combining synthesis network is an important design challenge. The differential topology is commonly used in CMOS PA for the Ka band. The Doherty architecture is a potential method to break the limitation of efficiency of CMOS PA at the Ka band.

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