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Fast Design Space Exploration and Multi-Objective Optimization of Wide-Band Noise-Canceling LNAs

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Abstract: Design optimization of RF low-noise amplifiers (LNAs) remains a time-consuming and complex process. Iterations are needed to adjust impedance matching, gain, and noise figure (NF) simultaneously. The process can involve more iterations to adjust the non-linear behavior of the circuit which can be represented by the input-referred third-order intercept (IIP3). In this work, we present a variation-aware automated design and optimization flow for a wide-band noise-canceling LNA. We include the circuit non-linearity in the optimization flow without using a simulator in the loop. By describing the transistors using precomputed lookup tables (LUTs), a design database that contains 200,000 design points is generated in 3 s only without non-linearity computation and 10 s when non-linearity is taken into account. Using a gm/ID-based correct-by-construction design procedure, the generated design points automatically satisfy proper biasing, input matching, and gain matching requirements. The generated database enables the designer to visualize the design space and explore the design trade-offs. Moreover, multi-objective optimization across corners for a given set of specifications is applied to find the Pareto-optimal fronts of the design figures-of-merit. We demonstrate the presented flow using two design examples in a 65 nm process and the results are verified using Cadence Spectre.

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1. Introduction

The increased demand on integrated circuits in recent decades has increased the need for fast circuit-design techniques to decrease the design time and the time to market. Care has been given to digital circuit automated design flow, which has already become mature and robust, while analog design has not received that much care.

Many approaches have been proposed to address the problem of the automation and optimization of analog and RF design [1,2]. An example is the knowledge-based approach, which attempts to solve an inverse problem, i.e., find the transistor sizing and bias voltages given a set of required design specifications. This approach depends mainly on the experience of the analog designer to make some assumptions and use simplified expressions to relate the specifications to the circuit sizing and biasing. The drawback of this approach is the discrepancy between the synthesized design results and the simulation results due to the assumptions and simplifications used [1,3]. In addition, the synthesized design point may not be optimal.

Another approach is the simulation-based optimization approach, which overcomes the drawbacks of the previous approach by relying on a simulator to solve the direct problem, i.e., compute the required specifications given the transistor sizing and bias voltages, then an optimization loop is used to obtain the best sizing and biasing that satisfies the design specifications. This approach gives very accurate results because no assumptions or simplifications are made; however, it is very time-consuming to call the simulator at every iteration in the optimization loop [1].

A third approach is the equation-based optimization. It is similar to the simulation-based optimization, but the simulator in the loop is replaced by equations. Evaluating the equations is faster than invoking the simulator. But the equations are approximate and do not match the actual device models used in the simulator, thus, the accuracy is degraded [1,2].

The work presented in this paper focuses on the design automation and optimization of wide-band LNAs. The use of wide-band RF front ends has become more popular due to the increased demand for their usage in multi-standard transceivers. To operate with different standards, the LNA (which is usually the first block in the chain) must be able to handle the frequency ranges of all these standards [4]. This can be achieved using either multiple narrow-band LNAs or a single wide-band LNA. The former solution suffers from consuming large area due to the usage of multiple inductors, in addition to complexity of selecting between the different LNAs [4]. The latter solution is much simpler due to the use of a single inductor-less LNA. But it may suffer from limited operation frequency and higher noise figure [4].

Several circuit topologies can be used to implement wide-band LNAs. One main concern is that the circuit must have a finite input impedance that can be adjusted to satisfy input matching. Two examples of these topologies are the common gate (CG) amplifier and the resistive feedback common source (CS) amplifier. The problem with these topologies is the fundamental limit for the minimum noise figure (NF), which is about 3 dB if the input impedance is matched to the source resistance. To overcome this problem, noise-canceling techniques were proposed to cancel the amplifying transistor noise [4–6]. These noise-canceling LNA topologies allow wide-band operation without the 3 dB limitation in the NF.

Several papers discussed the automation and optimization of narrow-band and wide-band LNAs. In Ref. [7], design automation was proposed for a single-ended narrow-band LNA. The design flow depended on the invoking the simulator in the loop, which increased the synthesis time. In addition, the non-linearity was not addressed. The work in [7] was further improved in [8] by adding some modules to replace the simulator and to address the non-linearity. However, it suffered from low accuracy and did not consider the design corners and the design space trade-offs. In Ref. [9], a tool to analyze the noise-canceling LNA was proposed, but it invoked the simulator in the loop, suffered from low accuracy, and did not address design corners and the non-linearity. The flow in [10] presented accurate results that address design corners, but it invoked the simulator in the optimization loop, which increased the time needed for the optimization to several hours.

In this paper, we use a hybrid analog automation approach that performs fast design space exploration and multi-objective optimization of a wide-band noise-canceling LNA while taking design corners and non-linearity into consideration. The proposed approach captures the merits of the knowledge-based, simulation-based, and equation-based approaches. First, we abstract the device models in precomputed lookup tables (LUTs) [3,11,12]. These LUTs are generated from the simulator, thus, simulator accuracy is preserved. But they are generated only once for a given technology, thus, the simulator is not invoked in the loop. Second, we use a symbolic solver to generate the equations of the design metrics. This avoids the approximations and simplifications involved in manually derived expressions. Third, we use knowledge-based rules to discard invalid design points and generate a search space of design points that are correct-by-construction. Fourth, the automation process is vectorized to solve a large number of design points simultaneously in a short time. This allows fast exploration of the design space and finding the Pareto-optimal fronts for multi-objective optimization.

The next sections are organized as follows: The noise-canceling LNA background is presented in Section 2. The proposed design flow is presented in Section 3. The results of the proposed automation flow and two design examples are presented in Section 4. The paper is concluded in Section 5.

2. Noise-Canceling LNA Background

Figure 1 shows the noise-canceling LNA topology considered in this paper. The noise cancellation is performed by subtracting the output of the CS and CG amplifiers, where the noise at the two outputs is correlated and has the same sign. If the CS and CG stages have the same gain, the CG amplifier noise can be ideally canceled.

Figure 1. CG-CS Noise-Canceling LNA.

If the transistor output resistance (r_o) is neglected, the gain of the CG stage (A_1) is approximately given by

$$A_1 \approx g_{m1} R_{Lp} \quad (1)$$

while the gain of the CS stage (A_2) is approximately given by

$$A_2 \approx -g_{m2} R_{Ln} \quad (2)$$

The input impedance seen by the input source is approximately equal to $1/g_{m1}$, which should be matched to the input source resistance R_S . Assuming that $r_{o3} \gg R_S$, where r_{o3} is the output resistance of M_3 , the noise of the transistor M_1 appears at the output of the CG amplifier as voltage noise ($V_{n1,CG}$) whose mean square value is given by

$$\overline{V_{n1,CG}^2} \approx \frac{4kT\gamma}{g_{m1}} \left(\frac{g_{m1} R_{Lp}}{1 + g_{m1} R_S} \right)^2 \quad (3)$$

where T is temperature in Kelvin and k is the Boltzmann constant. Substituting with the input impedance matching condition, then (3) reduces to

$$\overline{V_{n1,CG}^2} \approx kT\gamma R_S (g_{m1} R_{Lp})^2 \quad (4)$$

Assuming that M_1 is the only noise source in the circuit, then the noise figure (NF) in dB is given by

$$NF = 10 \log(1 + \gamma) \quad (5)$$

Since γ is typically close to 1, the noise figure is at least 3 dB. Actually, the NF is even higher because M_1 is not the only noise source.

The noise of M_1 also appears at the CS amplifier output as voltage noise ($V_{n1,CS}$) whose mean square is given by

$$\overline{V_{n1,CS}^2} \approx \frac{4kT\gamma}{g_{m1}} \left(\frac{R_s}{\frac{1}{g_{m1}} + R_s} \right)^2 (g_{m2}R_{Ln})^2 \quad (6)$$

Applying the matching condition, (6) reduces to

$$\overline{V_{n1,CS}^2} \approx KT\gamma R_s (g_{m2}R_{Ln})^2 \quad (7)$$

Noting that both (4) and (7) are from the same source (i.e., correlated), then if they are equal in magnitude, they will cancel each other when the output is taken differentially, i.e., the noise of M_1 is canceled. This will be satisfied if (1) and (2) are equal. It should be noted that the approximate expressions presented in this section are for the purpose of illustration only. The proposed design procedure uses exact expressions that are generated using a symbolic solver.

3. The Proposed Automation Flow

3.1. The Lookup Tables (LUTs)

The LUTs are multidimensional arrays that store the DC, AC, and noise parameters of transistors. They are generated by invoking the simulator and performing different sweeps to extract the transistor parameters. The generated parameters are post-processed to enable fast and efficient extraction of the device parameters when using the g_m/I_D ratio as a design knob [3], thus, the g_m/I_D design methodology can be seamlessly integrated in the design flow. Interpolation is performed to return the parameters that are off the LUTs grid. The enhanced interpolation method proposed in [3] is used in this work, where the derivative LUTs (e.g., g_m) are used to enhance the accuracy and the speed of the interpolation process. The LUTs are generated only one time for a given technology, and the simulator is invoked only in this step. Once the LUTs are generated, they can be used to explore the design space of the topology being studied in a very short time.

3.2. The Design Degrees of Freedom (DoFs)

The design DoFs are the independent variables of the circuit that are changed from one design point to another. Selecting the DoFs randomly will result in many invalid design points. Thus, the process was constrained to generate design points that are correct-by-construction.

The input resistance of the circuit is required to match R_s which adds a constraint on selecting g_{m1} . Given the input matching constraint, either the current of M_1 (I_{D1}) can be used as a DoF and the g_m/I_D is calculated or the g_m/I_D is used as a DoF then I_{D1} is calculated. The later solution was adopted to ensure generating valid design points because the range of the g_m/I_D is intuitive and confined. On the other hand, randomly selecting I_{D1} will result in design points that have invalid g_m/I_D .

The ratio between the bias currents of the CS and CG stages (I_{D2}/I_{D1}) is used as a DoF, thus, I_{D2} is constrained. Since we want to match the CS and CG voltage gains, g_{m2} (and hence g_{m2}/I_{D2}) is constrained and cannot be used as DoF. In addition, to improve the matching, L_2 is set to be equal to L_1 and they are used as a single DoF.

Using the load resistors (R_{Lp} and R_{Ln}) as DoFs may result in invalid DC output voltage ($V_{out,DC}$), thus, $V_{out,DC}$ is itself used as a DoF. To avoid the need for decoupling caps at the output, the resistors are chosen to adjust the CS and CG DC output voltage to have the same value

$$I_{D2}R_{Ln} = I_{D1}R_{Lp} \quad (8)$$

The remaining DoFs used in the design are the channel length of M_3 (L_3), g_{m3}/I_{D3} , and $V_{Dsat,margin}$ of M_3 which is the difference between the V_{DS} of M_3 and its saturation voltage (V_{Dsat}). The described strategy for selecting the DoFs coupled with the design

procedure explained in the next subsection guarantee that the generated design points will have proper DC biasing, and will have the input matching and CS-CG voltage gain matching satisfied, i.e., the generated design points are correct-by-construction.

3.3. The Symbolic Solver

A custom Python-based symbolic solver based on modified nodal analysis (MNA) is used to extract the circuit different AC performance metrics. The circuit netlist, which contains symbolic parameters, is passed in a string format as an input to the symbolic solver. The netlist is parsed, then symbolic matrices are constructed, where each transistor is replaced with its AC small-signal model. After solving the matrices, the resulting symbolic equations are then stored in the form of Python functions, which are invoked when the performance metrics are evaluated.

3.4. The Design Procedure

The symbolic solver is used to generate exact equations for the circuit transfer function, input impedance, and output noise as described in the previous subsection. These equations are then post-processed to evaluate the LNA specifications (gain, bandwidth, NF, and S11) at different design points.

Figure 2 illustrates the design flow used in this work. After the symbolic equations are generated using the symbolic solver, they are then used along with the LUTs and circuit DoFs to generate a design database containing a very large number of design points. The design procedure is implemented in Python. The variables used in the evaluation of DC operating point and AC quantities are stored in the form of NumPy vectors. Each variable has a length equals to the number of design points. The operations done on the variables are element-wise vectorized operations which avoid looping on the design points. This boosts the execution speed and enables handling many design points.

The generated design database can be used to visualize the design space. In addition, to obtain an optimum design point satisfying a specific set of constraints, an optimizer is used, where a new set of DoFs is generated at each iteration until the optimizer reaches an optimum design point.

Figure 2. Design database generation algorithm.

Figure 3 illustrates the details of the design procedure. Since the exact input impedance is initially unknown, an initial guess is used by assuming it is equal to $1/g_{m1}$, which must be equal to R_S for input matching. Since g_{m1}/I_{D1} is already a DoF, now I_{D1} is determined. The resistors values are then calculated using

$$R_{Lp(n)} = \frac{V_{DD} - V_{out,DC}}{I_{D1(2)}} \quad (9)$$

Figure 3. Proposed design procedure for the noise-canceling LNA.

Now to calculate g_{m2}/I_{D2} , another initial guess is made that the CG and CS voltage gains are as given by (1) and (2). If this assumption is combined with (8), then

$$\frac{g_{m1}}{I_{D1}} = \frac{g_{m2}}{I_{D2}} \quad (10)$$

Since the operating point parameters are now calculated, the actual input impedance can be accurately computed using the symbolic solver equations. Then I_{D1} is adjusted iteratively till the input impedance matching is satisfied.

At this point, the two gains A_1 and A_2 are not exactly equal due to the assumption made in (10). The gain mismatch (ΔA_{dB}) is defined as [6]

$$\Delta A_{dB} = 20 \log\left(\frac{A_1}{A_2}\right) \quad (11)$$

To make the gain mismatch less than a given tolerance (e.g., 10 mdB), g_{m2}/I_{D2} is adjusted iteratively till the condition is satisfied. It should be noted that at this point the CG amplifier operating point is kept unchanged, so there is no need to re-evaluate the input impedance. After the final operating point is computed, all the circuit metrics are calculated (gain, bandwidth, NF, and S11). Next, the non-linearity is evaluated by computing the input-referred third-order intercept (IIP3) as will be illustrated in the next subsection. It should be noted that the above procedure is vectorized, i.e., performed for many design points simultaneously using element-wise vector operations.

3.5. Non-Linearity Calculation

The basic method to analyze non-linearity is to perform a transient simulation then post-process the results using Fourier analysis to compute the harmonics. The main drawback of this method is the time and the memory used in the transient simulation. Another popular technique is the harmonic balance method, where the node voltages and branch currents are assumed to be the summation of sinusoidal signals of harmonic frequencies. Iterations are then made by the simulator to calculate the coefficients of these sinusoidal signals [13]. Alternatively, non-linearity analysis can be performed using the Volterra series and the phasor methods. The Volterra series method can be regarded as an extension to the Taylor series when the system is dynamic. It represents the system using multi-order transfer functions named “Volterra kernels”, whose s-domain forms are obtained using multidimensional Laplace transform [13–15]. All the previous methods require complex computations and large memory consumption, where many first, second and third derivatives will be required to be stored or computed. An equation-based non-linearity calculation technique based on gm/ID was discussed in [16,17], but it suffers from limited accuracy due to the approximations made in the derivations.

The algorithm used to calculate IIP3 in this paper is illustrated in Figure 4. After the DC operating point and AC parameters are calculated as illustrated in the previous subsection, a sweep is done for the input voltage, where the difference between the consecutive steps is small enough to apply a small-signal model. At each iteration, the small-signal parameters are evaluated and used to calculate the voltage gain from the input to different nodes, then the new node voltages are evaluated. The new set of node voltages is used to calculate the small-signal parameters for the next iteration and to obtain the node voltages for the next value of the input voltage in the sweep. Once the output voltage is determined for each input voltage, curve fitting is applied to obtain the non-linear input-output characteristics. Given the non-linear input-output characteristics, the output harmonics and the intermodulation products can be computed by calculating the fast Fourier transform (FFT) of the output.

Figure 4. Non-linearity calculation algorithm.

4. Results and Discussion

4.1. Design Trade-Offs and Design Space Visualization

The proposed design flow can be applied to any technology node by simply generating the LUTs of the desired technology. For the purpose of illustration, this section presents results generated from a 65 nm technology. The design database is generated according to the ranges of DoFs shown in Table 1. Three design corners are taken into consideration: TT 27 °C (Nominal), FF −40 °C (C1) and SS −90 °C (C2). The supply voltage is 1.2 V, and the output DC voltage is set to 0.6 V. The number of design points generated in the design database is 200,000 points. The design points in the database are correct-by-construction, i.e., they satisfy both impedance matching condition and less than 10 mdB of gain mismatch to achieve noise cancelation. The generation of the design database takes only three seconds without the non-linearity algorithm, and 10 s when the IIP3 is computed. The machine used in our test has Core-i7-8550U processor and 12 GB RAM, i.e., it is a standard computer that does not have any special capabilities.

Table 1. DoFs used in the design database generation.

DoF	Unit	Min	Max
g_{m1}/I_{D1}	S/A	8	20
g_{m3}/I_{D3}	S/A	8	20
L_1	nm	60	200
L_3	nm	60	200
$M_3 V_{Dsat,margin}$	mV	100	300
I_{D2}/I_{D1}	-	1	15

The proposed design flow is applied to the circuit topology shown in Figure 1. But it should be noted that if any modification is required in the circuit topology, the changes required are minor. The DC solution part will be amended by modifying the DC nodal/mesh equations describing the circuit. For the AC solution, the new netlist will be provided to the symbolic solver, and new expressions for the circuit performance metrics will be automatically generated. Regenerating a new design database using the LUTs takes a small time (a few seconds) as previously stated.

Given this large dataset of valid design points, the design space can be explored for different trade-offs. Furthermore, an optimizer is used to perform multi-objective optimization. By changing the weight assigned to each objective, the selected optimal design point can be tuned on the Pareto-optimal front of the design space. In addition, the selected optimal design point will satisfy any arbitrary design constraints across the three corners.

Figure 5 shows the design space of the bandwidth vs. the gain. Please note that the bandwidth here is defined as the smaller of the gain 3 dB bandwidth and the reflection coefficient -10 dB bandwidth. Optimization is run three times to maximize gain and bandwidth simultaneously using different weights for gain and bandwidth. As shown in the figure, when the gain increases, the bandwidth decreases, and vice versa. The optimized design points move on the Pareto-optimal front in the top right to maximize gain and bandwidth.

Figure 5. Bandwidth vs. gain design space and optimal design points for the three corners: TT 27 °C (Nominal), FF -40 °C (C1), and SS 125 °C (C2).

Figure 6 shows the design space of the NF vs. the gain. As shown in the figure, there is an optimum gain that will lead to the minimum noise figure. A noise figure less than 3 dB can be achieved when the design is properly optimized. By assigning different weights to the optimization objectives (NF and gain), the optimized design points move on the Pareto-optimal front in the bottom right to maximize gain and minimize noise.

Figure 6. NF vs. gain design space and optimal design points for the three corners: TT 27 °C (Nominal), FF -40 °C (C1), and SS 125 °C (C2).

Figure 7 shows the design space IIP3 vs. gain. As shown in the figure, the maximum IIP3 that can be achieved decreases when the gain increases. This is expected as the amplifier saturates with less input power when the gain increases. By assigning different weights to the optimization objectives (IIP3 and gain), the optimized design points move on the Pareto-optimal front in the top right to maximize IIP3 and gain.

Figure 7. IIP3 vs. gain design space and optimal design points for the three corners: TT 27 °C (Nominal), FF −40 °C (C1), and SS 125 °C (C2).

Figure 8 shows the design space of NF vs. bias current. Please note that we fixed the output dc value to 0.6 V, which means that as bias current increases, the resistance value decreases, thus, the gain decreases. This means that the noise figure also has an optimum value, where it is minimized at a specific bias current. By assigning different weights to the optimization objectives (NF and bias current), the optimized design points move on the Pareto-optimal front in the bottom left to minimize NF and power consumption.

Figure 8. NF vs. total bias current (in Ampere) design space and optimal design points for the three corners: TT 27 °C (Nominal), FF −40 °C (C1), and SS 125 °C (C2).

4.2. Design Examples

Two design examples are presented in this subsection. The two designs points should satisfy the constraints shown in Table 2. The first design point will have more weight for minimizing NF, and the second design point will have more weight for maximizing IIP3.

Tables 3 and 4 show the sizing of the synthesized designs for the first and second design points, respectively. Tables 5 and 6 show the achieved specifications across corners. The specifications are calculated at 1 GHz; however, results should not deviate from the reported values for any in-band frequency. The results show that when trying to minimize the noise figure, IIP3 decreases and vice versa. For the first example a NF less than 3 dB is achieved, but the IIP3 is −5.32 dB. For the second example, a higher IIP3 is achieved at the expense of the NF. This is expected as increasing IIP3 requires decreasing the gain, which will increase the minimum noise figure that can be obtained.

Table 2. Constraints used for the two design examples. The input matching and the noise cancellation gain matching requirements are automatically satisfied.

Spec	Condition
Gain	>14 dB
BW	>2 GHz
NF	minimum
IIP3	maximum

Table 3. Circuit sizing of the first design example.

Parameter	Value	Unit
L_1	100	nm
W_1	152.6	μm
L_2	100	nm
W_2	353.1	μm
L_3	65	nm
W_3	31.5	μm
R_{Lp}	440	Ω
R_{Ln}	134	Ω

Table 4. Circuit sizing of the second design example.

Parameter	Value	Unit
L_1	80	nm
W_1	56.7	μm
L_2	80	nm
W_2	341	μm
L_3	80	nm
W_3	126.8	μm
R_{Lp}	305	Ω
R_{Ln}	45	Ω

Table 5. Comparison of the achieved specifications from the proposed synthesis flow vs. spectre simulation results for the first design example.

	TT 27 °C		FF −40 °C		SS 90 °C	
	Synthesis	Simulation	Synthesis	Simulation	Synthesis	Simulation
Current (mA)	5.672	5.38	5.672	5.12	5.672	5.48
Gain (dB)	17.87	17.741	17.519	17.422	18.06	17.872
S11 (dB)	−19.08	−17.8	−16.63	−16.9	−16.5	−16.9
BW (GHz)	2.549	2.633	2.6	2.643	2.305	2.454
NF (dB)	3.05	3.2	2.78	2.98	3.166	3.35
IIP3 (dBm)	−5.32	−6.35	−5.2	−6.10	−5	−5.8

Table 6. Comparison of the achieved specifications from the proposed synthesis flow vs. spectre simulation results for the second design example.

	TT 27 °C		FF −40 °C		SS 90 °C	
	Synthesis	Simulation	Synthesis	Simulation	Synthesis	Simulation
Current (mA)	14.8	14.05	14.8	13.9	14.8	14.42
Gain (dB)	14.38	14.25	14.54	14.34	14.19	14.07
S11 (dB)	−18.36	−17.96	−17.61	−17.609	−17.39	−17.113
BW (GHz)	2.609	2.635	2.504	2.562	2.604	2.611
NF (dB)	4.163	4.266	3.98	4.08	4.29	4.412
IIP3 (dBm)	0.4	−0.54	1.08	0.14	−0.053	−1.51

Tables 5 and 6 also compare the synthesis results of the optimized designs using the proposed flow to simulation results using spectre simulator across corners. The results calculated using the proposed synthesis procedure deviates by less than 10% from the simulation results.

Figures 9–11 compares synthesis and simulation results for the gain, s11, and noise figure respectively for the first design point (Nominal corner) vs. frequency. The remaining design corners and the other design point have similar trends.

Figure 9. Gain (dB) vs. frequency (Hz) for the first design point nominal corner. **Figure 10.** S11 (dB) vs. frequency (Hz) for the first design point nominal corner.

Figure 11. NF (dB) vs. frequency (Hz) for the first design point nominal corner.

Figure 12 shows the simulated values of IIP3 at seven different frequencies. The simulated values begin to deviate from the synthesis IIP3 value at high frequencies as the algorithm used in this paper depends on the value of the in-band gain which is frequency independent. However, it is still accurate enough at frequencies not too far from the circuit bandwidth, which is the frequency range of interest.

Figure 12. IIP3 (dBm) vs. frequency (Hz) for the first design point nominal corner. The synthesis results use the in-band gain which is frequency independent. The error is small in the frequency range of interest.

5. Conclusions

We presented a hybrid analog design automation flow for wide-band noise-canceling LNA. Our flow uses precomputed LUTs to preserve the simulator accuracy while avoiding invoking the simulator in the loop. A symbolic solver is used to generate accurate equations for the design metrics. A gm/ID-based procedure is used to generate correct-by-construction design points that satisfy the basic design requirements. A vectorized implementation of the design procedure enables generating hundreds of thousands of design points in a few seconds. We illustrate that non-linearity can be evaluated using a fast technique that does not require invoking the simulator. The presented results show that the proposed flow enables fast visualization of the design trade-offs, informed design decisions, design tuning across corners, and multi-objective optimization.

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