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A Wideband Reconfigurable CMOS VGA Based on an Asymmetric Capacitor Technique with a Low Phase Variation

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Abstract: This paper presents a wideband digitally controlled variable gain amplifier (VGA) with a reconfigurable gain tuning range and gain step in a 65 nm CMOS process. A unique asymmetric capacitor-based reconfigurable technique is proposed to extend the gain tuning range and realize gain step reconfiguration. An active neutralization topology based on a stackless transistor is utilized to compensate for the additional phase shift introduced by the gain tuning. Moreover, a current-type digital-to-analog converter (DAC) is also integrated for easier precise gain control. With the asymmetric capacitor varying from 1000 fF to 200 fF with a step of 400 fF, the proposed VGA achieves a 12.2/9.2/6.1 dB gain tuning range with a 0.4/0.3/0.2 dB gain resolution, respectively. At the maximum gain tuning range mode, the measured minimum root-mean-square (RMS) phase error is 1.7° at 23.4 GHz. At the finest gain step control mode, the RMS phase error measured across 20–30 GHz is lower than 1.9°. The tested result also shows the proposed VGA achieves a peak gain of 13 dB with a 3 dB bandwidth of 21.4–29 GHz, and the output 1 dB compression point (OP_{1dB}) is up to 8.6 dBm at 25 GHz.

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1. Introduction

For the fifth-generation (5G) new radio (NR) phased array beamformers, the variable gain amplifier (VGA) is the key building block, which has attracted increasing attention from industrial and academic fields. The VGA is designed to serve both purposes. Firstly, it can effectively compensate for the different losses caused by the phase shifter during phase shifting [1,2]. Secondly, enough amplitude weighting can be provided for a phased array to achieve high sidelobe suppression [3–9]. For millimeter-wave (mm-wave) phase shifters (PSs), the 6 dB gain tuning range of the VGA is sufficient enough to cover the loss variation [2]. However, it is more desirable for the VGA to have a high gain resolution and low phase variation, to avoid introducing extra gain errors and degrading the phase resolution of PSs. For phased array systems, sidelobe suppression is very important, which directly determines the signal quality of the entire link. In order to achieve less than −30 dB sidelobe suppression, for a 16-element phased array, a range of gain tuning of about 12 dB is required, according to Taylor's method [10]. Based on the two applications mentioned above, a new generation VGAs should have reconfigurable characteristics of gain tuning range and gain step to simultaneously serve both purposes, which can greatly increase the flexibility of phased array systems. To the authors' best knowledge, so far, the VGA with reconfigurable gain tuning range and gain step size has not yet been reported.

Moreover, a VGA with low additional phase shift during gain tuning is also very important, which can greatly simplify the complexity of phased array calibration procedures [9]. To this end, various phase-invariant VGAs have been proposed [11–15], such as the study by [12], which achieves a 7.5 dB gain tuning range with <3.5° root-mean-square (RMS)

phase error across 27–42 GHz by introducing interstage inductance. However, the designs mentioned above all adopt multiple-stack transistor structures, which suffer from more complex circuit topologies and higher supply voltage values, compared with stackless topologies under the same technology node and the normal supply voltage recommended by the vendor.

To address these issues, a new technique named as asymmetric capacitor-based reconfigurable technique is proposed to extend the gain tuning range and reconfigure the gain step. Based on a stackless transistor structure, an active neutralization technique is adopted to minimize the additional phase shift during gain tuning. Furthermore, for achieving accurate gain control to reduce gain error, the chip also integrates a high-resolution digital-to-analog converter (DAC).

2. Design and Analysis of VGA

Unlike the widely used current-steering (Figure 1a) and Gilbert-cell-based (Figure 1b) VGA structures [16–21], the proposed reconfigurable digitally controlled VGA used a stackless common source (CS) topology, as plotted in Figure 1c, which has advantages such as a simpler circuit structure and lower power supply. Figure 2a presents the full circuit schematic of the proposed reconfigurable VGA, and in both stages, a differential CS structure was used. Among them, the input stage is a variable gain stage to achieve gain tuning, and the output stage is a fixed gain stage to realize high output power. Furthermore, in order to more easily achieve accurate gain control and high robustness against the process and supply voltage and temperature variations (PVT) [16–20], the designed VGA used a digital control method. The control voltages V_a and V_b were generated by a 7-bit current-type DAC control circuit [22]. Additionally, to achieve wideband matching and compact layout, transformer-based high-order matching networks were employed.

Figure 1. Commonly used mm-wave VGA structures: (a) classic current-steering VGA with two-stack transistor structure; (b) classic Gilbert-cell-based VGA with two-stack transistor structure; (c) proposed CS VGA with stackless transistor structure.

Figure 2. (a) Schematic of the proposed reconfigurable digitally controlled VGA and (b) diagram of the structure of the asymmetric capacitors C_x and C_y , where C_x is an adjustable capacitor and C_y is a fixed capacitor.

2.1. Asymmetric Capacitor-Based Reconfigurable Technique

The core idea behind the proposed asymmetric capacitor-based reconfigurable technique was to connect asymmetric capacitors C_x and C_y in series on the gate nodes of transistors (M_1 – M_4), respectively, as shown in Figure 2a. It should be pointed out that since the value of C_x is different from C_y , it is called asymmetric capacitors. Adjusting the values of asymmetrical capacitors provides another dimension of gain control, and hence, reconfigurable gain tuning range and gain step can be achieved. Figure 2b depicts the structure of the applied asymmetric capacitors. To achieve three configurations, the adjustable capacitor C_x was designed to be composed of three capacitors and two switching transistors, which are controlled by the bias voltage of Ctr1 and Ctr2. In addition, to ensure the reconfigurable effect, it is necessary to ensure that the designed capacitances of the asymmetric capacitors are as close as possible to the desired theoretical value. Based on this, both of the asymmetric capacitors used in this study were metal insulator metal (MIM) topology, because of its high resistance to process deviation. Meanwhile, C_x and C_y used similar capacitor arrays.

To investigate the reconfigurable mechanism, the core of the variable gain stage is shown separately, and its simplified schematic diagram is shown in Figure 3a. For further and more intuitive theoretical analysis, the corresponding half-side small-signal equivalent circuit is also established, as shown in Figure 3b. Based on Figure 3b, the voltage gain can be calculated by

$$G = \frac{V_{out}}{V_{in} + -V_{in-}} \approx \frac{A_1 g_{m1} - A_2 g_{m4}}{-(\frac{1}{Z_L} + \frac{1}{r_{o1}} + \frac{1}{r_{o4}} + j\omega C_{gd1} + j\omega C_{gd4} + j\omega C_{ds1} + j\omega C_{ds4})} \quad (1)$$

where g_m refers to the transconductances of transistors M_1 and M_4 ; the C_{gd} and C_{ds} describe the parasitic gate-to-drain capacitor and drain-to-source capacitor, respectively; the r_o represents channel output resistance; the Z_L is used to characterize the load impedance. In addition, A_1 and A_2 are obtained by

$$A_1 = \frac{C_x(\frac{1}{r_{o1}} + j\omega C_{ds1} + j\omega C_{gd1})}{(C_x + C_{gs1} + C_{gd1})(\frac{1}{r_{o1}} + j\omega C_{ds1}) + (C_x + C_{gs1})j\omega C_{gd1} + C_{gd1}g_{m1}} \quad (2)$$

$$A_2 = \frac{C_y(\frac{1}{r_{o4}} + j\omega C_{ds4} + j\omega C_{gd4})}{(C_y + C_{gs4} + C_{gd4})(\frac{1}{r_{o4}} + j\omega C_{ds4}) + (C_y + C_{gs4})j\omega C_{gd4} + C_{gd4}g_{m4}} \quad (3)$$

where g_{m1} and g_{m4} are biased by V_a and V_b , respectively, which are generated by a 7-bit DAC. According to (1), it can be observed that the voltage gain is proportional to the

difference between V_a and V_b ; that is, the greater the difference between the two, the higher the gain. Based on this, to achieve the gain tuning of the VGA, V_a should not be equal to V_b . Furthermore, when setting V_a less than V_b , from (1), the maximum gain tuning range $\Delta G_{\max}$ can be derived as

$$\Delta G_{\max} = \frac{A_1 g_{m1,\min} - A_2 g_{m4,\max}}{A_1 g_{m1,\max} - A_2 g_{m4,\min}} \quad (4)$$

where $g_{m,\min}$ and $g_{m,\max}$ are the transconductances of transistors biased in minimum and maximum control voltages. It should be pointed out that since the amplifier gain is in decibels, the voltage gain should be converted into decibels, after which the logarithmic operation is performed. Based on this, the normal difference operation becomes division when placed in the logarithmic operation. Therefore, the final derivation of the gain tuning range appears as a ratio. In addition, it is worth mentioning that the C_{gd} is not ignored but neutralized based on the proposed topology in deriving Equations (1)–(4). The detailed proofs of Equations(1)–(4) are presented in Appendix A.

Figure 3. (a) Simplified schematic of the proposed variable gain stage and (b) its half-side small-signal equivalent circuit.

Then, based on (4), the gain resolution G_r of the VGA can be calculated as

$$G_r = \frac{\Delta G_{\max}}{2^n} = \frac{1}{2^n} \cdot \frac{(A_1 g_{m1,\min} - A_2 g_{m4,\max})}{(A_1 g_{m1,\max} - A_2 g_{m4,\min})} \quad (5)$$

where n is the control bits of the DAC. According to (4) and (5), the proposed asymmetric capacitor-based reconfigurable technique provides a new method to configure $\Delta G_{\max}$ and G_r by adjusting the coefficients A_1 and A_2 . Meanwhile, in order to keep the maximum gain of the VGA, it is needed to set $A_2 \approx 1$. As shown in Figure 4a,b, the conventional methods are only obtained $\Delta G_{\max}$ and G_r by controlling transconductance g_m of the transistors, whereas the proposed technique achieves another dimension for $\Delta G_{\max}$ and G_r control. When A_1 is varied from 1 to 0, $\Delta G_{\max}$ and G_r will be reconfigured. When the asymmetric capacitors C_x and C_y are designed to be greater than 1000 fF across 20–30 GHz, it can be calculated from (2) and (3) that the values of the coefficients A_1 and A_2 are approximately equal to one. Conversely, when they are smaller than 1000 fF, the values of A_1 and A_2 will

be less than one. Thus, the gain tuning range and gain step can be reconfigured, which is adjusted to capacitors C_x and C_y .

Figure 4. (a) Conventional methods to obtain $\Delta G_{\max}$ and G_r ; (b) a new method to configure $\Delta G_{\max}$ and G_r with proposed asymmetric capacitor-based reconfigurable technique; (c) with different values of C_x , simulated small-signal gain versus frequency at the maximum and minimum control states.

From what has been discussed above, the capacitance of C_x was adjusted by 2-bit switched-capacitor array, which could achieve 200/600/1000-fF; the C_y was designed to be a fixed value with a capacitance close to 1000 fF, so that the coefficient A_2 was approximately equal to one, as shown in Figure 3a. By configuring different C_x values, the simulated small-signal gains versus frequency are plotted in Figure 4c. Among them, in order to observe the reconfigurable effect more intuitively, only the maximum and minimum gain states are shown in the results. At the minimum gain control mode, the gain of the VGA changes greatly as C_x increases from 200 fF to 1000 fF, while the gain is almost the same at the maximum gain control mode. As a result, the reconfigurable gain tuning range and gain step can be realized. The simulation results shown in Figure 4c agree well with the theoretical analysis.

2.2. Phase Compensation Technique

For mm-wave VGAs, low additional phase shift during gain tuning is also a very important performance metric [9]. As mentioned before, many scholars have conducted extensive research to realize low phase variation during gain tuning. For VGAs with CS topologies, the parasitic capacitor C_{gd} has been discussed in detail [23] as the most important factor causing the phase variation. In order to eliminate C_{gd} , a method is widely used in amplifier design that introduces a positive feedback capacitor, which is called the capacitive cross-coupled neutralization (CCCN) technique [24]. This technique has the advantages of simple structure and obvious neutralization effect. However, its disadvantage is also obvious, that is, only good neutralization can be achieved in a narrow

frequency band, as the positive feedback capacitor changes with frequency. This greatly limits the design of this technique in wideband VGA circuit design. To overcome this problem, the active neutralization technique in the previous study [23] was employed. The core idea of this technique is to replace the positive feedback capacitor in the conventional CCCN technique with an active transistor. Since the auxiliary transistors (M_3 and M_4) and the main transistors (M_1 and M_2) have the same size, the C_{gd} of the two can be guaranteed to be the same with frequency changes, thus achieving good neutralization in the wide frequency band.

Figure 5 plots the simulated maximum phase variation in the classic and proposed active neutralization-based CS VGAs across 20–30 GHz under the same gain adjustment range. Both simulations were conducted based on the same circuit configuration. Across 20–30 GHz, the maximum deviation of the phase variation in the proposed VGA with active neutralization technique was below 0.3° during gain tuning. In contrast, the maximum phase variation results for the two classic CS VGAs were relatively large. Among them, one VGA with conventional CCCN technique exhibited the maximum phase variation of 1.6° , while another VGA without any neutralization techniques showed 8.6° phase variation at 30 GHz. These results fully illustrate two points: (1) the proposed VGA with active neutralization technique can effectively eliminate C_{gd} and achieve low phase variation; (2) good phase compensation can be realized in the wide frequency band, which is very suitable for broadband VGA design.

Figure 5. Simulated maximum phase variation in the classic CS VGAs and the proposed active neutralization-based CS VGA across 20–30 GHz under the same gain adjustment range.

3. Measurement Results

The proposed reconfigurable digitally controlled CS VGA was fabricated in a 65 nm CMOS process, and its die micrograph is presented in Figure 6. In the case of not including PAD, the core area of this chip was $0.758 \text{ mm} \times 0.23 \text{ mm}$. The two-stage VGA had a total power consumption of 98 mW with a 1 V supply, and the selection of 1 V supply voltage followed the vendor's recommendation under the corresponding process node. It is worth mentioning that, to achieve active neutralization, the auxiliary pairs in the proposed structure were on, which consumed slightly extra power to maintain the same gain. Even so, the total power consumption of the variable gain stage with the DAC was only 29 mW (including auxiliary pairs). The VGA presented in this paper consumed relatively high power consumption, which is because it achieved large output power. If a system does not need such high output power, the bias voltage of the output stage can be decreased, and the total dc power consumption of the proposed VGA would be reduced accordingly.

Figure 6. Micrograph of the proposed VGA.

The VGA gain was controlled by V_a and V_b , which were generated by the designed seven-bit DAC. The measured 32 states of gains under different control modes are shown in Figures 7a, 8a and 9a, respectively. It can be observed that the proposed VGA achieved a 12.2/9.2/6.1 dB gain tuning range, respectively, when the bias voltage of Ctr1 and Ctr2 were configured from 11 to 10 and then to 00 (C_x varying from 1000 to 200 fF, stepping 400 fF). Implementation of a 6.1 dB gain tuning range was aimed to insert loss compensation of PSs in phased array systems. Implementation of a 12.2 dB gain tuning range was intended for gain tuning in each element to suppress the sidelobes. As for the intermediate state, it was a compromise that was reserved according to actual design requirements. Meanwhile, the peak gain remained basically constant with the changes in C_x . The measured 3 dB bandwidth was as wide as 7.6 GHz, from 21.4 to 29 GHz, with an approximately 13 dB peak gain.

Figure 7. Based on $C_x = 1000$ fF, $C_y = 1000$ fF (Ctr1 = 1 V, Ctr2 = 1 V): (a) measured 32 gain states versus frequency and (b) its corresponding 31 gain resolutions versus frequency; (c) measured S11 and S22 versus frequency at 32 control states.

Figure 8. Based on $C_x = 600$ fF, $C_y = 1000$ fF (Ctr1 = 1 V, Ctr2 = 0 V): (a) measured 32 gain states versus frequency and (b) its corresponding 31 gain resolutions versus frequency; (c) measured S11 and S22 versus frequency at 32 control states.

Figure 9. Based on $C_x = 200$ fF, $C_y = 1000$ fF ($\text{Ctr1} = 0$ V, $\text{Ctr2} = 0$ V): (a) measured 32 gain states versus frequency and (b) its corresponding 31 gain resolutions versus frequency; (c) measured S11 and S22 versus frequency at 32 control states.

To further achieve the ultrahigh average sidelobe suppression ratio of the beamforming to ensure beamforming quality and chain data rate, the VGA was suggested to achieve a gain step of less than 0.5 dB [10]. As for insertion loss compensation of PSs, higher gain steps were also required, to avoid introducing extra gain errors. Based on the above considerations, the proposed VGA was designed to have a 0.4/0.3/0.2 dB gain resolution, respectively. Achieving such a high-precision gain step control, it was necessary to design a high-precision DAC. According to (5) and the measured gain tuning range, the calculation results of the three gain resolutions are as follows:

$$G_{r\max} = \frac{\Delta G_{\max}}{2^n} = \frac{G_{\max} - G_{\min}}{2^6} = \frac{12.75 - 0.6}{2^6} \approx 0.4 \quad (6)$$

$$G_{r\text{mean}} = \frac{\Delta G_{\max}}{2^n} = \frac{G_{\max} - G_{\min}}{2^6} = \frac{12.9 - 3.7}{2^6} \approx 0.3 \quad (7)$$

$$G_{r\min} = \frac{\Delta G_{\max}}{2^n} = \frac{G_{\max} - G_{\min}}{2^6} = \frac{13 - 6.9}{2^6} \approx 0.2 \quad (8)$$

Furthermore, the three configurations for the min, mean, and max gain step versus the six-bit binary control word overall frequency band are plotted in Figures 7b, 8b and 9b, respectively. The proposed VGA basically realized three reconfigurable gain steps of 0.4/0.3/0.2 dB, respectively. Then, the measured input return loss (S11) and output return loss (S22) of the VGA for the different configurations are plotted in Figures 7c, 8c and 9c, respectively. It can be seen from the results that changing the capacitance of C_x will slightly affect the offset of S11, which, due to the C_x , will slightly change the imaginary part of the source impedance. Since the output stage was a fixed gain stage, S22 basically remained unchanged versus 32 control words. In addition, it is worth mentioning that, to achieve wideband matching and compact layout, the transformer-based high-order matching networks were adopted. By adjusting the coupling coefficient k of the primary and secondary coils, the values of resonance frequency (ω_L and ω_H) could be adjusted, thereby realizing the adjustment of the bandwidth [25]. Figure 10 presents the measured small-signal gains versus 32 gain modes at 25.4 GHz, which verifies that the proposed VGA achieves reconfigurable gain tuning range and gain resolution, in addition to realizing linear gain control.

The RMS phase error was used to characterize the phase variation in the VGA. The specific formula for calculating RMS phase error is expressed as

$$\text{RMS Phase Error} = \sqrt{\frac{1}{N} \sum_{i=1}^N |\theta_i - \theta_{\text{ave}}|^2} \quad (9)$$

where θ_i is the phase at the i state, and θ_{ave} is the average of the phases of all states. In this paper, the phase was extracted from the argument of S21. The RMS phase errors for all gain states were measured by taking the maximum gain state as a reference, and they are shown in Figure 11a. At the maximum gain tuning range mode, the measured RMS

phase error was 1.7° at 23.4 GHz. Across 20–30 GHz, the measured RMS phase error was less than 5.5° . At the medium gain tuning range mode (0.3 dB gain step), the measured minimum RMS phase error was 0.5° at 25.2 GHz. Across 20–30 GHz, the measured RMS phase error was less than 2.4° . At the finest gain step control condition, the RMS phase error measured across 20–30 GHz was lower than 1.9° . At 30 GHz, a minimum phase error of 0.22° was achieved. Meanwhile, under the maximum gain state, the OP_{1dB} was up to 8.6 dBm at 25 GHz, as plotted in Figure 11b.

Figure 10. Measured gains versus gain mode under different control modes at 25.4 GHz.

Figure 11. (a) Measured RMS phase errors versus frequency at different control modes; (b) measured large signal performance of the VGA at 25 GHz.

Table 1 summarizes the performance of this research and compares it to prior studies. The proposed VGA is the only one that can reconstruct gain tuning range and gain resolution, which will greatly increase the flexibility of phased array systems. Additionally, it is the only one that adopts stackless transistor topology, thus achieving the lowest supply voltage, compared with other state-of-the-art multiple-stack transistor structures.

Table 1. Performance summary and comparison of the VGAs.

	This Study	ISSCC 2017 [11]	RFIC 2018 [12]	MWCL 2019 [14]	TMTT 2021 [15]
Technology	65 nm CMOS	40 nm CMOS	65 nm CMOS	65 nm CMOS	55 nm CMOS
Topology	Stackless	Two-stack	Two-stack	Two-stack	Two-stack
Supply (V)	1	1.1	1.2	1.2	1.3
Freq (GHz)	21.4–29	26–36	27–42	30–34.5	6.5–12
S11 (dB)	−9~−5	−20~−10	−30~−4	−28~−11	−14~−36
S22 (dB)	−17~−13	−7~−6	−50~−5	−30~−10	−14~−35
Peak gain (dB)	13	22.4	9.6	20.8	20.7
ΔG (dB)	12.2/9.2/6.1	8	7.5	10.6	18
Gain resolution (dB)	0.4/0.3/0.2	1	0.5	20.1	N/A
RMS phase error (°)	<1.9/2.4/5.5	<6 *	<3.5	<8 **	<4.5
OP1 dB (dBm)	8.6	13.7	2.5	−0.6 #	7.5 #
P _{DC} (mW)	98	30.3	15.6	26.7	75
Core Area (mm ²)	0.174	0.23	0.083	0.2	0.98

* Estimated from measurement results; ** phase variation; # calculated from IP_{1dB} with gain.

4. Conclusions

A 21.4–29 GHz reconfigurable digitally controlled VGA based on stackless CS structure with novel asymmetric capacitor-based reconfigurable and active neutralization phase compensation techniques was introduced. The proposed VGA achieved a 12.2/9.2/6.1 dB gain tuning range with a 0.4/0.3/0.2 dB gain step while maintaining the peak gain constant. At the finest gain step mode, the measured RMS phase error was <1.9° across 20–30 GHz. At 30 GHz, a minimum phase error of 0.22° was achieved. At the maximum gain state, it achieved a measured 13 dB peak gain and 8.6 dBm OP_{1dB}. The measurement characteristics demonstrate the proposed VGA is suitable for 5G mm-wave NR phased array beamformers that require reconfigurable gain tuning range and gain step with low phase variation.

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Appendix A

Derivations of Equations (1)–(4)

Figure A1 shows a small-signal equivalent circuit of a common source (CS) amplifier with parasitic elements when the effect of asymmetric capacitors is considered.

According to Kirchhoff's current law (KCL) and Kirchhoff's voltage law (KVL), the following equations can be obtained:

$$\begin{cases} (V_{in} - V_x)sC_x = sC_{gs1}V_x + (V_x - V_{out})sC_{gd1} \\ (V_x - V_{out})sC_{gd1} = g_{m1}V_x + (\frac{1}{r_{o1}} + sC_{ds1})V_{out} \end{cases} \quad (A1)$$

$$\begin{cases} V_{in}sC_x = s(C_x + C_{gs1} + C_{gd1})V_x - V_{out}sC_{gd1} \\ V_x(sC_{gd1} - g_{m1}) = (\frac{1}{r_{o1}} + sC_{ds1} + sC_{gd1})V_{out} \end{cases} \quad (A2)$$

$$V_{in}sC_x = s(C_x + C_{gs1} + C_{gd1})\frac{1}{r_{o1}} + sC_{gd1} + sC_{ds1}V_{out} - V_{out}sC_{gd1} \quad (A3)$$

$$\begin{aligned} V_{in}sC_x(sC_{gd1} - g_{m1}) &= \left[s(C_x + C_{gs1} + C_{gd1})(\frac{1}{r_{o1}} + sC_{ds1}) + s(C_x + C_{gs1} + C_{gd1})sC_{gd1} - sC_{gd1}(sC_{gd1} - g_{m1}) \right] V_{out} \\ &= \left[s(C_x + C_{gs1} + C_{gd1})(\frac{1}{r_{o1}} + sC_{ds1}) + s(C_x + C_{gs1})sC_{gd1} + (sC_{gd1})^2 - (sC_{gd1})^2 + sC_{gd1}g_{m1} \right] V_{out} \\ &= \left[s(C_x + C_{gs1} + C_{gd1})(\frac{1}{r_{o1}} + sC_{ds1}) + s(C_x + C_{gs1})sC_{gd1} + sC_{gd1}g_{m1} \right] V_{out} \end{aligned} \quad (A4)$$

$$\begin{aligned} G_{asymmetric} &= \frac{V_{out}}{V_{in}} = \frac{sC_x(sC_{gd1} - g_{m1})}{s(C_x + C_{gs1} + C_{gd1})(\frac{1}{r_{o1}} + sC_{ds1}) + s(C_x + C_{gs1})sC_{gd1} + sC_{gd1}g_{m1}} \\ &= \frac{C_x(sC_{gd1} - g_{m1})}{(C_x + C_{gs1} + C_{gd1})(\frac{1}{r_{o1}} + sC_{ds1}) + (C_x + C_{gs1})sC_{gd1} + C_{gd1}g_{m1}} \end{aligned} \quad (A5)$$

Figure A1. Small-signal equivalent circuit with asymmetric capacitor C_x .

Figure A2 shows the small-signal equivalent circuit of a CS amplifier with parasitic elements when the effect of asymmetric capacitors is not considered.

Figure A2. Small-signal equivalent circuit without asymmetric capacitor C_x .

According to Kirchhoff's current law (KCL) and Kirchhoff's voltage law (KVL), it can be derived that

$$g_{m1}V_{in} - (V_{in} - V_{out})sC_{gd1} = \frac{-V_{out}}{r_{o1}} - V_{out}sC_{ds1} \quad (A6)$$

In order to facilitate the operation, let $Av = V_{out}/V_{in}$. Then, Equation (A6) can be simplified to

$$g_{m1} - (1 - Av)sC_{gd1} = \frac{-Av}{r_{o1}} - AvsC_{ds1} \quad (A7)$$

$$g_{m1}r_{o1} - sC_{gd1}r_{o1} + AvsC_{gd1}r_{o1} = -Av - AvsC_{ds1}r_{o1} \quad (A8)$$

$$g_{m1}r_{01} - sC_{gd1}r_{01} = -Av - AvsC_{ds1}r_{01} - AvsC_{gd1}r_{01} \quad (A9)$$

$$g_{m1}r_{01} - sC_{gd1}r_{01} = -Av(1 + sC_{ds1}r_{01} + sC_{gd1}r_{01}) \quad (A10)$$

$$Av = G_{symmetric} = \frac{V_{out}}{V_{in}} = \frac{j\omega C_{gd1} - g_{m1}}{(\frac{1}{r_{o1}} + j\omega C_{gd1} + j\omega C_{ds1})} \quad (A11)$$

In order to facilitate the operation, let:

$$A = j\omega C_{gd1} - g_{m1};$$

$$B = (C_x + C_{gs1} + C_{gd1})(1/r_{o1} + j\omega C_{ds1}) + (C_x + C_{gs1})j\omega C_{gd1} + C_{gd1}g_{m1};$$

$$C = (1/r_{o1} + j\omega C_{gd1} + j\omega C_{ds1}).$$

Then, Equation (A5) can be simplified to

$$G_{asymmetric} = \frac{V_{out}}{V_{in}} = \frac{C_x A}{B} \quad (A12)$$

Equation (A11) can be simplified to:

$$G_{symmetric} = \frac{V_{out}}{V_{in}} = \frac{A}{C} \quad (A13)$$

Based on Equations (A12) and (A13), A_1 is given by

$$A_1 = \frac{G_{asymmetric}}{G_{symmetric}} = \frac{C_x A}{B} \div \frac{A}{C} = \frac{C_x C}{B} \quad (A14)$$

$$= \frac{C_x (\frac{1}{r_{o1}} + j\omega C_{ds1} + j\omega C_{gd1})}{(C_x + C_{gs1} + C_{gd1})(\frac{1}{r_{o1}} + j\omega C_{ds1}) + (C_x + C_{gs1})j\omega C_{gd1} + C_{gd1}g_{m1}}$$

Similarly, A_2 is given by

$$A_2 = \frac{C_y (\frac{1}{r_{o4}} + j\omega C_{ds4} + j\omega C_{gd4})}{(C_y + C_{gs4} + C_{gd4})(\frac{1}{r_{o4}} + j\omega C_{ds4}) + (C_y + C_{gs4})j\omega C_{gd4} + C_{gd4}g_{m4}} \quad (A15)$$

According to Equations (A14) and (A15), Equation (A5) can be written as

$$G_{asymmetric} = A_1 G_{symmetric} = \frac{A_1 (j\omega C_{gd1} - g_{m1})}{(\frac{1}{r_{o1}} + j\omega C_{gd1} + j\omega C_{ds1})} \quad (A16)$$

Qualitatively analyzing Equation (A16), compared with the conventional symmetrical capacitor structure, the A_1 coefficient is generated by the voltage divider of the asymmetrical capacitor C_x . Therefore, if the capacitance of C_x is large (equivalent to short-circuit without voltage divider), A_1 is approximately equal to 1; on the contrary, if the capacitance of C_x is small, and there is a certain voltage divider, A_1 will be less than 1.

Figure A3a shows the half-side small-signal equivalent circuit of the proposed variable gain stage with asymmetric capacitors. Since it is a half-side circuit, V_{in} becomes one-half. According to the above derivation, coefficients A_1 and A_2 are introduced due to the influence of the asymmetric capacitor. Therefore, in order to express the derivation of Equation (1) more clearly and concisely, we first use the symmetrical capacitor structure to derive Equation (1). Based on Equation (A16), for the asymmetric capacitor structure, coefficients A_1 and A_2 should simply be added later to the numerator. Figure A3b presents the half-side small-signal equivalent circuit of the variable gain stage without asymmetric capacitors. According to Kirchhoff's current law (KCL) and Kirchhoff's voltage law (KVL), it can be derived that

$$(\frac{1}{2}V_{in} + -V_{out})sC_{gd1} = \frac{1}{2}g_{m1}V_{in} + +V_{out}(\frac{1}{r_{o1}} + sC_{ds1} + \frac{1}{Z_L} + sC_{ds4} + \frac{1}{r_{o4}}) + \frac{1}{2}g_{m4}V_{in} - + (V_{out} - \frac{1}{2}V_{in}-)sC_{gd4} \quad (A17)$$

$$\frac{1}{2}V_{in} + (sC_{gd1} - g_{m1}) + \frac{1}{2}V_{in} - (sC_{gd4} - g_{m4}) = V_{out}(\frac{1}{r_{o1}} + sC_{ds1} + \frac{1}{Z_L} + sC_{ds4} + \frac{1}{r_{o4}} + sC_{gd1} + sC_{gd4}) \quad (A18)$$

Since $\frac{1}{2}V_{in+} = -\frac{1}{2}V_{in-}$, the left side of Equation (A18) can be simplified to Equations (A19) and (A20), respectively.

$$\frac{1}{2}V_{in} + (sC_{gd1} - g_{m1}) + \frac{1}{2}V_{in} + (g_{m4} - sC_{gd4}) \quad (A19)$$

$$-\frac{1}{2}V_{in} - (sC_{gd1} - g_{m1}) + \frac{1}{2}V_{in} - (sC_{gd4} - g_{m4}) \quad (A20)$$

Since the two transistors are the same size, C_{gd} is the same ($C_{gd1} = C_{gd4}$), the two C_{gd} values can cancel each other, and Equations (A19) and (A20) can be further simplified as

$$-\frac{1}{2}V_{in} + (g_{m1} - g_{m4}) \quad (A21)$$

$$\frac{1}{2}V_{in} - (g_{m1} - g_{m4}) \quad (A22)$$

Then, substituting Equation (A21) into Equation (A18) yields

$$-\frac{1}{2}V_{in} + (g_{m1} - g_{m4}) = V_{out}(\frac{1}{r_{o1}} + sC_{ds1} + \frac{1}{Z_L} + sC_{ds4} + \frac{1}{r_{o4}} + sC_{gd1} + sC_{gd4}) \quad (A23)$$

$$\frac{V_{in+}}{2V_{out}} = \frac{-(\frac{1}{r_{o1}} + sC_{ds1} + \frac{1}{Z_L} + sC_{ds4} + \frac{1}{r_{o4}} + sC_{gd1} + sC_{gd4})}{(g_{m1} - g_{m4})} \quad (A24)$$

Similarly, substituting Equation (A22) into Equation (A18) yields

$$\frac{1}{2}V_{in} - (g_{m1} - g_{m4}) = V_{out}(\frac{1}{r_{o1}} + sC_{ds1} + \frac{1}{Z_L} + sC_{ds4} + \frac{1}{r_{o4}} + sC_{gd1} + sC_{gd4}) \quad (A25)$$

$$\frac{V_{in-}}{2V_{out}} = \frac{(\frac{1}{r_{o1}} + sC_{ds1} + \frac{1}{Z_L} + sC_{ds4} + \frac{1}{r_{o4}} + sC_{gd1} + sC_{gd4})}{(g_{m1} - g_{m4})} \quad (A26)$$

Then, Equations (A24)–(A26) are used to obtain

$$\frac{V_{in+} - V_{in-}}{2V_{out}} = -\frac{2(\frac{1}{r_{o1}} + sC_{ds1} + \frac{1}{Z_L} + sC_{ds4} + \frac{1}{r_{o4}} + sC_{gd1} + sC_{gd4})}{(g_{m1} - g_{m4})} \quad (A27)$$

Then, according to (A27), the voltage gain without asymmetric capacitors can be calculated by

$$G_{symmetric} = \frac{V_{out}}{V_{in+} - V_{in-}} = -\frac{(g_{m1} - g_{m4})}{(\frac{1}{r_{o1}} + sC_{ds1} + \frac{1}{Z_L} + sC_{ds4} + \frac{1}{r_{o4}} + sC_{gd1} + sC_{gd4})} \quad (A28)$$

Similarly, based on Equation (A16), when considering the asymmetric capacitors, coefficients A_1 and A_2 are simply added to the numerator, respectively, and Equation (A28) becomes

$$G_{asymmetric} = \frac{V_{out}}{V_{in+} - V_{in-}} \approx \frac{A_1g_{m1} - A_2g_{m4}}{-(\frac{1}{Z_L} + \frac{1}{r_{o1}} + \frac{1}{r_{o4}} + j\omega C_{gd1} + j\omega C_{gd4} + j\omega C_{ds1} + j\omega C_{ds4})} \quad (A29)$$

According to (A29), any voltage gain can be calculated by

$$G_1 = \frac{V_{out}}{V_{in+} - V_{in-}} = \frac{A_1g_{m1,1} - A_2g_{m4,1}}{-(\frac{1}{Z_L} + \frac{1}{r_{o1}} + \frac{1}{r_{o4}} + j\omega C_{gd1} + j\omega C_{gd4} + j\omega C_{ds1} + j\omega C_{ds4})} \quad (A30)$$

$$G_2 = \frac{V_{out}}{V_{in} + -V_{in-}} = \frac{A_1 g_{m1,2} - A_2 g_{m4,2}}{-\left(\frac{1}{Z_L} + \frac{1}{r_{o1}} + \frac{1}{r_{o4}} + j\omega C_{gd1} + j\omega C_{gd4} + j\omega C_{ds1} + j\omega C_{ds4}\right)} \quad (A31)$$

Moreover, since the amplifier gain is in decibels, G_1 and G_2 need to be converted to decibels. Therefore, Equations (A30) and (A31) are modified as

$$G_1(dB) = 20\lg\left(\frac{V_{out}}{V_{in} + -V_{in-}}\right) = 20\lg\left(\frac{A_1 g_{m1,1} - A_2 g_{m4,1}}{-\left(\frac{1}{Z_L} + \frac{1}{r_{o1}} + \frac{1}{r_{o4}} + j\omega C_{gd1} + j\omega C_{gd4} + j\omega C_{ds1} + j\omega C_{ds4}\right)}\right) \quad (A32)$$

$$G_2(dB) = 20\lg\left(\frac{V_{out}}{V_{in} + -V_{in-}}\right) = 20\lg\left(\frac{A_1 g_{m1,2} - A_2 g_{m4,2}}{-\left(\frac{1}{Z_L} + \frac{1}{r_{o1}} + \frac{1}{r_{o4}} + j\omega C_{gd1} + j\omega C_{gd4} + j\omega C_{ds1} + j\omega C_{ds4}\right)}\right) \quad (A33)$$

Based on Equations (A32) and (A33), the gain tuning range ΔG can be derived as $(G_1(dB) - G_2(dB))$ as follows:

$$\begin{aligned} \Delta G = G_1(dB) - G_2(dB) &= 20\lg\left(\frac{\left(\frac{A_1 g_{m1,1} - A_2 g_{m4,1}}{-\left(\frac{1}{Z_L} + \frac{1}{r_{o1}} + \frac{1}{r_{o4}} + j\omega C_{gd1} + j\omega C_{gd4} + j\omega C_{ds1} + j\omega C_{ds4}\right)}\right)}{\left(\frac{A_1 g_{m1,2} - A_2 g_{m4,2}}{-\left(\frac{1}{Z_L} + \frac{1}{r_{o1}} + \frac{1}{r_{o4}} + j\omega C_{gd1} + j\omega C_{gd4} + j\omega C_{ds1} + j\omega C_{ds4}\right)}\right)}\right) \\ &= \frac{A_1 g_{m1,1} - A_2 g_{m4,1}}{A_1 g_{m1,2} - A_2 g_{m4,2}} \end{aligned} \quad (A34)$$

Figure A3. (a) Half-side small-signal equivalent circuit of the proposed variable gain stage with asymmetric capacitors; (b) half-side small-signal equivalent circuit of the proposed variable gain stage without asymmetric capacitors.

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