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A Novel Carrier Scheme Combined with DPWM Technique in a ZVS Grid-Connected Three-Phase Inverter

Yi-Hung Liao *, Jiong-Ye Chen and Ying Zhou

Department of Electrical Engineering, National Central University, Taoyuan 320, Taiwan; a88769291@gmail.com (J.-Y.C.); ying6102@gmail.com (Y.Z.)
* Correspondence: yhungliao@ee.ncu.edu.tw; Tel.: +886-3-4227151 (ext. 35153)

Abstract: In this paper, a novel switching scheme using discontinuous pulse-width modulation (DPWM) for a zero-voltage switching (ZVS) grid-connected three-phase inverter is proposed. ZVS in the main and auxiliary switches was achieved. Moreover, the reverse recovery currents of the anti-parallel diodes in the main switches were suppressed. A circuit analysis was performed, and a simulation was carried out. Furthermore, a prototype of the ZVS grid-connected three-phase inverter was constructed to verify the effectiveness of the proposed PWM control scheme. Both the simulation and experimental results verified the validity of the proposed PWM control scheme.

Keywords: grid-connected three-phase inverter; zero-voltage switching (ZVS); reverse recovery current suppression; discontinuous pulse-width modulation (DPWM)

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1. Introduction

Three-phase inverters are widely utilized in PV systems, wind power generation, electrical vehicles, and uninterruptible power systems, etc. Especially, distributed grid-connected inverters play an important role in renewable energy generation systems as the interface between the renewable energy and the grid. The conventional six-switch three-phase inverter is a preferred topology with several advantages such as lower current stress and higher efficiency. However, the anti-parallel diodes of the six switches have a reverse recovery problem that causes many switching loss and electromagnetic interference problems.

Over the past few years, various soft-switching techniques for three-phase inverters have been studied [1–12]. Generally, the voltage of the DC link is periodically resonated to a zero voltage level to create soft-switching conditions, which causes the three-phase six switches achieve zero-voltage switching at the corresponding time. The typical method to achieve ZVS is by adding an auxiliary resonant circuit in the inverter [2]. According to the different locations of the auxiliary circuit, the soft-switching method of DC–AC voltage-source inverters can be classified into two categories: DC-side auxiliary circuit topologies [1–7] and AC-side auxiliary circuit topologies [8–11]. In DC-side auxiliary circuit topologies, an auxiliary circuit is inserted between the DC voltage source and the main six-switch bridge to achieve the zero-voltage condition. Generally speaking, according to the clamp capacitor location, the clamp capacitor can be in series with resonant inductance [1,2] or in series with the auxiliary switch [3–7] to achieve ZVS. If the clamp capacitor is in series with the auxiliary switch, the reverse recovery current of the anti-parallel diodes can be easily suppressed, but the switch voltage stress is high. If the clamp capacitor is in series with the resonant inductor, the switch voltage stress is equal to the DC link voltage. In addition, different PWM strategies for ZVS have been developed. The space-vector pulse-width modulation (SVPWM) control strategy has been utilized for ZVS in the literature [1–3,7], and the discontinuous pulse-width modulation (DPWM) control strategy has also been studied to achieve ZVS in the literature [12,13]. However, although there is no additional component added in the circuit [12], the inverter-side current is larger

and the current stress on the main switches is higher than that in the literature [1–7]. In addition, the filter design is more complicated due to the variable switching frequency operation. In [13], in order to unify the PWM methods for soft-switching active-clamping three-phase power converters, the edge-aligned PWM (EA-PWM) was proposed to simplify the control method. Nevertheless, the EA-PWM needs three-phase current sensors to obtain information on the filter's current polarities to achieve ZVS in the active switches. Moreover, the soft-switching condition is affected by the modulation index, which may reduce the ability to achieve ZVS in any modulation index.

In the DPWM control strategy, only two of three legs are switching at any time. Therefore, the switching loss and electromagnetic interference (EMI) can be reduced. In order to reduce the switching loss, in this paper, a carrier-based ZVS DPWM (CB-DPWM) control strategy was studied for grid-connected three-phase inverters. A simple saw-tooth carrier waveform with positive and negative slope rates was developed to achieve ZVS in both the main and auxiliary switches. Using this method, the auxiliary switch, S_7, control signal can be generated more easily compared with the literature [1,2]. In addition, the ZVS of the main and auxiliary switches can be obtained. Moreover, the reverse recovery current of the anti-parallel diodes in the main switches can also be reduced in the proposed modulation scheme. Furthermore, the voltage stress of main and the auxiliary switches was still equal to DC bus voltage.

The remaining contents of this paper are organized as follows. First, the circuit configuration and the operating principle of the proposed ZVS DPWM control strategy are described in Sections 2 and 3. Based on the proposed ZVS DPWM control strategy, simulation and experimental results are offered in Section 4 to verify the validity of the proposed control strategy for a ZVS grid-connected three-phase six-switch inverter. Finally, some conclusions are offered in Section 5.

2. Proposed Modulation Scheme

The circuit of the ZVS inverter is shown in Figure 1 [1,2]. The circuit topology is composed of a standard six-switch grid-connected inverter and an auxiliary resonant circuit that is connected with the distributed energy resources (DERs) in the DC side. In the auxiliary circuit, the auxiliary switch, S_7, is conducted most of the time during the switching period. While the auxiliary switch, S_7, is turned ON, the resonant inductor, L_r, is charged. While the auxiliary switch, S_7, is turned OFF, the energy stored in the resonant inductor, L_r, releases energy to the parasitic capacitors of the main switches. When the auxiliary switch, S_7, is switched once in a PWM period, both the main and auxiliary switches can achieve ZVS. In addition, the reverse recovery current of the main switches can be suppressed. Thus, the system's conversion efficiency can be increased.

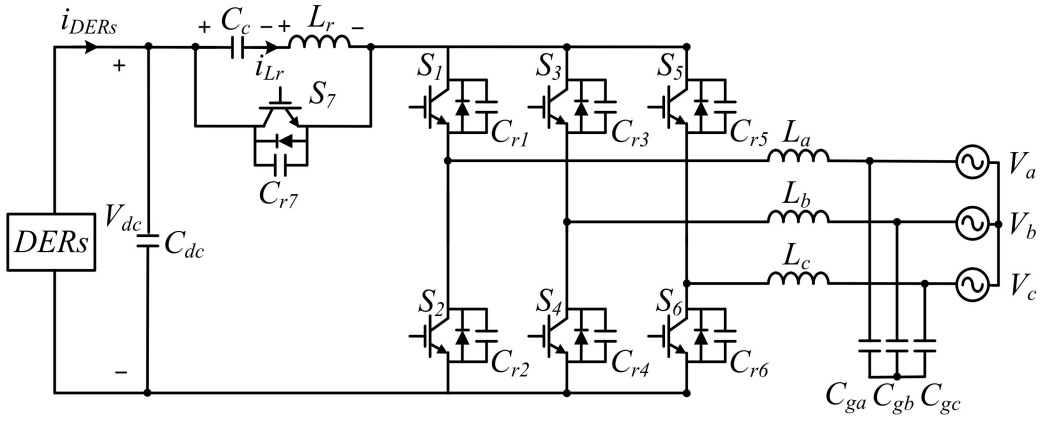


Figure 1. The circuit topology of the ZVS grid-connected inverter.

The proposed DPWM control strategy and corresponding carrier waveform are shown in Figure 2. In order to achieve zero-voltage switching and decrease the switching numbers of the main and auxiliary switches, a ZVS carrier-based PWM is proposed to reduce switching loss and improve energy conversion efficiency. The proposed control strategy judges three-phase DPWM control signals to determine the slope of the saw-tooth carrier waveform. When one of the three-phase DPWM control signals reaches high level (i.e., $V_{dc}/2$), the slope of the saw-tooth waveform is negative, and when one of the three-phase DPWM control signals reaches low level (i.e., $-V_{dc}/2$), the slope of the saw-tooth carrier waveform is positive.

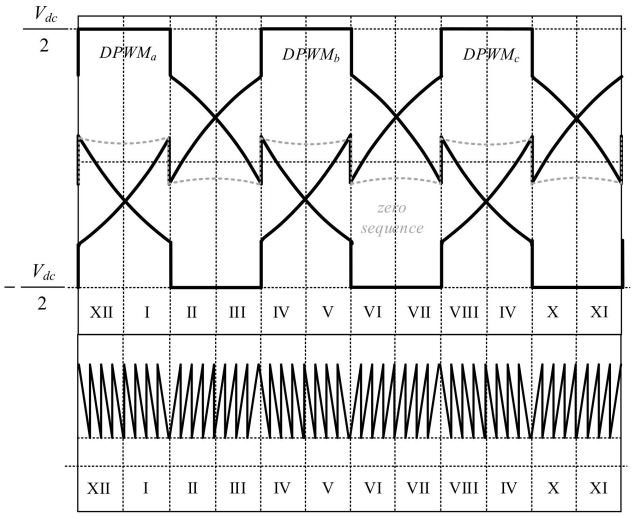


Figure 2. Proposed DPWM method and carrier waveform diagram.

In the proposed control scheme, the zero vectors, V_0 and V_7, were selected as shown in Figure 3, and the auxiliary switch, S_7, control signal is determined to achieve ZVS in the main S_1–S_6 and S_7 switches. The generation of the S_7 signal is mainly based on the dead-time among the three legs in the three-phase inverter as shown in Figure 4. Take sector I and sector II as an example. In the control signal in sector I, one of the three-phase DPWM control signals reaches high level, i.e., DPWMa. Then, the negative slope of the saw-tooth waveform is utilized, and the control signals are generated as shown in Figure 4a. In the meantime, the zero vector, V_7, is naturally selected. If the dead-time of any two legs occur at the same time, the S_7 control signal is established. In the same manner, the corresponding control signals in sector II are shown in Figure 4b, and the positive slope of the saw-tooth waveform is utilized, the zero vector, V_0, is naturally selected, and S_7 control signal is also established.

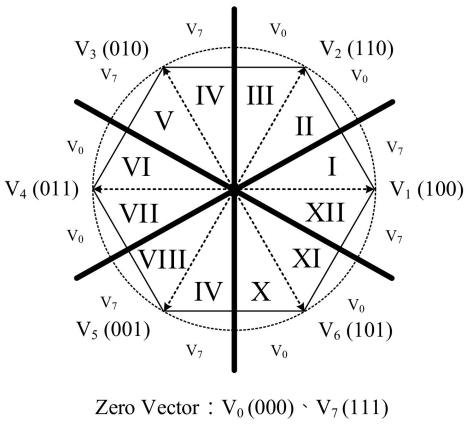


Figure 3. Sectors of the space-vector diagram.

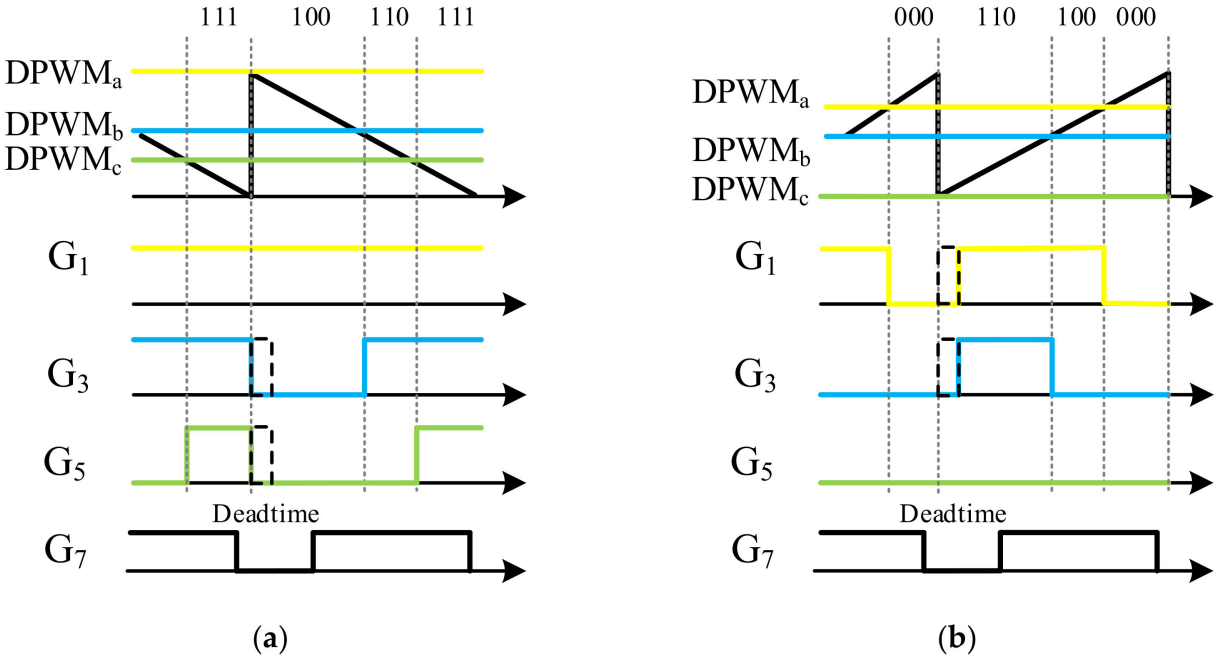


Figure 4. The proposed DPWM scheme: (**a**) sector I; (**b**) sector II.

3. Analysis of DPWM Grid-Connected Inverter

According to the proposed DPWM method and the zero vector selection in Figures 2–4, there are twelve sectors in a line-cycle period. The twelve-sector modulation can be operated in sequence. Take sector I as an example and assume a three-phase current: $i_a > 0 > i_b > i_c$. For a convenient explanation of how the proposed modulation scheme works, the following assumptions were made to simplify the analysis of the grid-connected ZVS inverter;

(1) The main switches, S_1–S_6, and auxiliary switch, S_7, were considered to be ideal switches connected with corresponding anti-parallel diodes;
(2) All of the parasitic capacitances, C_{r1}–C_{r7}, paralleled the switches S_1–S_7, respectively;
(3) In this architecture, the current ripple of i_a, i_b, and i_c in grid-side inductor was small, and i_a, i_b, and i_c were considered as constant current sources in a switching period;
(4) The capacitance of the clamping capacitor, C_c, was so large that the voltage ripple across it was relatively small; thus, v_{Cc} can be regarded as a voltage source;
(5) The resonant frequency of C_c and L_r was much lower than the operation frequency of the inverter. In this paper, the filter resonant frequency was 707 Hz, and the operation switching frequency was 18 kHz;
(6) In order to explain the reverse recovery current of switch body diode, i_{cex}, $x \in \{1, 2, \ldots, 7\}$ denotes the switch current including the parasitic capacitor current, and i_{sx}, $x \in \{1, 2, \ldots, 7\}$ denotes the switch current except the parasitic capacitor current.

The circuit operation, equivalent circuit, and theoretical waveform are illustrated in Figures 5–7, respectively. The following are the working stages of the proposed ZVS DPWM control strategy for grid-connected three-phase inverters.

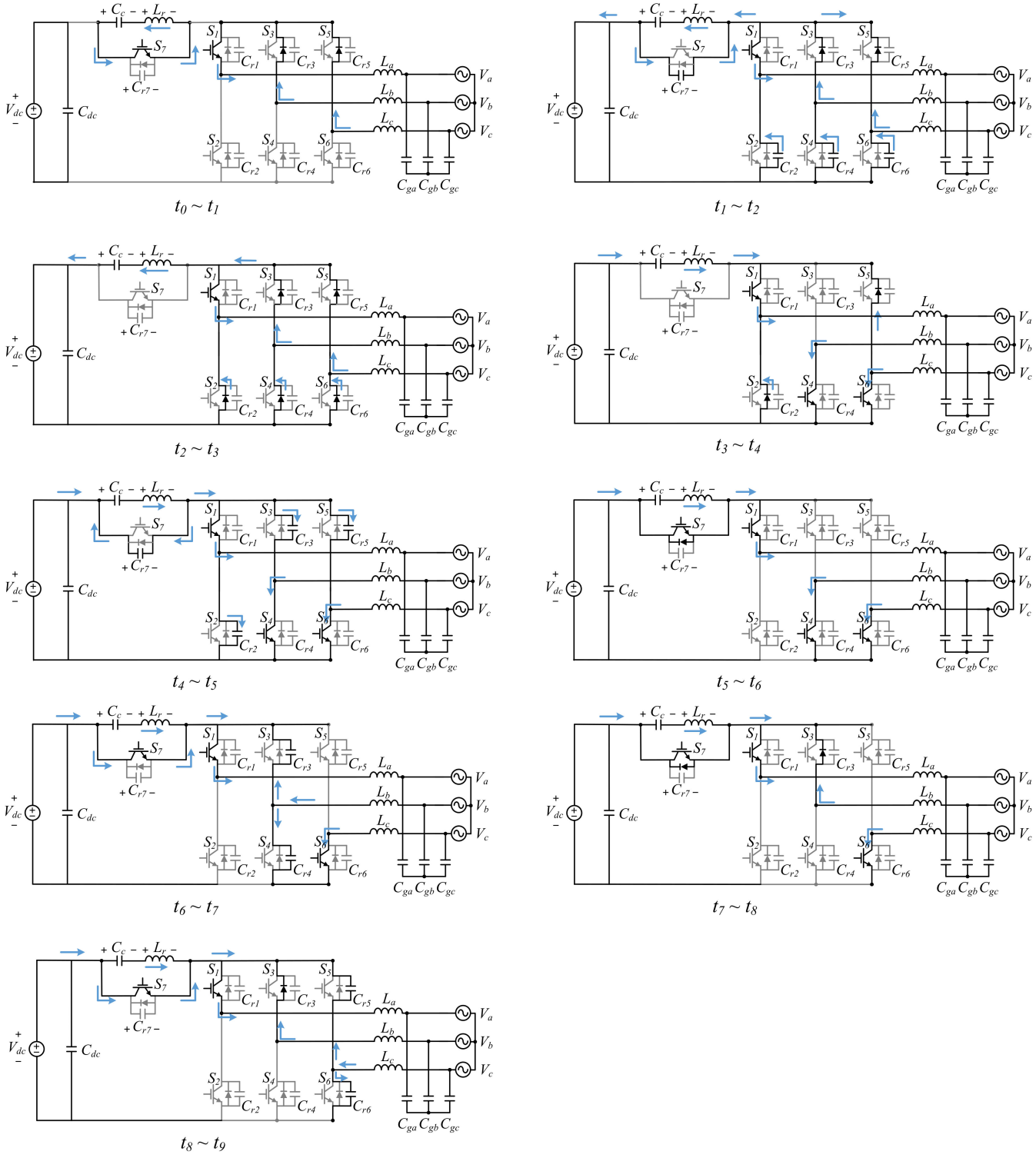


Figure 5. The operation stages of the proposed ZVS DPWM control strategy in sector I.

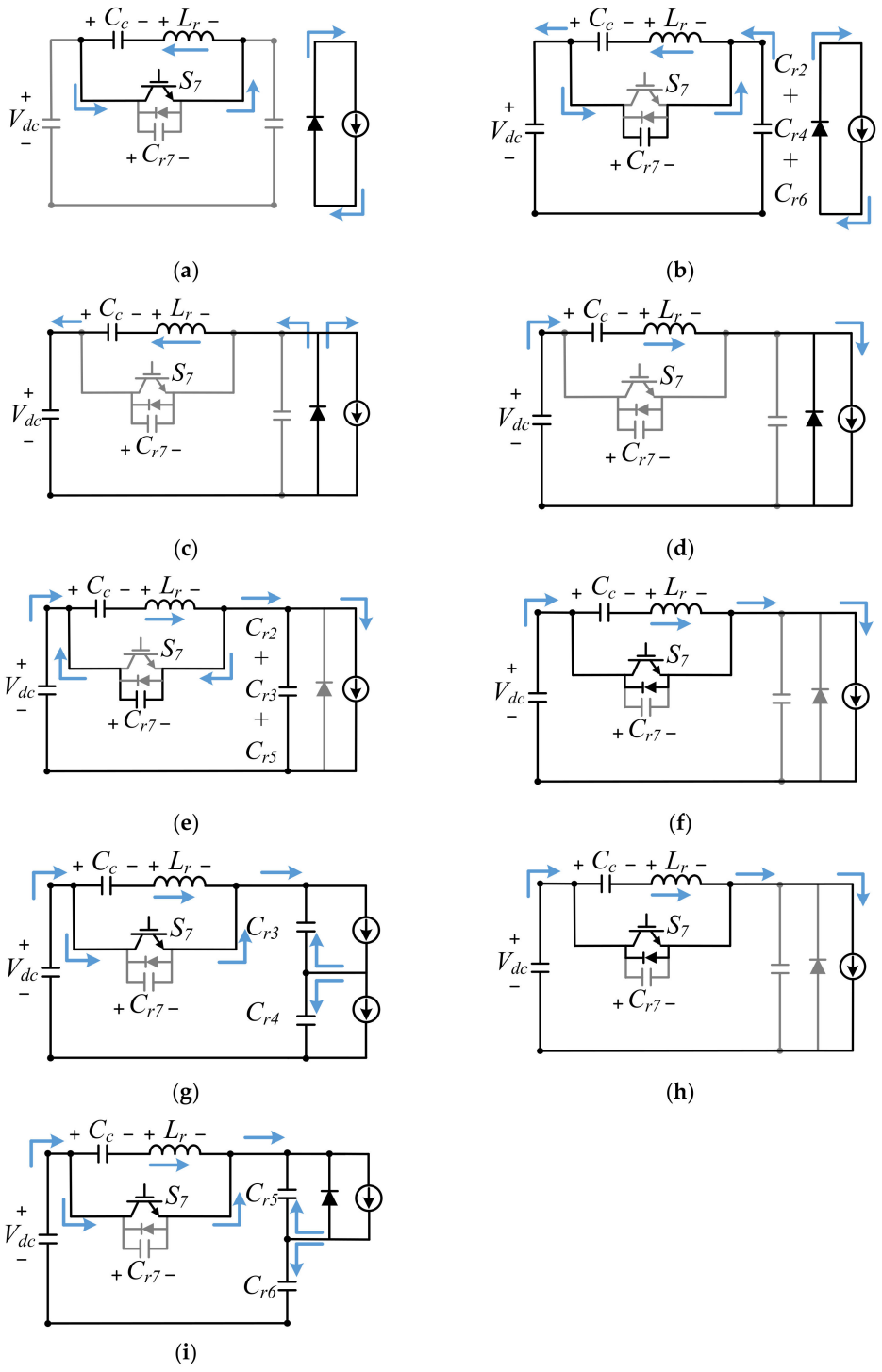


Figure 6. The equivalent circuits of the operation stages of the proposed ZVS grid-connected inverter. (**a**) t_0~t_1. (**b**) t_1~t_2. (**c**) t_2~t_3. (**d**) t_3~t_4. (**e**) t_4~t_5. (**f**) t_5~t_6. (**g**) t_6~t_7. (**h**) t_7~t_8. (**i**) t_8~t_9.

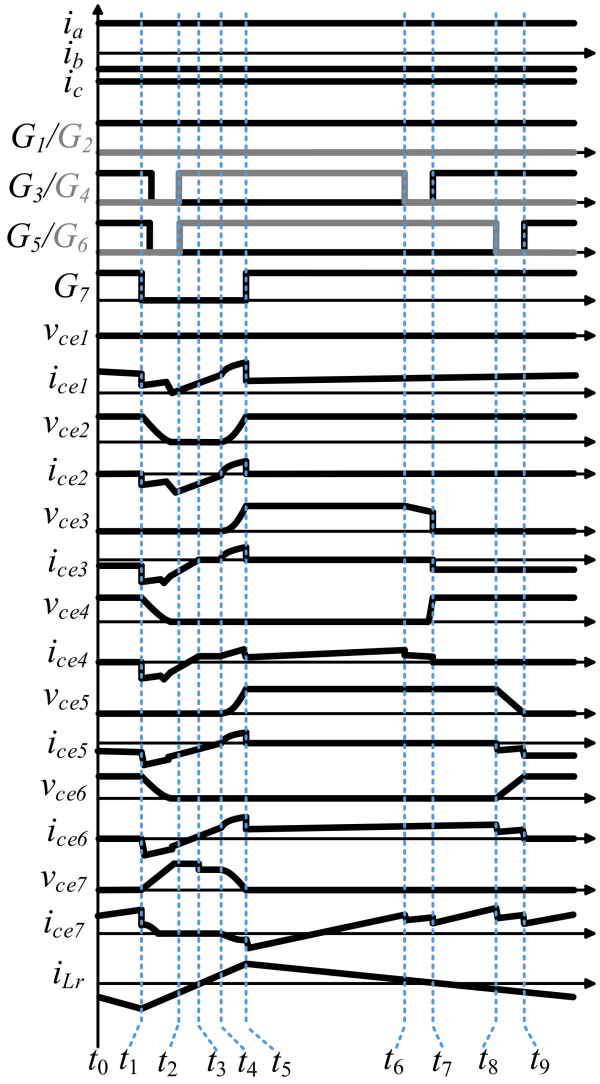


Figure 7. The theoretical waveform of the proposed ZVS DPWM control strategy.

State 1 ($t_0 \sim t_1$):

The circuit is operated at vector state 111. The main switch, S_1, auxiliary switch, S_7, and the anti-parallel diodes, D_3 and D_5, are ON. The inverter is operated at zero vector. The resonant inductor, L_r, is charged by the clamping voltage, v_{Cc}. The equivalent circuit is shown in Figure 6a, and the relationship between L_r and C_c is obtained as follows:

$$v_{Lr} = L_r \frac{\mathrm{d}i_{Lr}}{\mathrm{d}t} = -v_{Cc} \tag{1}$$

State 2 ($t_1 \sim t_2$):

The resonant inductor, L_r, resonates with C_{r2}, C_{r4}, C_{r6}, and C_{r7}. The auxiliary switch, S_7, is turned OFF at t_1 under the ZVS condition due to the resonance where C_{r2}, C_{r4}, and C_{r6} is discharging and C_{r7} is charging in this moment. During this state, switches S_3 and S_5 are turned OFF. The energy stored in inductor, L_r, is returned to the DC capacitor. The equivalent circuit is shown in Figure 6b, and the relationship between C_c, C_r, and L_r is expressed as follows:

$$v_{Lr} = L_r \frac{\mathrm{d}i_{Lr}}{\mathrm{d}t} = (-v_{Cc} + V_{dc} - v_{Cr}) \tag{2}$$

$$-3C_r \frac{\mathrm{d}v_{Cr}}{\mathrm{d}t} + C_{r7} \frac{\mathrm{d}(V_{dc} - v_{Cr})}{\mathrm{d}t} = -i_{Lr} \tag{3}$$

State 3 ($t_2 \sim t_3$):

At this time, the circuit is operated at vector state 100. The voltages of C_{r2}, C_{r4}, and C_{r6} are discharged to zero, and the voltage of C_{r7} is charged to V_{dc}. The anti-parallel diodes D_2, D_3, D_4, D_5, and D_6 are ON. The switches S_4 and S_6 are turned ON under ZVS conditions at instant time t_2, and the resonant inductor, L_r, suppresses the reverse recovery current of the anti-parallel diode, D_3. The equivalent circuit is shown in Figure 6c, and the relationship between i_{Lr} and v_{Cc} is derived as follows:

$$v_{Lr} = L_r \frac{\mathrm{d}i_{Lr}}{\mathrm{d}t} = -(v_{Cc} - \mathrm{V}_{dc}) \tag{4}$$

State 4 ($t_3 \sim t_4$):

The main switches S_1, S_4, and S_6 remain ON, and the resonant inductor, L_r, suppresses the reverse recovery current of the anti-parallel diodes, D_2 and D_5. The power flows from the DC side to the AC side. The equivalent circuit is shown in Figure 6d, and the relationship between i_{Lr} and v_{Cc} is expressed as follows:

$$v_{Lr} = L_r \frac{\mathrm{d}i_{Lr}}{\mathrm{d}t} = -(v_{Cc} - \mathrm{V}_{dc}) \tag{5}$$

State 5 ($t_4 \sim t_5$):

The resonant inductor, L_r, resonates with C_{r2}, C_{r3}, C_{r5}, and C_{r7}, and the anti-parallel diode, D_7, is ready to be turned ON. During this state, C_{r2}, C_{r3}, and C_{r5} are charged, and C_{r7} is discharged. The power still flows from the DC side to the AC side. The equivalent circuit is shown in Figure 6e, and the relationship between the voltage and current can be obtained as follows:

$$v_{Lr} = L_r \frac{\mathrm{d}i_{Lr}}{\mathrm{d}t} = (-v_{Cc} + V_{dc} - v_{Cr}) \tag{6}$$

$$3C_r \frac{\mathrm{d}v_{Cr}}{\mathrm{d}t} + i_{La} = C_{r7} \frac{\mathrm{d}(V_{dc} - v_{Cr})}{\mathrm{d}t} + i_{Lr} \tag{7}$$

State 6 ($t_5 \sim t_6$):

At this state, the circuit is still operated at vector state 100, and the main switches, S_1, S_4, and S_6, are ON. The auxiliary switch, S_7, is turned ON under the ZVS condition. The voltage of the clamping capacitor, v_{Cc}, is charged by the resonant inductor current, i_{Lr}, and the power flows from the DC side to the AC side. The equivalent circuit is shown in Figure 6f, and the relationship between i_{Lr} and v_{Cc} is as follows:

$$v_{Lr} = L_r \frac{\mathrm{d}i_{Lr}}{\mathrm{d}t} = -v_{Cc} \tag{8}$$

State 7 ($t_6 \sim t_7$):

At this state, the circuit is operated at vector state 100. The phase current i_b discharges voltage v_{Cr3} and charges voltage v_{Cr4}. The main switch, S_4, is turned OFF under the ZVS condition, and the power flows from the DC side to the AC side. The equivalent circuit is shown in Figure 6g, and the relationship between the voltage and current can be derived as follows:

$$v_{Lr} = L_r \frac{\mathrm{d}i_{Lr}}{\mathrm{d}t} = -v_{Cc} \tag{9}$$

$$i_{Lb} = -C_{r3} \frac{\mathrm{d}v_{Cr3}}{\mathrm{d}t} + C_{r4} \frac{\mathrm{d}v_{Cr4}}{\mathrm{d}t} \tag{10}$$

State 8 ($t_7 \sim t_8$):

At this state, the circuit is operated at vector state 110. The main switches, S_1 and S_6, the auxiliary switch, S_7, and the anti-parallel diode, D_3, are in the conducting state. The

power flows from the DC side to the AC side. The equivalent circuit is shown in Figure 6h, and the relationship between i_{Lr} and v_{Cc} is expressed as follows:

$$v_{Lr} = L_r \frac{\mathrm{d}i_{Lr}}{\mathrm{d}t} = -v_{Cc} \tag{11}$$

State 9 ($t_8 \sim t_9$):

At this state, the circuit is still operated at vector state 110. The phase current i_c discharges voltage v_{Cr5} and charges voltage v_{Cr6}. The main switch, S_6, is turned OFF under the ZVS condition, and the power flows from the DC side to the AC side. The equivalent circuit is shown in Figure 6i. After this stage, the circuit operation returns to the first stage and starts a new cycle. The relationship between the voltage and current can be obtained as follows:

$$v_{Lr} = L_r \frac{\mathrm{d}i_{Lr}}{\mathrm{d}t} = -v_{Cc} \tag{12}$$

$$i_{Lc} = -C_{r5} \frac{\mathrm{d}v_{Cr5}}{\mathrm{d}t} + C_{r6} \frac{\mathrm{d}v_{Cr6}}{\mathrm{d}t} \tag{13}$$

4. Simulation and Experimental Results

After the explanation of the theoretical analysis of the proposed ZVS PWM control scheme, the simulation and experiment were carried out to verify the validity the proposed ZVS PWM control scheme. Hence, the system parameters of the grid-connected ZVS inverter are listed in Table 1 for the simulation and experiment.

Table 1. System parameters for the simulation and experiment.

Symbol	Description	Value
V_a, V_b, V_c	AC grid phase/line voltage	127/220 V_{rms}
V_{bus}	DERs DC voltage	450 V
C_{dc}	DC-side capacitor	2200 µF
f_s	Switching frequency	18 kHz
L_a, L_b, L_c	Filter inductor	2.3 mH
C_{ga}, C_{gb}, C_{gc}	Filter capacitor	22 µF
L_r	Resonant inductor	40 µH
C_r	Parasitic/resonant capacitor	2 nF
C_c	Clamping capacitor	100 µF

The system control block of the grid-connected ZVS inverter is shown in Figure 8. The grid voltage and inverter output current were sensed and fed into the controller. The three-phase voltages and currents were transferred from nature reference frame to the synchronous reference frame. There exist three control loops in the proposed system. The first, second, and third control loops were the droop control, voltage control, and current control, respectively, as shown in Figure 8. The ZVS voltage source inverter was operated at a grid-supporting condition. In this paper, a 3 kW system was constructed for the simulation and experiment to verify the validity of the proposed ZVS PWM control scheme. The software PSIM version 9.1 was adopted for the simulation. In the experiment, the adopted active switches, S_1–S_7, were with an insulated-gate bipolar transistor (Fuji 2MBI100VA-060-50) that had a parasitic capacitor of 2 nF. The system controller was realized using DSP (TMS320F28335) manufactured by Texas Instruments and FPGA (Cmod-A7-35T) manufactured by Digilent, Inc. The design parameters of the circuit are listed in Table 1.

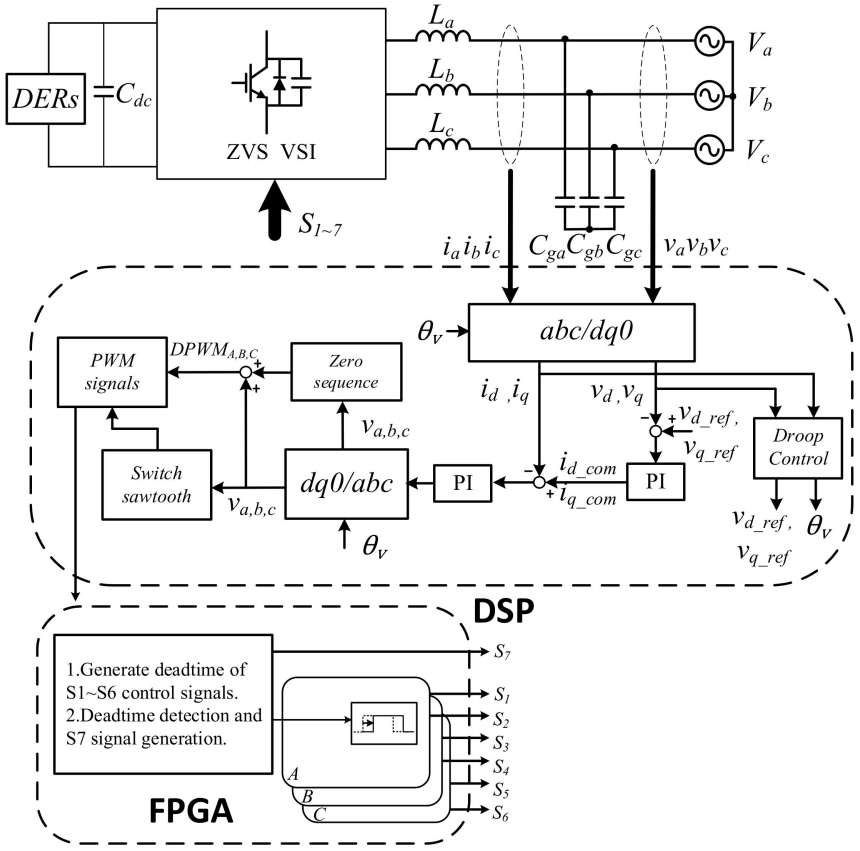


Figure 8. The control block of the proposed ZVS DPWM control strategy for grid-connected three-phase inverters.

Figure 9a,b show the simulation and experimental results of grid-connected voltage v_a, v_b, v_c and output phase current i_c respectively. As can be observed from Figure 9, inverter output current i_c is phase shifted by 180 degrees from grid-connected voltage v_c. That means the power flows from the DC side to grid side.

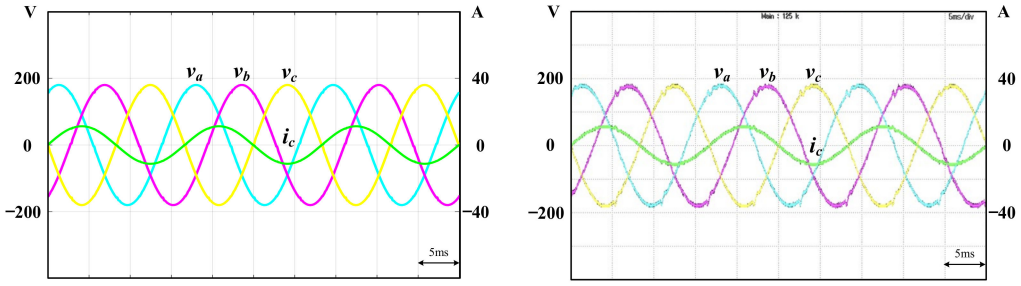
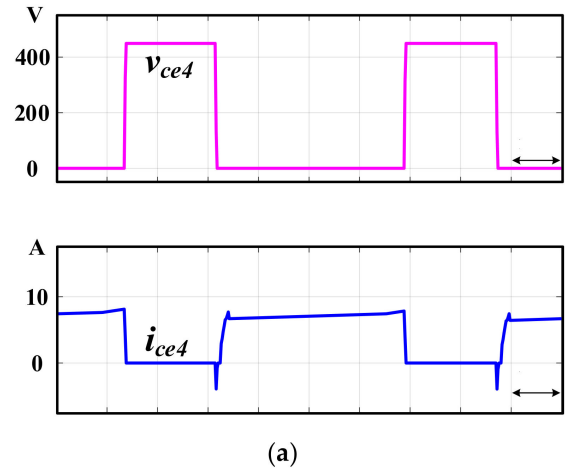


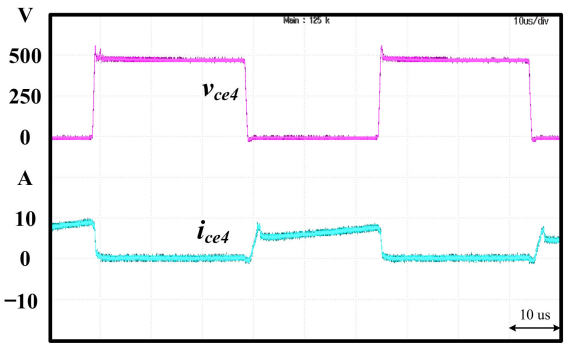
Figure 9. (**a**) Simulation waveforms and (**b**) experimental waveforms of the grid voltages v_a, v_b, and v_c, and output phase current i_c.

The simulation and experimental waveforms of the voltage, v_{ce}, and current, i_{ce}, of the main switch, S_4, operated in sector I are shown in Figure 10a,b, respectively. As can be observed form Figure 10, the ZVS ON was achieved in the switch S_4 and, at this time, the reverse recovery current in body diode D_3 of switch S_3 was suppressed as shown in Figure 11a,b for the simulation and experimental results, respectively. As can be seen from the simulation in Figure 11a, the current i_{S3}, which flowed through the body diode of switch S_3, was successfully suppressed when the switch S_3 was turned OFF. It should be noticed that in Figure 11b, the measured waveform can only show the current i_{ce3}, which is

the total current flowing through the switch and the parasitic capacitor. The simulation and experimental waveforms of voltage v_{ce7} and current i_{ce7} of the S_7 are shown in Figure 12a,b, respectively. It follows from Figure 12 that ZVS ON was indeed achieved in the S_7. The simulation and experimental waveforms of the v_{Cc} and the i_{Lr} in the auxiliary circuit are shown in Figure 13a,b, respectively. The v_{Cc} was at a low voltage level, and L_r was magnetized and demagnetized via control by the S_7. From Figures 9–13, one can see that the simulation and experimental results were in close agreement. The ZVS in both the main and auxiliary switches were indeed achieved. In addition, the reverse recovery current of the main switches was suppressed in the proposed ZVS DPWM control strategy.

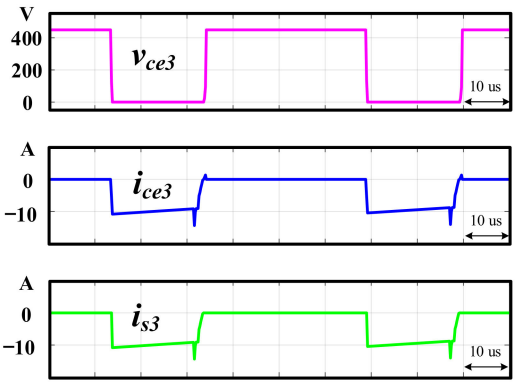


(**a**)



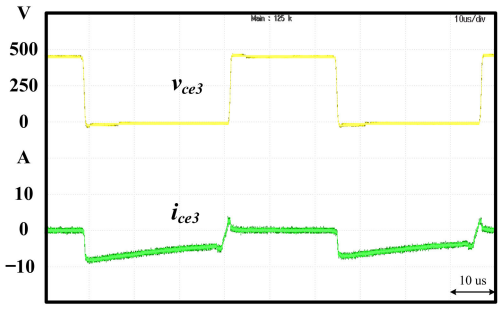
(**b**)

Figure 10. (**a**) Simulation waveforms and (**b**) experimental waveforms of the voltage and current of switch S_4.



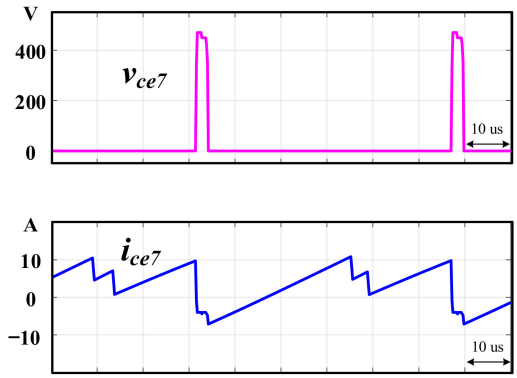
(**a**)

Figure 11. *Cont.*

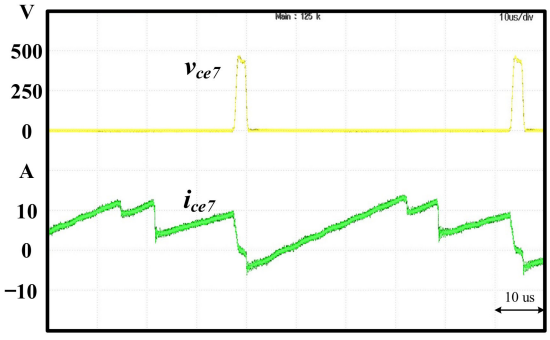


(**b**)

Figure 11. (**a**) Simulation waveforms of v_{ce3}, i_{ce3}, and i_{s3}; (**b**) the experimental waveforms of v_{ce3} and i_{ce3}.

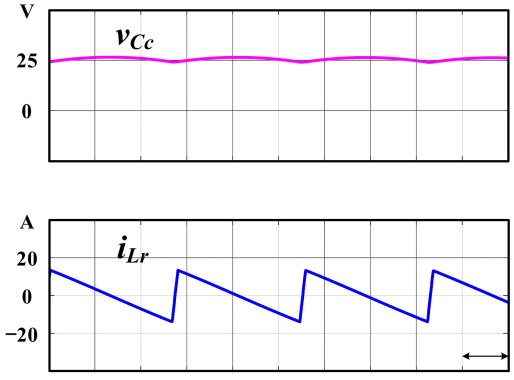


(**a**)



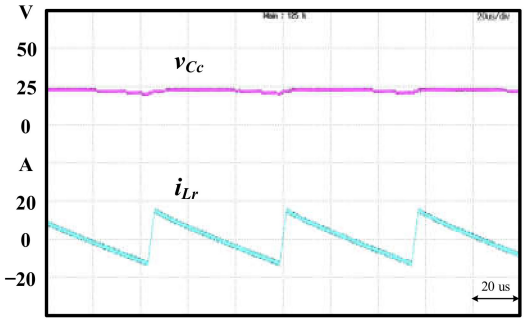
(**b**)

Figure 12. (**a**) Simulation waveforms and (**b**) experimental waveforms of the voltage and current of S_7.



(**a**)

Figure 13. *Cont.*



(**b**)

Figure 13. (**a**) Simulation waveforms and (**b**) experimental waveforms of v_{Cc} and i_{Lr}.

The conversion efficiency of the implementation is shown in Figure 14 in the comparison between the traditional sinusoidal pulse-width modulation (SPWM) without auxiliary circuit and the proposed ZVS DPWM control scheme. From a light load to a full load, the proposed ZVS DPWM control scheme had higher efficiency than the SPWM operation. The efficiency was significantly improved and reached a conversion efficiency of 97.1% at a load of 3 kW.

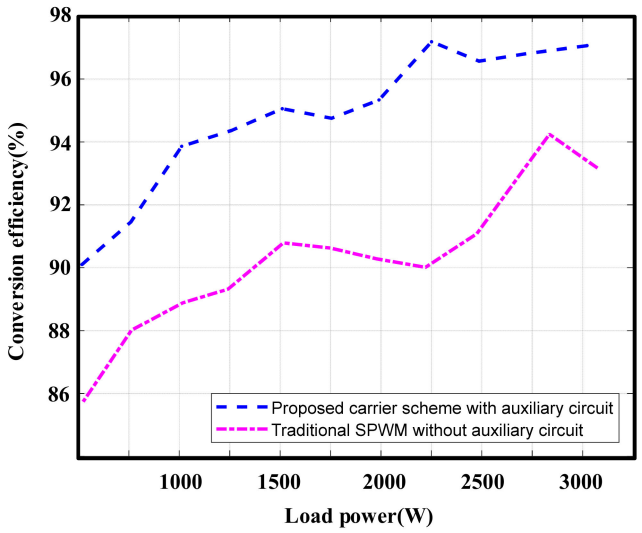


Figure 14. Efficiency comparison between the proposed ZVS PWM control scheme and the traditional SPWM control scheme.

Finally, to further reveal the potential merits of the proposed PWM control scheme, Table 2 is provided to summarize the comparisons of the extra elements, soft switching range, switching frequency, control complexity, switch voltage stress, and current stress as well as the filter design of the literature [2,3,12,13] and the proposed PWM control scheme.

Table 2. Comparison of the different ZVS methods for inverters.

-	Extra Elements	Soft Switching Range	Switching Frequency (f_s)	Control Complexity	Switch Voltage Stress	Switch Current Stress	Filter Design
[2]	LC+ switch	Full ZVS range	Fixed	Normal	V_{dc}	Low	LC
[3]	LC+ switch	Full ZVS range	Fixed	Difficult (leg-short operation)	V_{dc} + V_{cc}	Low	LC
[12]	None	Full ZVS range	Variable	Normal	V_{dc}	High	LCL
[13]	LC+ switch	Full ZVS range	Fixed	Simple (three carrier signals)	V_{dc} + V_{cc}	Low	LC
CB-DPWM	LC+ switch	Full ZVS range	Fixed	Simple (one carrier signal)	V_{dc}	Low	LC

5. Conclusions

In this article, a ZVS DPWM strategy for a grid-connected three-phase inverter was proposed. The saw-tooth carrier waveform with positive and negative slopes was utilized to generate the control signal of S_7, and it achieved ZVS in both the main and auxiliary switches. In addition, the reverse recovery current in the anti-parallel diodes of the main switches were suppressed. The circuit operation was clearly explained. Finally, a prototype was constructed. Both the simulation and experimental results verified the validity of the proposed ZVS DPWM strategy for the grid-connected three-phase inverter.

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References

1. Li, R.; Ma, K.; Xu, D. A Novel Minimum Voltage Active Clamping SVM (MVAC-SVM) Controlled Three-Phase PFC. In Proceedings of the Twenty-Fourth Annual IEEE Applied Power Electronics Conference and Exposition, Washington, DC, USA, 15–19 February 2009; pp. 1879–1885.
2. Li, R.; Ma, Z.; Xu, D. A ZVS Grid-Connected Three-Phase Inverter. *IEEE Trans. Power Electron.* **2012**, *27*, 3595–3604. [CrossRef]
3. Li, R.; Xu, D. A zero-voltage switching three-phase inverter. *IEEE Trans. Power Electron.* **2014**, *29*, 1200–1210.
4. Du, C.; Hurley, W.G.; Xu, D. Design Methodology of Resonant Inductor in a ZVS Inverter. *IEEE J. Emerg. Sel. Top. Power Electron.* **2015**, *3*, 1142–1150. [CrossRef]
5. Du, C.; Xu, D.; He, N.; Zhu, N. Modeling and Optimization of a Zero-Voltage Switching Inverter for High Efficiency and Miniaturization. *IEEE Trans. Power Electron.* **2017**, *32*, 150–163. [CrossRef]
6. Du, C.; He, N.; Xu, D. Design of zero-voltage-switching three-phase grid inverter. In Proceedings of the IEEE 2nd Annual Southern Power Electronics Conference (SPEC), Auckland, New Zealand, 5–8 December 2016; pp. 1–6.
7. Wu, Y.; He, N.; Chen, M.; Xu, D. Generalized Space-Vector-Modulation Method for Soft-Switching Three-Phase Inverters. *IEEE Trans. Power Electron.* **2021**, *36*, 6030–6045. [CrossRef]
8. De Doncker, R.W.; Lyons, J.P. The auxiliary resonant commutated pole converter. In Proceedings of the Conference Record of the 1990 IEEE Industry Applications Society Annual Meeting, Seattle, WA, USA, 7–12 October 1990; pp. 1228–1235.
9. Beukes, H.J.; Enslin, J.H.R.; Spee, R. Performance of the auxiliary resonant commutated pole converter in converter based utility devices. In Proceedings of the PESC Record 27th Annual IEEE Power Electronics Specialists Conference, Baveno, Italy, 23–27 June 1996; pp. 1033–1039.
10. Zhou, W.; Yuan, X.; Laird, I. Performance Comparison of the Auxiliary Resonant Commutated Pole Inverter (ARCPI) using SiC MOSFETs or Si IGBTs. In Proceedings of the 2019 IEEE Energy Conversion Congress and Exposition (ECCE), Baltimore, MD, USA, 29 September–3 October 2019; pp. 1981–1987.
11. Voss, J.; Warmuz, J.; Mathai, D.; De Doncker, R.W. Adapted Auxiliary-Resonant Commutated Pole in the Dual-Active Bridge. *IEEE J. Emerg. Sel. Top. Power Electron.* **2019**, *7*, 2553–2560. [CrossRef]
12. Chen, J.; Sha, D.; Zhang, J. Current ripple prediction and DPWM based variable switching frequency control for full ZVS range three-phase inverter. *IEEE Trans. Ind. Electron.* **2021**, *68*, 1412–1422. [CrossRef]
13. Shi, K.; Deng, J.; Xu, D. A General Pulse Width Modulation Method for Zero-Voltage-Switching Active-clamping Three-phase Power Converters: Edge Aligned Pulse Width Modulation (EA-PWM). *IEEE Open J. Power Electron.* **2020**, *1*, 250–259. [CrossRef]