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Analysis and Design of a Wideband Low-Noise Amplifier with Bias and Parasitic Parameters Derived Wide Bandpass Matching Networks

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Abstract: This paper proposes a 110% relative bandwidth (RBW) low-noise amplifier (LNA) for broadband receivers with flat gain, low noise and high linearity. Bias and parasitic parameters derived wide bandpass (BPDWB) matching networks and a cascode with dual feedbacks are introduced for broadband performance. Matching network design procedures are demonstrated, and results show that the frequency response of the network fits the target impedance well from 1 GHz to 3.5 GHz. The proposed BPDWB network improves the design efficiency and enhances the prediction accuracy of impedance matching. The proposed LNA in 0.25 μm GaAs pseudomorphic high electron mobility transistor (GaAs pHEMT) technology realizes a minimum NF of 0.45 dB at 1.6 GHz where the NF is less than 0.55 dB within the operating frequency band. A flat gain of 22.5–25.2 dB is achieved with the input voltage standing wave ratio (VSWR) below 1.22 and output VSWR less than 2.5. In addition, the proposed LNA has good linearity where the output third-order intercept point (OIP3) is better than +31.5 dBm, and the output 1 dB compression point (OP1dB) is better than +19 dBm over the wide frequency range.

Keywords: low-noise amplifier; wide bandpass matching network; cascode; feedback

1. Introduction

Modern wireless communication systems are rapidly developing in the direction of multi-carrier, large-capacity and high-speed information transmission. The demand for high-performance transceivers is increasing [1–3]. As the first active component of the RF front-end, the properties of the LNA, especially bandwidth, noise and linearity, will directly affect the performance of the receiver [4,5]. In response to various RF applications, wideband LNAs handle multiple operating frequencies within a limited chip area, which greatly improves the integration of the RF front-end and plays an important role in many applications such as mobile communications, CATV, satellite navigation, and so on [6–8].

To achieve a balanced performance, the wideband LNA needs to compromise on the strict specifications in a large frequency range, usually several GHz. However, these indicators have a trade-off to each other, which brings challenges to the design of wideband LNAs. Technologies to achieve broad bandwidth with low noise simultaneously are extensively developed and studied [9–14]. In [9], a bandwidth-enhanced Darlington amplifier with shunt feedback is adopted to implement a broadband amplifier with flat gain. However,

the NF could not be tolerated due to resistance networks at the Darlington structure. In [10], an LNA with a relative bandwidth of 165% is realized based on the cascade amplifier with resistive feedback. The CS with feedback can achieve a flat broadband bandwidth, but the noise caused by the resistance in feedback is unsatisfactory. Reference [11] explores a bandwidth enhancement technique based on inductive peaking. In [12], a method for designing wideband noise matching is presented.

Compared with semiconductor processes like CMOS and GaN, GaAs has excellent RF performance and cost advantages [13,14]. Compared with MOSFET, HBT and other devices, pHEMT devices have better noise performance and thermal stability [15,16]. Compared with HEMT, the pHEMT has lower noise and higher electron mobility [17,18]. Therefore, GaAs pHEMT, with excellent RF characteristics and acceptable cost, was selected in this paper.

In order to achieve the goal of wide bandwidth and low noise simultaneously, this paper proposed a wideband LNA using BPDWB matching networks and cascode topology with dual feedbacks. The proposed BPDWB network incorporates the L/C in the bias circuit and non-ideal parasitic elements into the design of the matching network, which can realize broadband matching and reduce the negative impact of parasitic components on the circuit concurrently.

The paper is organized as follows: Section 2 introduces the design method of the wideband LNA in detail, including the analysis of the cascode amplifier with dual feedbacks and the design process of the BPDWB network. Section 3 presents the simulation and measurement performance of the proposed LNA and compares it with other published works. Finally, conclusions are given in Section 4.

2. Proposed LNA Design

Compared with a narrowband amplifier, a wideband amplifier has the characteristics of large impedance change. To achieve wideband operation, additional circuitry is required. Typically, this means that additional lumped components need to be added to improve the impedance matching of the amplifier to support wideband operation, feedback configuration needs to be added to widen the operable frequency range, or the narrowband amplifier needs to be cascaded [19–21]. In this paper, dual feedbacks and bandpass matching networks are combined to expand the bandwidth of LNA and to select the input signal simultaneously. Figure 1 shows the block diagram of the proposed wideband LNA module. The core of LNA is a cascode topology with dual feedbacks, and the input–output matching is a bandpass network using BPDWB, respectively.
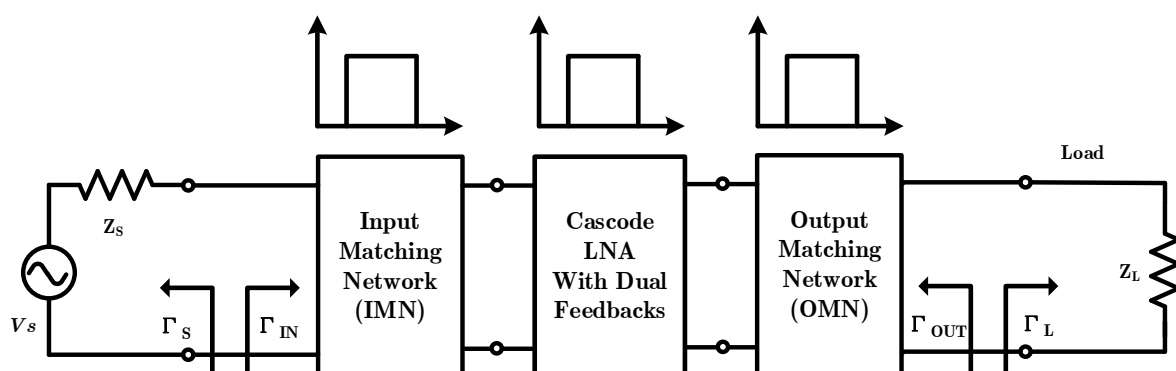

Figure 1. The block diagram of the proposed wideband LNA module.

2.1. Cascode with Dual Feedbacks

Linearity and gain are two opposing poles that are difficult to balance, and if we try to improve one, it automatically reduces the other [22]. In this paper, this problem is alleviated by the cascode with feedbacks. The gain of LNA is improved by the stacking of CS and CG, where the Miller effect of CS is cancelled by CG. The linearity is enhanced at the cost

of gain by introducing feedback [23]. In short, this approach allows a good compromise between gain and linearity.

In this paper, dual feedbacks (series inductance L_S, parallel resistance R_f and capacitance C_f) are connected to the cascode in Figure 2 to achieve high, flat gain and improved linearity.
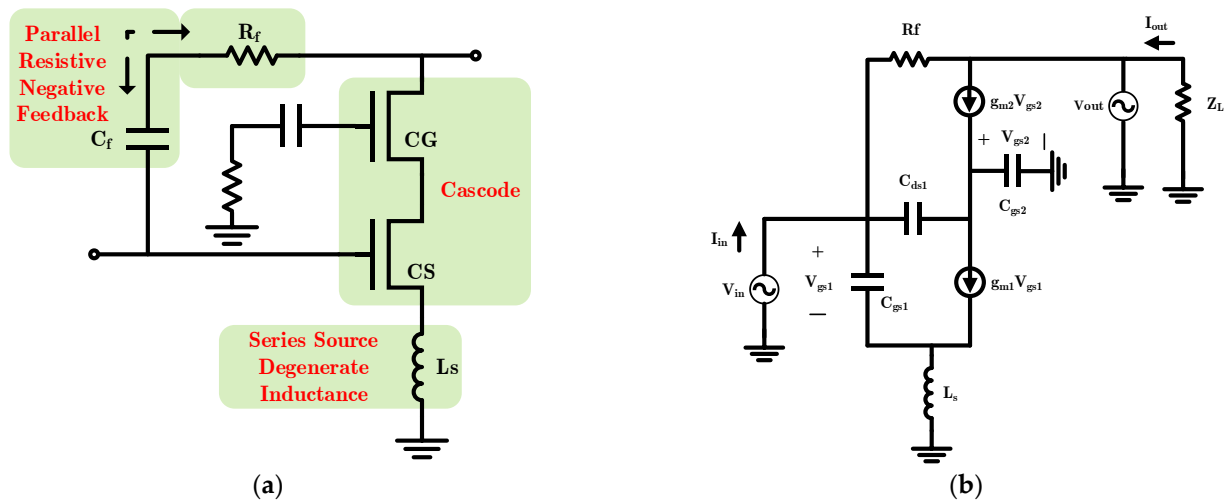
Figure 2. (**a**) Cascode with dual feedbacks; (**b**) The small-signal equivalent model of (**a**).

For the series inductor L_s at the source terminal of C_S, a real impedance is introduced to help meet the requirement of input matching and noise matching. In theory, simultaneous noise and input impedance matching can be attained. And there is no impact on the noise performance in the case of ideal inductance [23]. However, due to the non-ideality associated with L_s, additional noise will be introduced to the amplifier. It is necessary to select a suitable value of L_S at an acceptable range. When small enough, L_s is often replaced by microstrip lines.

For the parallel negative feedback network between the drain terminal of CG and the gate terminal of CS, it couples the AC signal from the output to the input through the feedback capacitor C_f. The depth of feedback is adjusted by resistor R_f. Since the feedback resistor will also introduce a noise source, the value of the feedback resistor needs to be chosen properly.

2.2. Bias and Parasitic Parameters Derived Wide Bandpass Matching Network

For the structure in Figure 2b, the input and output impedance can be equivalent to the form of the capacitance and reactance element in parallel, which exhibits capacitive properties at high frequency. For this case, bandpass matching can be used to achieve ideal matching where ideal bandpass filters can be realized by infinite RLC passive components theoretically [24], as shown in Figure 3, divided into basic units. However, the more components used in the circuit design, the more noise and parasitic are introduced. Several common implementations of bandpass matching circuits are shown below.

To achieve the goal of a bandpass matching network without too many lumped components and improve the design accuracy of the matching network, this paper proposes a bandpass filter matching circuit derived from the bias and parasitic parameters named the BPDWB network. A combination of the bias and parasitic elements is used to compose the basic form of the bandpass filter marked in red in Figure 3. After that, the integrated matching network design is completed with the help of the Smith Chart according to the actual needs of impedance transformation. Figure 4 show two possible input and output matching circuits based on BPDWB.
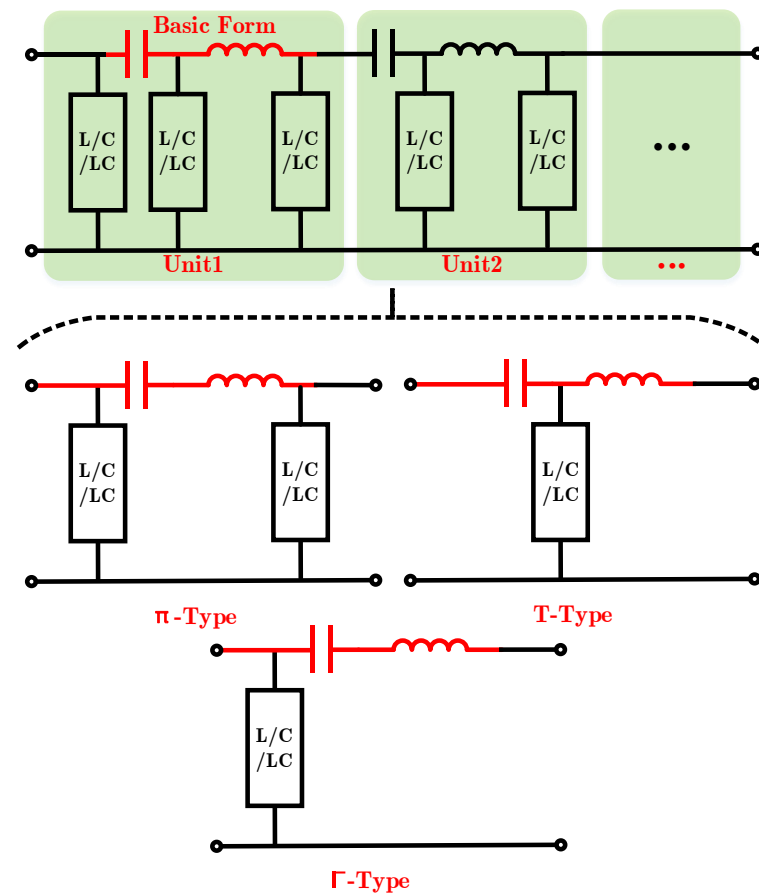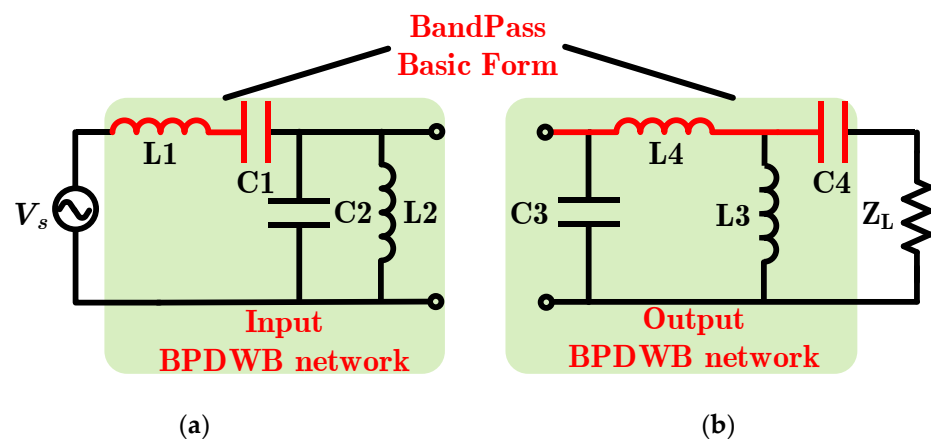
Figure 3. The composition of the bandpass filter.

Figure 4. (**a**) The proposed input matching network based on BPDWB; (**b**) output matching network based on BPDWB.

For the input matching network in Figure 4a, it is composed of a series inductor L_1 and capacitor C_1 with a parallel capacitor C_2 and inductor L_2. C_1 can serve as the input DC block, and L_2 as the gate choke inductor. Bonding wire is incorporated into L_1. The model of the bonding wire is shown in Figure 5. Its parasitic resistance is usually ignored at RF because it is made of the gold. The capacitor C_2 includes the parasitic capacitance at the input such as the PAD and ESD. The output network shown in Figure 4b is composed of L_4, C_4 in series and C_3, L_3 in parallel. L_3 can be used as a choke inductor and C_4 as the output DC block capacitor. C_3 includes the parasitic capacitance at the output. C_2 and C_3 in parallel expand the reactance adjustment range of the matching network so as to fit the frequency response target better.
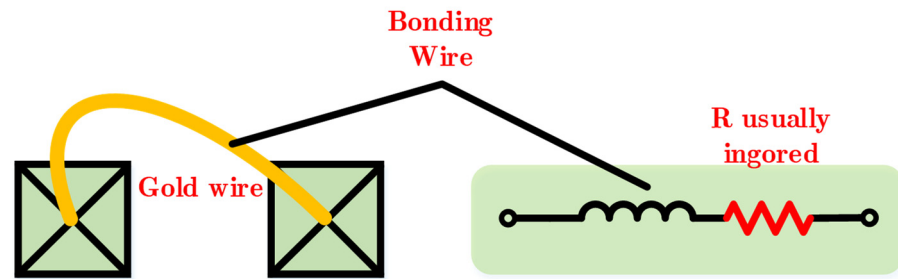
Figure 5. The model of the bonding wire.

Once the structure is determined, the frequency response of the network can be determined by analyzing the transmission characteristics. Regarding the network as a two-port network composed of internal unit circuits, the characteristics of the network can be described by the ABCD matrix.

According to the definition of the ABCD matrix, the input network in Figure 4a can be expressed as

$$
\begin{bmatrix} A & B \\ C & D \end{bmatrix}_{IMN} = \begin{bmatrix} 1 & j\omega L_1 \\ 0 & 1 \end{bmatrix} \begin{bmatrix} 1 & 0 \\ j\omega C_2 & 1 \end{bmatrix} \begin{bmatrix} 1 & \frac{1}{j\omega C_1} \\ 0 & 1 \end{bmatrix} \begin{bmatrix} 1 & 0 \\ \frac{1}{j\omega L_2} & 1 \end{bmatrix}
$$
$$
= \begin{bmatrix} 1 + \frac{C_2}{C_1} - \omega^2 C_2 L_1 - \frac{1}{\omega^2 C_1 L_2} + \frac{L_1}{L_2} & \frac{1}{j\omega C_1} + j\omega L_1 \\ j\omega C_2 + \frac{1}{j\omega L_2} & 1 \end{bmatrix} \tag{1}
$$

The A parameter of the input network can be obtained as

$$
A_{IMN} = 1 + \frac{C_2}{C_1} - \omega^2 C_2 L_1 - \frac{1}{\omega^2 C_1 L_2} + \frac{L_1}{L_2} \tag{2}
$$

Therefore, the transfer function of the input matching network can be obtained as

$$
S_{21}(\omega)_{IMN} = \frac{2}{A_{IMN}} = \frac{2}{1 + \frac{C_2}{C_1} - \omega^2 C_2 L_1 - \frac{1}{\omega^2 C_1 L_2} + \frac{L_1}{L_2}} \tag{3}
$$

Similarly, the ABCD matrix of the output network in Figure 4b is

$$
\begin{bmatrix} A & B \\ C & D \end{bmatrix}_{OMN} = \begin{bmatrix} 1 & \frac{1}{j\omega C_4} \\ 0 & 1 \end{bmatrix} \begin{bmatrix} 1 & 0 \\ \frac{1}{j\omega L_3} & 1 \end{bmatrix} \begin{bmatrix} 1 & j\omega L_4 \\ 0 & 1 \end{bmatrix} \begin{bmatrix} 1 & 0 \\ j\omega C_3 & 1 \end{bmatrix}
$$
$$
= \begin{bmatrix} 1 - \frac{1}{\omega^2 C_4 L_3} - \omega^2 C_3 L_4 + \frac{C_3 L_4}{C_4 L_3} + \frac{C_3}{C_4} & j\omega L_4 + \frac{L_4}{j\omega C_4 L_3} + \frac{1}{j\omega C_4} \\ \frac{1}{j\omega L_3} + \frac{j\omega C_3 L_4}{L_3} + j\omega C_3 & 1 + \frac{L_4}{L_3} \end{bmatrix} \tag{4}
$$

The A parameter of the output network can be obtained as

$$
A_{OMN} = 1 - \frac{1}{\omega^2 C_4 L_3} - \omega^2 C_3 L_4 + \frac{C_3 L_4}{C_4 L_3} + \frac{C_3}{C_4} \tag{5}
$$

The transfer function of the output matching network is

$$
S_{21}(\omega)_{OMN} = \frac{2}{A} = \frac{2}{1 - \frac{1}{\omega^2 C_4 L_3} - \omega^2 C_3 L_4 + \frac{C_3 L_4}{C_4 L_3} + \frac{C_3}{C_4}} \tag{6}
$$

From Equations (3) and (6), it can be seen that the transfer characteristics of matching circuits are affected by constituent units. The target function can be obtained by tuning the value of components which indicates that the BPDWB network possesses strong tunable performance.

2.3. Design and Implementation of the Wideband Low-Noise Amplifier

Composed of the cascode with dual feedbacks and BPDWB matching networks, the complete circuit of the proposed LNA is shown in Figure 6. LNA is designed with a single positive voltage supply of 5 V. Additionally, the size of the CS and CG transistor is 8 × 75 μm and 8 × 90 μm. The CS and CG is biased at VGS = 0.62 V@VDS = 1.3 V, VGS = 0.52 V@VDS = 3.6 V, respectively.
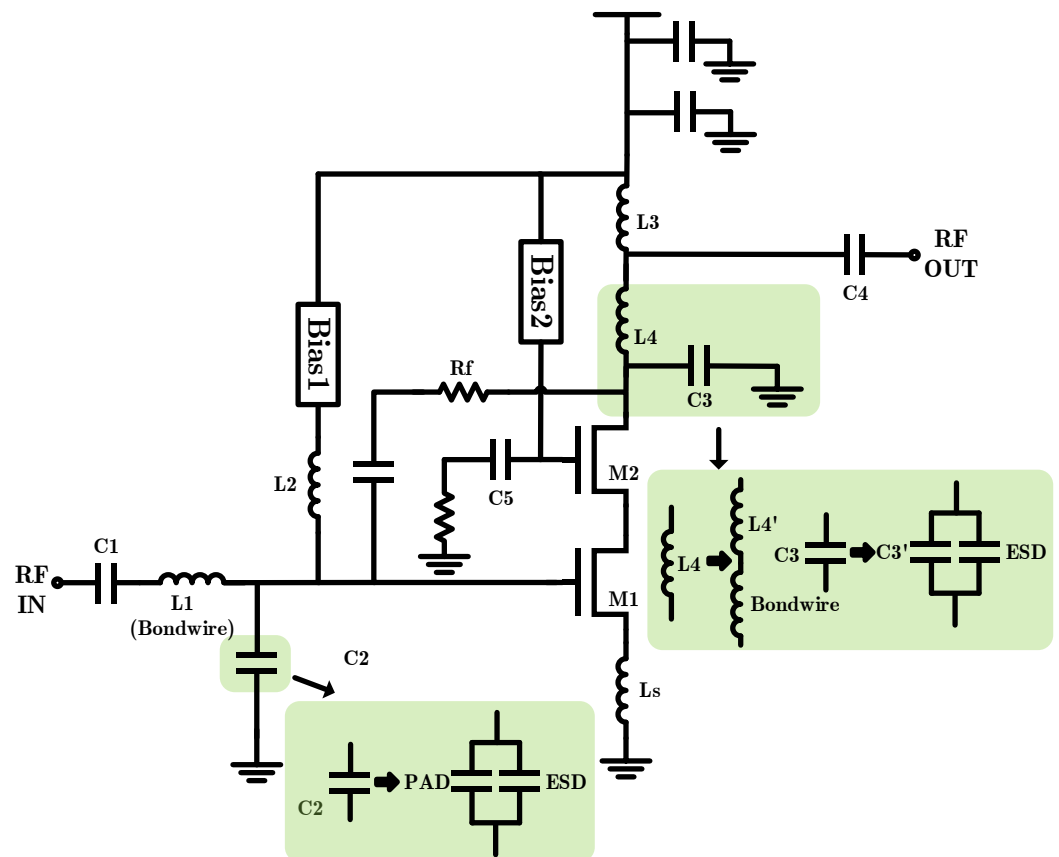
Figure 6. The complete circuit of the proposed LNA.

For expressions (3) and (6), we simplify the analysis by considering the actual situation of the circuit. Since the relation in expressions (7) is:

$$L_1 << L_2;\ C_2 << C_1 \tag{7}$$

The following items in Equation (3) can be ignored:

$$\frac{C_2}{C_1} \approx 0;\ \frac{L_1}{L_2} \approx 0 \tag{8}$$

Thus, Equation (3) can be simplified as

$$S'_{21}(\omega)_{IMN} \approx \frac{2}{1 - \omega^2 C_2 L_1 - \frac{1}{\omega^2 C_1 L_2}} = \frac{2\omega^2 C_1 L_2}{\omega^2 C_1 L_2 - \omega^4 C_1 C_2 L_1 L_2 - 1} \tag{9}$$

It can be found that expression (9) is mainly determined by C_1-L_2 on a numerator at low frequency. Therefore, the target transmission characteristics can be achieved by adjusting the value of C_1-L_2 accompanied by tuning C_2 and L_1.

As frequency increases, Equation (9) can be abbreviated as

$$S''_{21}(\omega)_{IMN} \approx \frac{2\omega^2 C_1 L_2}{\omega^2 C_1 L_2 - \omega^4 C_1 C_2 L_1 L_2} = \frac{2}{1 - \omega^2 C_2 L_1} \tag{10}$$

In Equation (10), the transmission characteristic is mainly affected by the parasitic parameters L_1-C_2. It shows that the parasitic parameters begin to take effect at high frequencies and deteriorate the transmission performance of the network severely. Therefore, the high cut-off frequency of the matching network can be tuned by controlling the value of parasitic parameters, such as the length of the bond wire.

In addition to the S_{21} transmission, noise is also an important index that we should consider synchronously.

For noise figures, we know that

$$F = F_{MIN} + \frac{G_n}{R_s}|Z_s - Z_{SOPT}|^2 \tag{11}$$

where F_{MIN} is the minimum noise figure, G_n is the noise admittance, R_s is the real part of complex source impedance and Z_{SOPT} is the optimum source impedance.

As the frequency increases, the C_{gd} of M1 is considered. According to Miller equivalence, C_{gd} and R_f can be equivalent to the equivalent capacitance and resistance to ground at the input, that is, to contribute to C_2 and introduce an equivalent noise source R_{fM}.

$$R_{fM} = R_f/(1 - A_v) \tag{12}$$

where A_V is the open-loop voltage gain of the amplifier. According to Formula (12), we know that the greater R_f, the greater R_{fM}.

C_2 affects the G_n, R_s and $Z_s - Z_{SOPT}$, thereby deteriorating the NF. Fortunately, we can try to improve this situation by feedbacks. For R_{fM}, the greater its value, the smaller the impact on noise. Therefore, it is necessary to meet the noise requirements by adjusting L_s and selecting an appropriate R_f. Simulation finds that when R_f is greater than 2000 Ω, the effect on noise is no longer obvious. Finally, $R_f = 2500$ Ω was chosen. On this basis, according to the transmission characteristics and acceptable noise performance, we finally selected $L_s \approx 0.1$ nH.

At the output, the capacitance of the DC blocking capacitor C_4 is large enough to make the following items close to zero

$$\frac{C_3 L_2}{C_4 L_3} \approx 0; \; \frac{C_3}{C_4} \approx 0 \tag{13}$$

Therefore, Equation (6) can be abbreviated as

$$S'_{21}(\omega)_{OMN} \approx \frac{2}{1 - \frac{1}{\omega^2 C_4 L_3} - \omega^2 C_3 L_4} = \frac{2\omega^2 C_4 L_3}{\omega^2 C_4 L_3 - \omega^4 C_3 C_4 L_3 L_4 - 1} \tag{14}$$

At low frequencies, the response of the matching network in Equation (14) is mainly affected by C_4-L_3. At high frequencies, the transfer function can be expressed as Equation (15) which is mainly affected by C_3-L_4, especially the high cut-off frequency.

$$S''_{21}(\omega)_{OMN} \approx \frac{2}{1 - \omega^2 C_3 L_4} \tag{15}$$

Therefore, the output network can keep constant within the target bandwidth by controlling the tuning C_3-C_4-L_3-L_4, especially C_3-L_4, because high-frequency characteristics are paid special attention to in the design of LNA. In addition, the influence of the output impedance on linearity such as OIP3, should be taken into account in the design of the LNA. According to the two-tone load–pull results, the impedance point for the maximum OIP3

at frequency = 2.2 GHz is Z = 60.6 + j × 12.6 Ω. In order to select the appropriate value of C_3-L_4 to meet the requirements of output matching and linearity, different combinations of C_3-L_4 are scanned, and the corresponding results are shown in Figure 7. According to the results, the inductance L_4 = 2.5 nH and the capacitance C_3 = 300 fF are selected, which can meet the requirements of bandwidth, reflection coefficient and linearity at the same time.
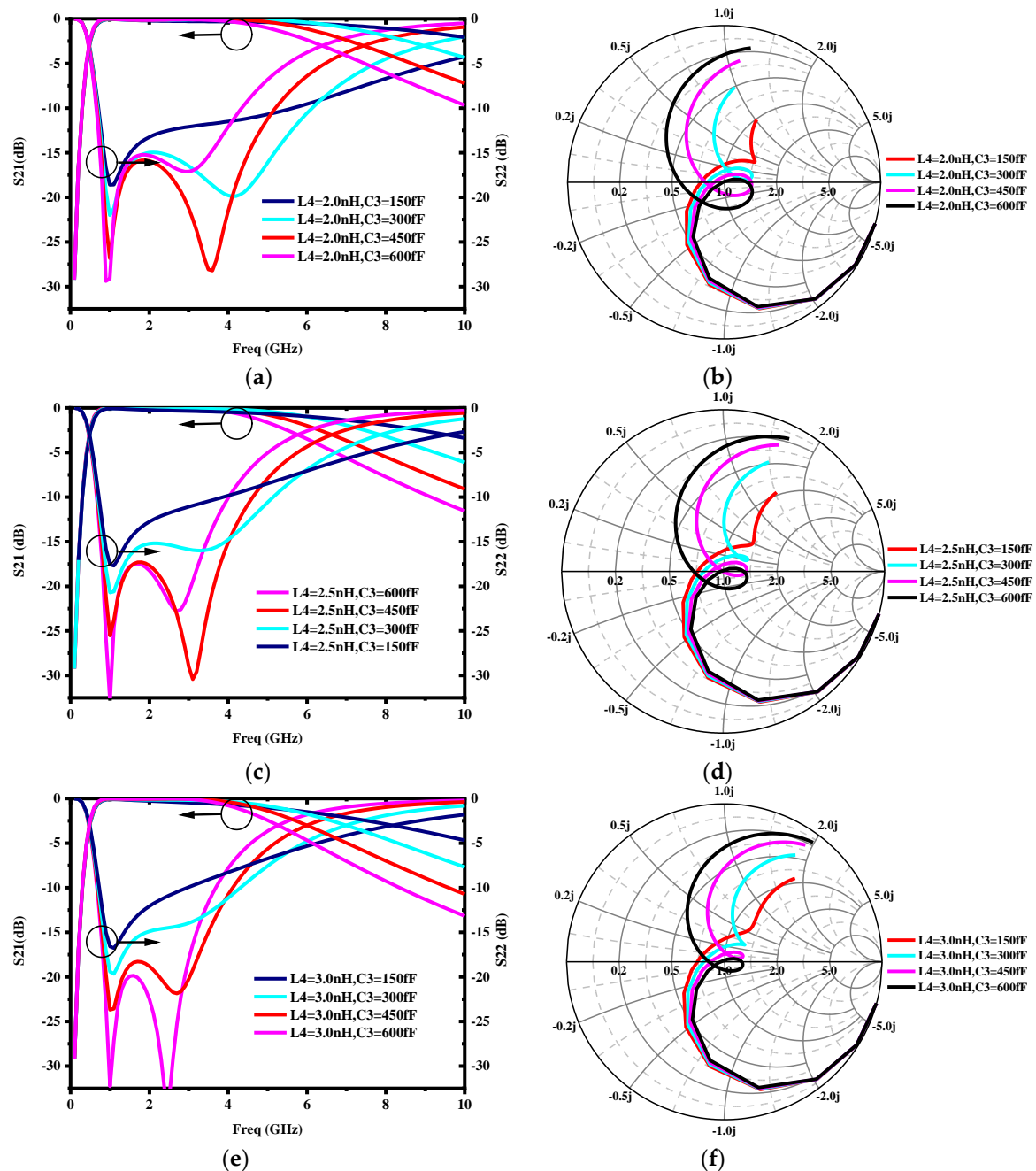
Figure 7. Performance of different combinations of capacitor C_3 and inductance L_4: (**a**) S-Parameters for L_4 = 2 nH; (**b**) Impedance trace of (**a**); (**c**) S-Parameters for L_4 = 2.5 nH; (**d**) Impedance trace of (**c**); (**e**) S-Parameters for L_4 = 3 nH; (**f**) Impedance trace of (**e**).

Finally, according to the compromise of each index, the values of each component of the proposed LNA are shown in Table 1.
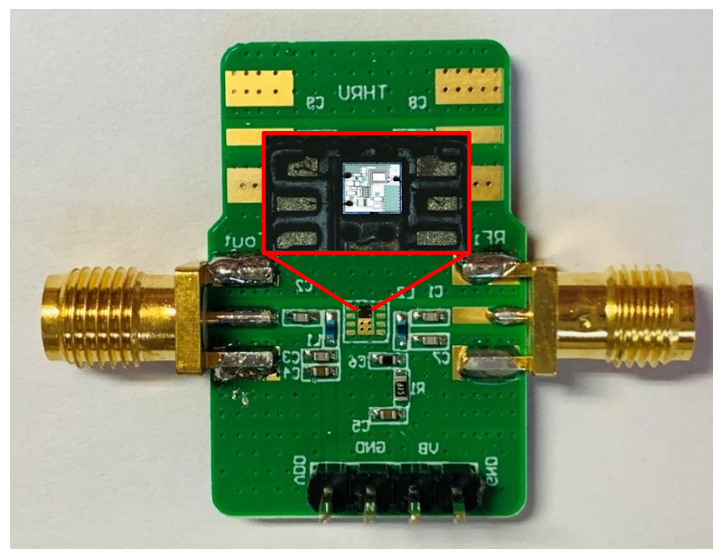
Table 1. Values of components in circuit.

Device	Value	Uint
M1	8×75	µm
M2	8×90	µm
C_1	56	pF
C_2	5.7	pF
C_3	300	pF
C_4	6.6	pF
C_5	2.4	pF
L_1	0.75	nH
L_2	9.5	nH
L_3	9.5	nH
L_4	2.5	nH
L_s	0.1	nH
R_f	2500	Ω

3. Measurement Results

The die and assembly diagram of the chip is shown in Figure 8. The realized LNA is characterized by both linear and non-linear measurements.

Figure 8. The assembly diagram of the proposed LNA complete circuit.

To define small-signal behavior, LNA scattering parameters were measured with an Agilent N5230A vector network analyzer. The input/output port of the LNA was designed to be 50 Ω. A PCB test board was developed to simulate practical scenarios, and bond wires were used to connect to the PCB board at each port on the chip. Figure 9 show the measured scattering parameters of the LNA, together with the simulated ones.

From Figure 9, a peak gain of 25.8 dB was measured at 1.2 GHz, which is 1.4 dB lower than the simulated result. Measured S11 and S22 was lower than −20 dB and −7 dB from 1 GHz to 3.5 GHz. As far as S11 and S22 are concerned, the difference between simulation and measurement can be ascribed to the input and output connector and to the coupling parasitic between the devices. The S12 data is lower than −30 dB in the frequency band, indicating that the amplifier had a high level of reverse isolation making the LNA unconditionally stable. Measured scattering parameters demonstrated that the BPDWB network had good prediction accuracy for RF LNA.

For the noise performance, the NF measurement was completed by an Agilent N8975A noise figure meter. A low noise figure (NF) of 0.5 dB (with a ripple of 0.05 dB) was registered in the range from 1 GHz to 3.5 GHz, shown in Figure 10. Compared with simulation data,

the measured NF was about 0.1 dB higher. This was caused by the difference between the device and model. And the simulation could not simulate the real conditions of the working device absolutely.
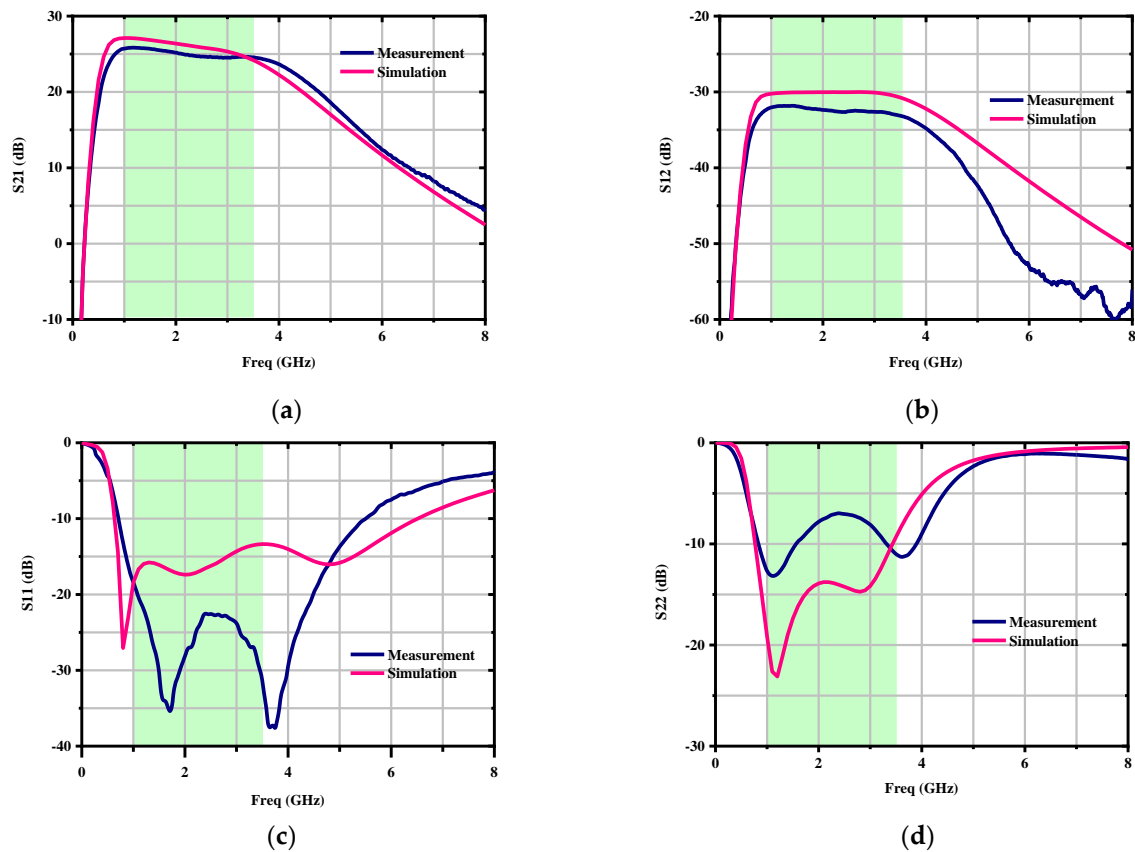

(a)

(b)

(c)

(d)

Figure 9. Scattering parameters of the proposed LNA (**a**) S21; (**b**) S12; (**c**) S11; (**d**) S22.
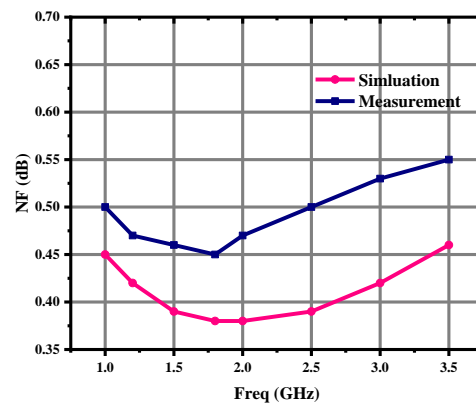
Figure 10. NF performance in the frequency range 1 GHz–3.5 GHz.

To define large-signal behavior, the linearity measurements were performed for the LNA. Figure 11 present the measured OP1dB and OIP3 results with simulated data according to the single-tone output power test and two-tone third-order intermodulation test. The LNA processes the OP1dB better than +19 dBm and OIP3 greater than +31.5 dBm by 3.5 GHz. Due to transistor large-signal model errors, the measured linearity data is about 2 dB lower than the simulated results.

(**a**)　　　　　　　　　　　　　　　　　　　　　　　(**b**)

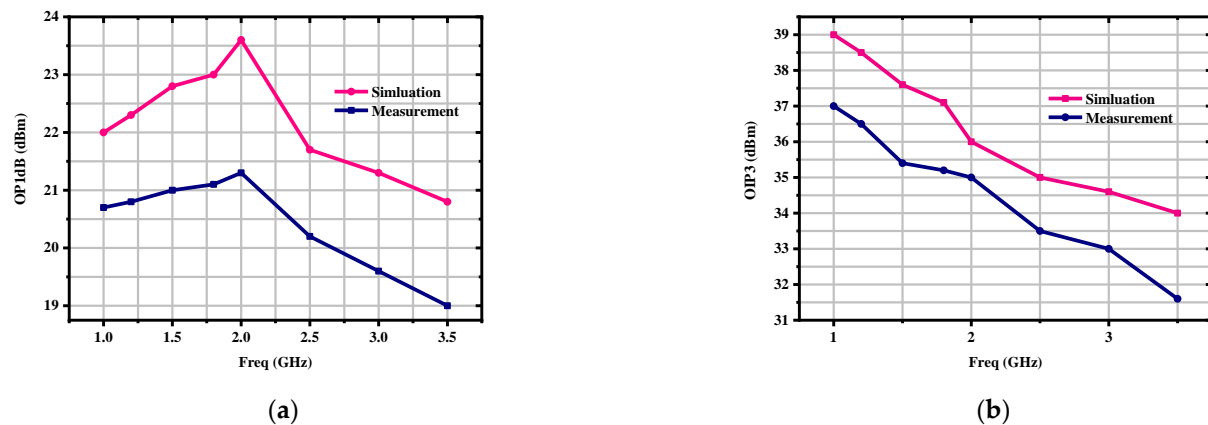**Figure 11.** Linearity performance in the frequency range 1 GHz–3.5 GHz (**a**) OP1dB; (**b**) OIP3.

Table 2 present a comprehensive summary of the performance of the designed wideband LNA and a comparison of the latest works of other published LNAs over the L to S-band.

Table 2. Performance summary and comparison.

Ref.	Process	Architecture/Model	Bandwidth (GHz)	Gain (dB)	NF (dB)	S11 (dB)	IIP3 (dBm)	IP1dB (dBm)	Vdd(V)	Pdd (mW)
This Work	0.25 μm GaAs pHEMT	Casscode with dual feedbacks and BPDWB	1–3.5/110%	22.5–25.2	0.5 ± 0.05	−20 max	9 min	−3 min	5	330
Ref' 01 [25]	GaAs pHEMT Off the-shelf	Folded-cascode with intrinsic Cgd feedback	0.4–0.8/66.7%	41	0.34 max	−8 max	−25 min	−32.8	5	406
Ref' 02 [26]	0.25 μm GaAs pHEMT	Two-stage cascade	2–4/66.7%	32.1 ± 0.44	0.8–2.0	−6 max	NA	NA	5	267
Ref' 03 [27]	0. 5 μm GaAs pHEMT	Casscode with capacitive feedback	1–4/120%	20–23	1.8–2.3	−10 max	NA	NA	5	250
Ref' 04 [28]	0.25 μm GaAs pHEMT	Casscode with feedback	1.65–2.75/50%	19.7 ± 1.5	0.58 max	NA	10 *	NA	NA	NA
Mod' 01	GaAs pHEMT	HMC618ALP3E	1.2–2.2/58.8%	19	0.75	−18	10	−3	5	445
Mod' 02	GaAs pHEMT	SKY67151-396LF	0.7–3.8/130%	19 @2.5 G	0.5 @2.5 G	−11 @2.5 G	17 @2.5 G	1.7 @2.5 G	5	360
Mod' 03	GaAs pHEMT	QPL9057	1.5–4/91%	18.5–21.7	0.5–0.85	−10 max	NA	NA	5	600
Mod' 04	GaAs pHEMT	TQL9093	0.6–4.2/150%	21.5–25	0.43–0.9	−6 max	NA	NA	5	250

* Calculated from gain and OIP3.

From the comparison in the table, we can find that in the L-S frequency band, the LNA implemented in this paper within an octave bandwidth has better gain and NF performance than most of the LNAs compared.

4. Conclusions

In this paper, the proposed broadband LNA with the BPDWB network were designed. The theoretical analysis and graphical explanation of the BPDWB design were also discussed. By combining parasitic parameters and bias into BPDWB, the design efficiency and prediction accuracy of the matching circuit were greatly improved. Furthermore, thanks to dual feedbacks, the gain, bandwidth and linearity were also well compromised. The measurement results show that the LNA gain was greater than 22.5 dB and the noise figure less than 0.55 dB from 1 GHz to 3.5 GHz, which verifies the good performance of the proposed LNA and the reliability of the proposed BPDWB network.

Author Contributions: Conceptualization, J.Z., F.W., H.Y., K.W., C.L., J.W., X.L. and Y.Y.; methodology, J.Z., X.L., J.W. and Y.Y.; software, J.Z., F.W. and H.Y.; validation, J.Z., S.Z. and K.W.; data curation, J.Z., F.W. and H.Y.; writing—original draft preparation, J.Z., S.Z. and K.W.; writing—review and editing, J.W., X.L., C.L. and Y.Y.; funding acquisition, X.L. All authors have read and agreed to the published version of the manuscript.

Conflicts of Interest: The authors declare no conflict of interest.

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