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From 32 nm to TFET Technology: New Perspectives for Ultra-Scaled RF-DC Multiplier Circuits

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Abstract: In this present work, different Cross-Coupled Differential Drive (CCDD) CMOS bridge rectifiers are designed using either 32 nm or Tunnel-FET (TFET) technology. Commercial PDK has been used for the 32 nm technology, while lookup tables (LUT) resulting from a physics model have been applied for the TFET. To consider the parasitic effects for the circuit performances, the 32 nm-based circuits have been laid out, while a parasitic model has been included in the TFET LUT for circuit implementation. In this work, the post-layout simulations, including parasitic, demonstrate for conventional CCDD circuits that TFET technology has a larger dynamic range (DR) (>60%) and better 1 V-sensitivity than the 32 nm planar technology has. Note that, in this case, the figure of merit defined by the Voltage Conversion Efficiency (VCE) and Power Conversion Efficiency (PCE) remains somewhat similar. On the other hand, topology proposing better VCE at the cost of low PCE shows lower performance than expected in 32 nm than in reported data for larger technology nodes (e.g., 180 nm). The TFET-based circuit shows a PCE of 70%, VCE of 82% with an 8 dB DR (>60%), and the best 1 V-sensitivity in this work. Because of the low-bias condition and the good reverse current blocking (unidirectional channel), the TFET offers new perspectives for RF-DC rectifier/multiplier topology, which are usually limited with planar technology.

Keywords: TFET; 32 nm; multiplier; full wave rectifier; CCDD; PCE; VCE

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1. Introduction

CMOS rectifier circuits are gaining interest for many system implementations. Indeed, the Internet of Things (IoT) requires more and more compact systems, resulting in the integration of the same monolithic chip (generally) sensors, memory, microprocessor, BT port, and power supply blocks. Such system integration is made possible by applying the System-on-Chip (SoC) strategy which is essentially employed for smart object conception. Today, IoTs or smart objects are now part of an important electronic market motivated by the relatively new Moore than More (MtM) paradigm [1].

Many applications, such as RFID wireless sensors for biomedical devices have allowed extensive research on a specific rectifier: the RF-DC power converter. Lately, engineers have concentrated their efforts on the possibility of wireless IoT implementation, namely independent of a centralized power source. To reach this goal, the concept of harvesting energy has been recently introduced to empower the electronic system [2]. Additionally, Radio Frequency Energy Harvesting (RFEH) [3–5] devices enable the powering of a chip with RF waves from the environment of the system. Indeed, a 50 Ω-antenna harvests an RF signal and transmits it to a rectifier by means of a matching impedance network [3,4]. Then, the rectifier or RF-DC converter provides a micropower DC signal to a Power Management Unit (PMU) to supply the chip (Figure 1) [5,6]. The most challenging step remains the rectifying stage that must produce DC with a low power supply. Many different circuit

topologies and technologies should be explored to propose solutions for the future needs of RFEH systems. As IoTs are mostly supply-voltage-based systems, we are focusing on multiplier rectifier circuits. Full-Wave Rectifier Multipliers (FWRM) can be integrated with the VLSI process using CMOS technology [5,7,8]. FWRM implementation can be done using many topologies [9,10]. Most of them are commonly based on the Cross-Coupled Drive Differential (CCDD) bridge structure [7,8,10].

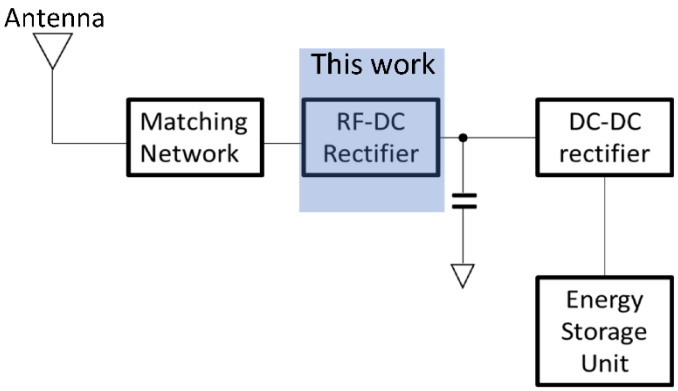


Figure 1. RF Energy Harvesting (RFEH) system description and specific focus on the rectification or RF-DC conversion stage that is the focus of this work.

To obtain the best circuit performance for a given frequency and amplitude signal, it is important to correctly size the circuit devices, namely the MOSFET gate dimensions, capacitances, and loads. In our previous studies, we developed a method to size the circuit for a given load and given frequency signal. We applied this method to different technologies such as planar 90 nm and 32 nm and no-planar technologies: FinFET and TFET [11]. Additionally, we also found out that the choice of a well-optimized topology could significantly influence the metric performance [12,13]. However, all these studies never went through post-layout simulations or considered parasitic components for a realistic assessment of the performance.

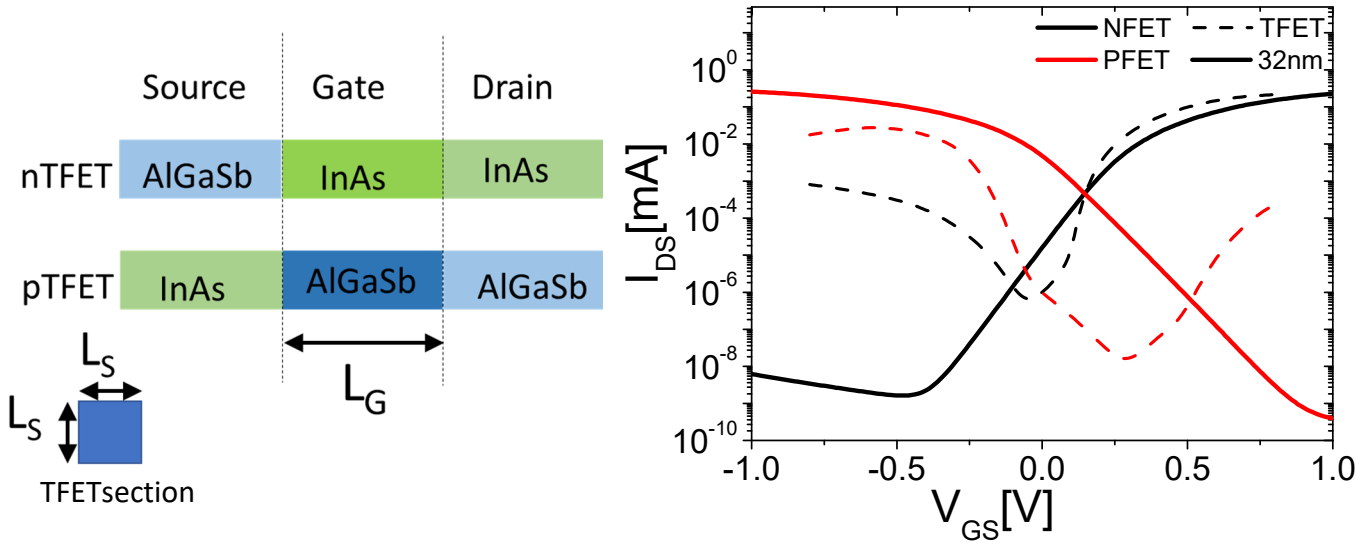
In the present work, we aim to establish the best topology and technology for RFEH applications. To reach this objective, we based our study on results obtained in our previous works. We also use mainly two specific figures of merit (FOM), which are defined as Power Conversion Efficiency (PCE) and Voltage Conversion Efficiency (VCE). Therefore, we have selected from our previous studies the two most interesting technologies: 32 nm planar and TFET [12,13]. The first one is an advanced node for conventional planar technology, while the second is an emergent technology providing an exceptional swing (<<60 mV/dec) and is supposedly ideal for low power applications [14–17]. For this study, we also decided to focus on two topology arrangements [10]: the V_{TH}-compensated cascaded CCDD bridge rectifier [18] and multiplier CCDD [19]. For these specific technological solutions, we have implemented the layout (32 nm) or applied parasitic component model (TFET) and compared these circuits to assess a realistic performance and FOM of such FWRM circuits. This study is divided as follows. First, we describe the different topologies, the 32 nm iPDK, and, above all, the TFET physics-based models for circuit simulations [20,21]. For the latter, we have included a physics approach that considers the parasitic components [22] for a fair comparison for the post-layout simulation results. Then, the topologies are optimized using the same method from our previous work [13], and the simulations are carried out using the circuit TCAD simulator Synopsys. Finally, the results are compared, and FOM have been applied to assess the circuit and obtain a metric of performance in each case. We conclude on the effect of the 32 nm and TFET technologies on the different studied topologies.

2. Technology and Topology

2.1. Technology

The planar technology is well known and would benefit a reliable and affordable technology library. Furthermore, for the 32-nm MOSFET, we are using the 28/32 nm iPDK developed by TSMC. In addition to electrical HSPICE-based simulation, we had the possibility of drawing the layout of our circuit. The latter gives a realistic behavior of the circuit thanks to post-layout simulations. We also considered non-planar TFET technologies for more advanced nodes. However, TFET is not a commercial technology, as the 32 nm is. Therefore, there is no PDK, and we cannot propose a layout. However, it is a proposed physics model for the TFET that enables the simulation of the circuit with parasitic components similar to a real layout. in this way, we emulated a TFET "virtual layout" to make a fair comparison with the post-layout simulation of the 32 nm. As a result, the electrical behavior of the TFET was provided by the lookup tables (LUT). Then, these LUTs were imported into the Cdesigner environment of Synopsys by means of Verilog-A description languages-enabling circuit simulations.

These LUTs were built based on I-V and C-V characteristics obtained from a physics-based model applied to the TCAD-Sentaurus simulator. The considered TFETs were Nanowire (NW) structures made of III-V materials [20,21] and described in Figure 2a. For this kind of TFET, the use of III-V materials has many advantages for the ON state current. Indeed, the heterojunction increases the tunnel effect (energy bands distortion) to maximize the charge carrier injection density. Then, the charge carrier benefits further from a relatively high mobility by means of the effective mass of the AlGaSb (p-type) and InAs (n-type) in the channel conduction.



(**a**) (**b**)

Figure 2. (**a**) Nanowire (NW) structure of the considered TFET. The NW section is a square of side L_S =7 nm. The gate length is L_G = 20 nm, and the gate dielectric consists of 2.3 nm of $Al2O_3$ all around the gate portion, which results in aa EOT = 1 nm; not shown. (**b**) The simulation of I-V characteristics of the 32 nm MOSFET and the Tunnel-FET for p- and n-FET.

However, and as for 32 nm planar technologies, lower I_{ON} was observed for the p-type transistor, Figure 2b. This is explained by a lower doping of the p-TFET source (5× lower) to avoid degeneracy and keep a steep enough subthreshold slope (Sub-S); InAs counts with about 10× lower DOS in the conduction band. Finally, the n-TFET has a lower Sub-S than p-TFET for $V_{GS} < 0.1$ V, as in Figure 2b, explained by Band-to-Band-Tunneling phenomena (direct gap of InAs) producing stronger ambipolarity [23]. Note that gradual doping at the drain was considered to reduce this effect and to produce a good enough I_{ON}/I_{OFF}

ratio. Regarding the 32 nm technology, the main difference between the p- and n-type is mainly explained by a lower hole mobility (2–3× lower). As a result, the TFET produces a much larger current than the 32 nm MOSFET in the subthreshold regime, namely in the range of V_{GS} = 0.1–04 V [24], while this one in the inversion regime or above the threshold voltage (V_{TH}) produces a larger current. Regarding the parasitic components, the 32 nm iPDK includes these when the circuit is laid out, so for more realistic results, we carried out post-layout simulations. In the case of the TFET, the leakage current (I_{OFF}) and extrinsic parasitic capacitive components were calibrated and included in the simulation by means of the extrinsic model for the TFET developed in [22].

2.2. Topology

It is obvious but essential to highlight the fact that the rectifier circuit must consume the lowest energy and display the highest power efficiency during the working cycle and the OFF/ON(ON/OFF) state transitions [18]. As for the RF-DC power converter, the signal level can be very low (hundredth of mV). The range of the wireless powering system is mainly determined by the rectifier sensitivity. This one is defined as the minimum input RF power to obtain enough output DC voltage to supply the chip or circuit [10]. This sensitivity must be achieved at the highest PCE possible.

In addition, for the CMOS rectifier, the limiting parameter is the control of the V_{TH}. As a matter of fact, if this one is too high, a large part of the signal is consumed by the transistor, while if it is too low, the reverse current (OFF state) overwhelms the charging process, which results in PCE being lower than expected. Among the different existing topologies [18,19,25], the Cross-Coupled Differential Drive (CCDD) [8,11] might be the best strategy for RF signal rectification. In the CCDD, the peak-to-peak RF signal is applied as a differential input at the gate/source transistor, providing a DC common mode as static bias to overcome the V_{TH} and a differential mode for an active control of the rectification. Therefore, this topology provides a low sensitivity by a dynamic gate bias control [26].

We also expected good PCE because during the charging time, the transistor works in the triode regime with low overdrive. However, this last effect is mitigated by a reverse current of the p-type transistors connected at the load once the output voltage is larger than the RF input. A way to reduce this reverse current is, for instance, to make use of the body-biased technique. In this case, the n-/p-type body bias enables, in addition, a dynamic control of the V_{TH} [13,19,27] so that both the large charging current and the small reverse current are obtained without any depression on the load charging current. Note that this technique is worthwhile for low input power since it limits the dynamic range, hence this technique involving a subthreshold regime operation of the transistor [10].

Furthermore, to gain a larger DC rectified voltage, a Voltage Multiplier (VM) should be considered. In this type of circuit, the part of the energy carried by the current is transferred to the voltage by means of capacitive components [28]. Mostly, a VM is made of cascaded FWR [4,7,17], as shown in Figure 3a. However, the cascading rectifier has a detrimental effect on the V_{TH} control [16,20]. Indeed, after each stage, the bias control through the DC common mode at the gate transistor is degraded by overdrive increase. In our previous study, we obtained that VMs with the best PCE and VCE were the ones using two-stage FWR composed of a conventional CCDD as a first stage and a body-biased CCDD as a second stage to consolidate the bias control of the transistor; see Figure 3b.

Another strategy to overcome this difficulty consists of producing an auxiliary bias to level up the gate bias for the second stage [16]. This can be carried out by means of a dynamic change of the common mode (DC) using a level shift of the RF signal input of the DC component from the first stage through the capacitor Cr in Figure 3c. This topology has also the advantage of offering a good drive capability, which offers several choices for the load.

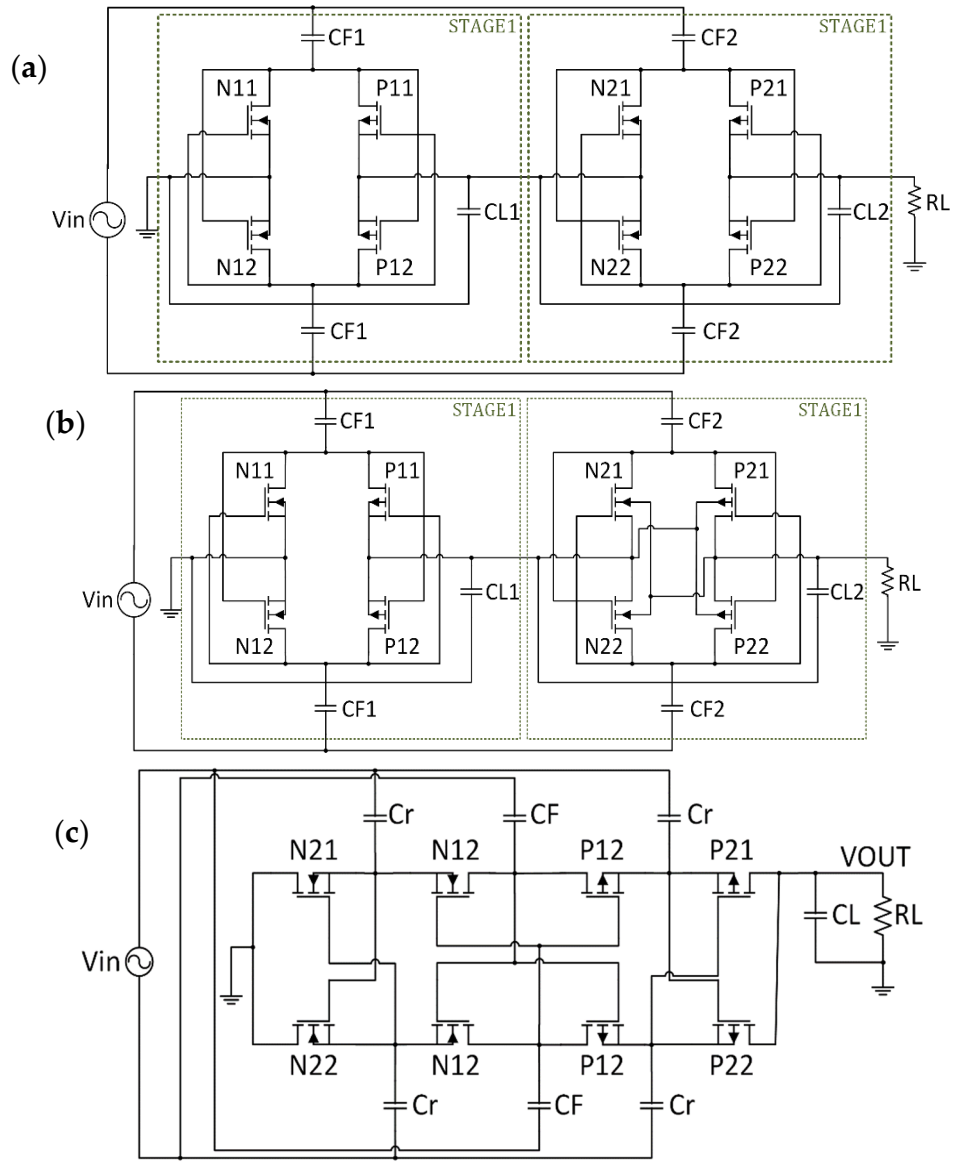


Figure 3. Different CCDD-based topologies used in this work: (**a**) conventional CCDD or CDC (only TFET), (**b**) conventional/body bias or CDB (only for 32 nm), and (**c**) bias control by level shift or CDC (32 nm and TFET). Note that CDN is not a cascaded configuration as in the topology CDC and CDB.

All the aforementioned topologies were employed for the present study. For all considered cases, the results are benchmarked with the conventional topology of the CCDD (no body bias, no level shift) in Figure 3a and are labelled as CDC. Topology in Figure 3b are only used for the 32 nm technology node since this topology requires a body bias, which is not physically possible for TFET technology; this topology is labelled as CDB. Finally, the topology in Figure 3c is labelled as CDN, and it was implemented with the two proposed technologies: 32 nm and TFET. In all designs in Figure 3, CF or Cr is the fly capacitance, and CL is the load capacitance. The latter is involved in the smoothing of the signal or ripple reduction. Therefore, if well-sized, it does not discharge during the signal cycles to enable a DC output.

We used mainly two figures of merit (FOMs). First, there was Power Conversion Efficiency (PCE), measuring the output power (P_{out}) and w.r.t. the input power (P_{in}) and defined by (2)

$$\mathrm{PCE} = \frac{\mathrm{Pout}}{\mathrm{Pin}} \times 100 \tag{1}$$

Second, there was Voltage Conversion Efficiency (VCE), measuring the obtained output voltage (v_{out}) and w.r.t. the ideal DC output (v_{out_id}) and defined by (2):

$$VCE = \frac{1}{n.T}\int_{t_0}^{t_0+T}\frac{v_{out}(t)}{v_{out\_id}}dt \times 100 \quad (2)$$

For a pure single-tone sine signal we obtained that $v_{out\_id} = \frac{2}{\pi}.\ v_{in\_MAX}$ where v_{in_MAX} is the maximum or amplitude of the input signal. It is worth noting that the voltage conversion ratio is n = 2 based on the circuit topologies used in this work. Note that the ripple factor was negligible since the CL was optimized to properly smooth the output signal; more details will be given in the next section. As explained previously, it is important that a rectifier/VM consume the lowest power of the harvesting system, and this is measured by the PCE. However, good PCE (>60%) is reached for the largest range of input power, and this is assessed by the Dynamic Range (DR) [4]. Indeed, the DR is limited by the reverse leakage phenomenon for high input power (P_{in}), and this explains the PCE degradation for such P_{in} [29]. Finally, we also considered that these previous requirements had to comply with a good sensitivity defining the threshold P_{in} for V_{out} = 1 V and, therefore, had to be the lowest possible. For all tests, the input value was a pure sinusoidal signal set at f = 950 MHz varying from 0.1 to 0.8 to match with UHD RFID [17] and biomedical application [2,10]. Note that for the 32 nm technology node, we extended the RF input amplitude up to 1.2 V.

3. Design Optimization, Sizing, and Layout

3.1. Design Optimization and Sizing

The procedure to optimize and design the circuits was based on the method described in [30]. However, in our case, the capacitance and transistor were sized to maximize the PCE in perspective to yield no power losses [13,14]. For each considered technology, the topology was optimized by fixing the load resistance at 50 kΩ and the channel length of the transistors (N- and P-type) to the same value, in the same circuit. For each topology, we applied also the next constraint: the width of all NFET transistors had to be identical in the same stage and the same for the PFET. The optimization procedure was based on the sweep of each capacitor, namely CF or Cr then CL, for a given fixed width transistor value until we reached simultaneously the maximum PCE and VCE and the lowest ripple factor. Then, to obtain the capacitance values, the width of the transistor was swept until we reached the maximum VCE on one side and the maximum PCE on the other side. This procedure enabled us to design symmetrical topologies with good control of the channel resistance. Note that the latter is primordial for the lowest technology node as the 32 nm one. The results of this optimization technique are shown in Figure 4, where the PCE and VCE are plotted as a function of the N/P-MOSFET widths for the TFET and 32 nm technologies. In the following, we consider only the solutions where the PCE and the VCE are maximized by the circuit sizing. Based on that, the transistors and capacitors sizing of the optimized CDC, CDB, and CDN topologies are given in Table 1. Note that the total width is obtained for each transistor, summing all the fingers.

Table 1. Sizing of the two-stage CCDD Circuits.

Circuit Sizing	CDC (TFET)		CDC (32 nm)		CDB (32 nm)		CDN (TFET)	CDN (32 nm)
Stage	1	2	1	2	1	2	1	1
CF [pF]	10	20	10	10	10	10	10	1
Cr [pF]	-	-	-	-	-	-	5	1
CL [pF]	7	1	10	10	10	10	10	1
RL [kΩ]	50		50		50		50	50
Total Wn [µm]	40(300 NW)	40(300 NW)	2(10 Fin)	2(6 Fin)	2(10 Fin)	2(10 Fin)	2	2(1 Fin)
Total Wp [µm]	40(300 NW)	40(300 NW)	3.5(10 Fin)	3.5(14 Fin)	3.5(14 Fin)	3.5(14 Fin)	3.5	3.5(10 Fin)
Length [nm]	30		30		30		30	30

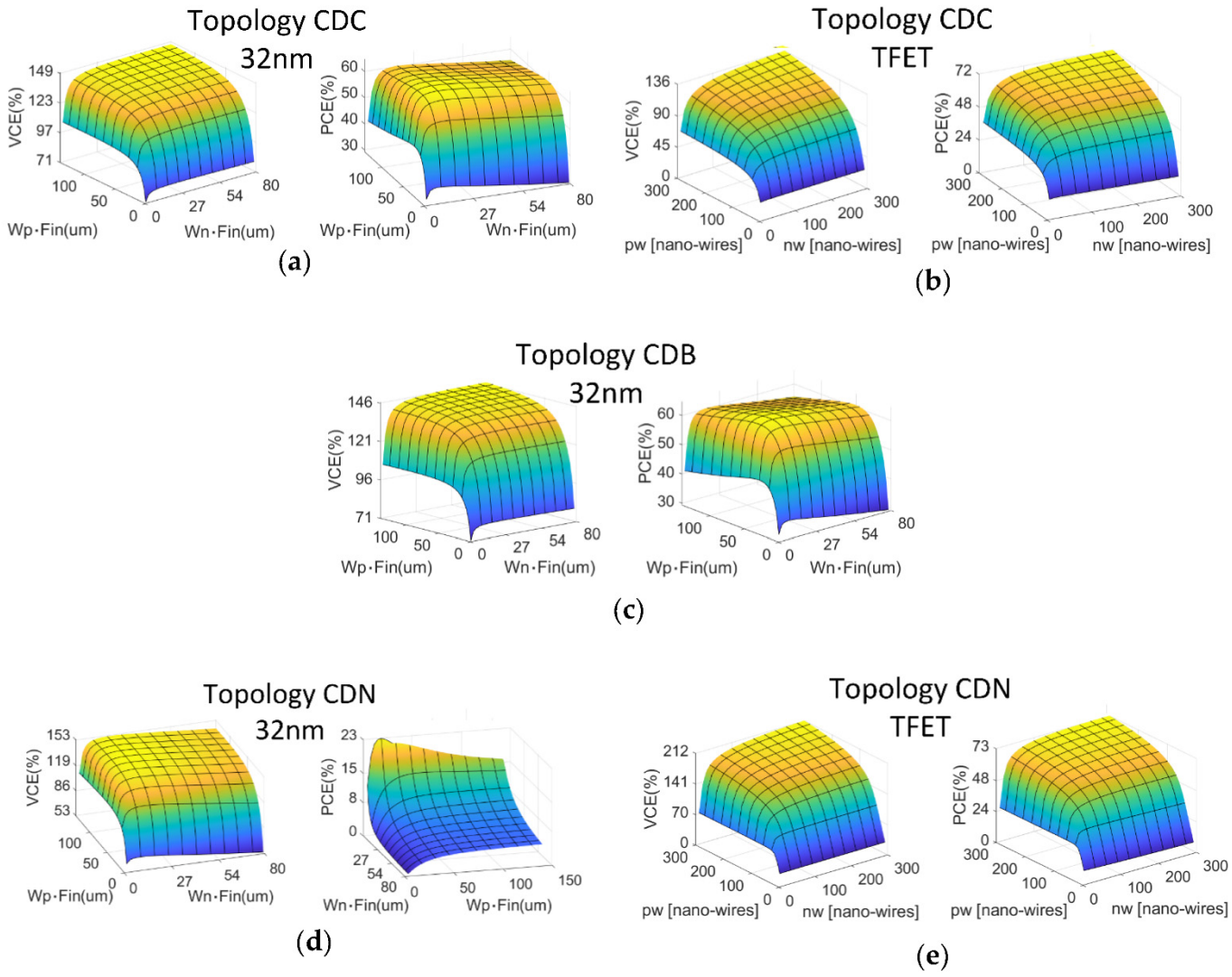
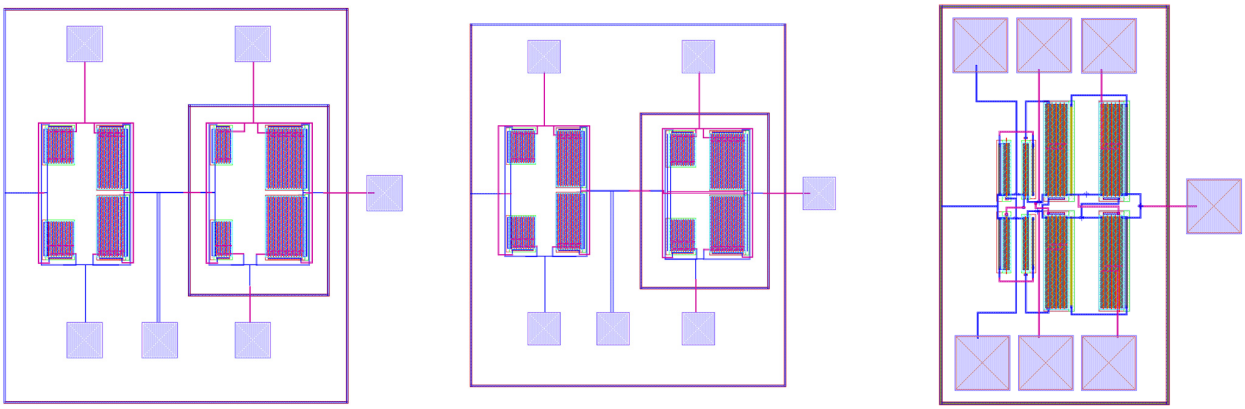


Figure 4. VCE and PCE optimization for circuit sizing of the different CCDD-based topologies studied in this work: (**a**,**b**) the conventional topologies [Figure 4a] in 32 nm and TFET, respectively; (**c**) the first stage is conventional and the second stage is body bias [Figure 4b] with only 32 nm technology; (**d**,**e**) two-stage with bias level shift in the second stage [Figure 4c] for 32 nm and TFET techno, respectively. The load is fixed to 50 kΩ and Ln = Lp = 30 nm for the 32 nm technology. For the TFET, see the details in Figure 2.

3.2. Layout and Parasitic Components

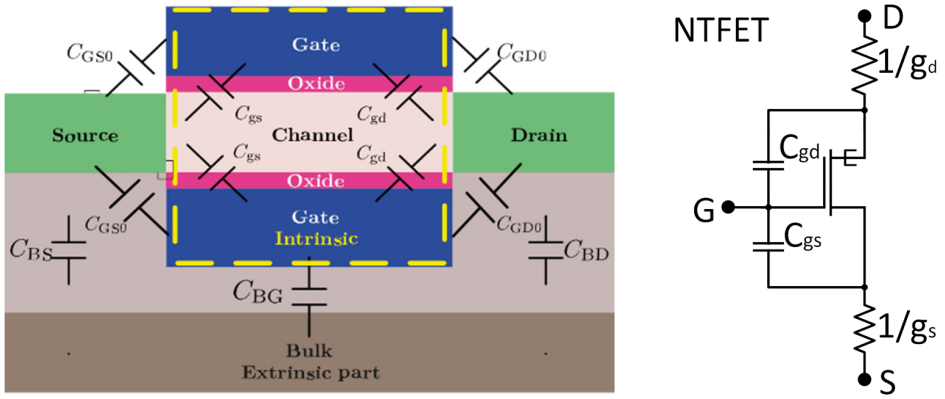
As explained previously, the best way to assess and predict the circuit performance is to simulate the rectifier circuit, including the parasitic components caused by the circuit integration into material. To do so, we laid out the 32 nm circuit using the commercial PDK from TSMC. The developed layouts of the CDC, CDB, and CDN using the 32 nm technology are shown in Figure 5. It is important to highlight that the optimization of the capacitor size was considered for the layout, above all in the LPE extraction step. For the load, a specific port was considered for the connection to the next circuit (e.g., the DC-DC converter). Regarding the TFET technology, there is no commercial design kit; therefore, we could not consider a standard for the TFET-based circuit layout. However, many works have reported TFET fabrication [15,24] and some proposed parasitic component models resulting from the material integration of the TFET. In the present study, we used the model proposed in [23] to provide parasitic components, as in Figure 6a, with an equivalent circuit shown in Figure 6b. We took good care to use the proper physics constants and

descriptions related to the materials used to implement our TFET technology: AlGaSb and InAs. Then, we assumed that we would obtain the most realistic results for the use of the TFET technologies with the considered topologies (CDC and CDN). It is worth noting that we did not consider the RC effects of the path from the circuit to Cr, CF, and CL for the TFET since no model considers it. However, for the 32 nm, we considered both cases with and without these specific effects, and no more than a 1% variation in the results was observed. Therefore, we assumed that their effect was negligible for the comparison of both technologies.



(**a**) (**b**) (**c**)

Figure 5. Layout of the topology CDC (**a**), CDB, (**b**) and CDN (**c**) in 32 nm with, the iPDK using Cdesigner. The capacitors are not represented because they are occupying much more space in the layout. In pratice, the large capacitors can be used in the metal layers.



(**a**) (**b**)

Figure 6. Description of the model used for the parasitic components of the TFET: (**a**) the capacitive contribution related to the TFET architecture (transversal cut) considered based on the model in [22], (**b**) the electrical circuit model resulting from the capacitive parasitic components.

4. Results and Discussion

The FOMs (PCE and VCE) were extracted from the electrical simulations of the layouts in Figure 5, and the models described in Figure 6 were shown in the previous section. We considered the 32 nm planar and TFET technologies applied to the three different circuit topologies (Figure 3). Note that the results are benchmarked with the ones provided by the circuit simulation of the conventional CCDD labelled as CDC (Figure 3a) [13].

As expected in Figure 7a, the PCE increases as a function of the P_{in} up to a maximum (PCE_{peak}), which is the best yield for the circuit in terms of power consumption and provided output power. In the best conditions, this peak should coincide with the maximum

output voltage (V_{out}) that can be delivered to the circuit for the best yield. In this regime (up to the peak), the PCE suggests that the transistors in the circuit, under the bias condition and for given input level, work in a such way that in OFF state, they properly block the reverse leakage current. Therefore, the peak suggests that the gate overdrive satisfies the least or lowest charge displacement on the gate to switch the transistor from the cut-off to the triode regime.

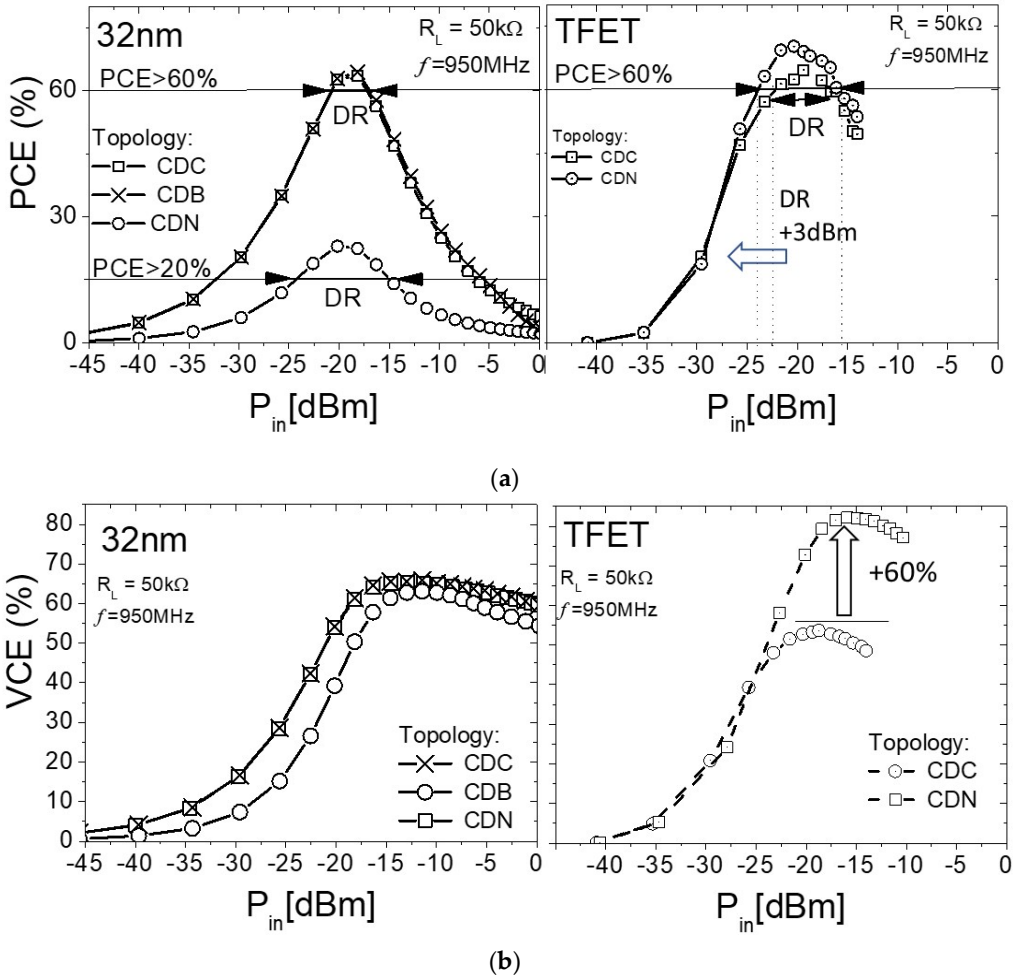


Figure 7. The FOM to assess the performance of the different topologies for different technology: (**a**) the PCE and (**b**) the VCE. In (**a**), the PCE for the TFET is the DR (>60%), which is increased from 5 dBm to 8 dBm or 3 µW to 6 µW. For the 32 nm, the DR is not improved if we use the back bias to control the V_{TH} (CDB circuit). The PCE is importantly degraded for the CDN topology with 32 nm.

Once the peak is reached, the PCE decreases as the P_{in} increases, suggesting that the transistors are not able to block the leakage current since the signal level is too high; this is equivalent to the peak reverse voltage for diode devices. For the 32 nm, this is clearly explained by the source/drain leakage junction, while for the TFET, this is explained by the ambipolarity phenomenon [23,31]. As explained in Section 2, the use of the topologies should improve these intrinsic technology limits. We stress that the performance metric used to assess how much P_{in} the circuit can hold in a given PCE is provided by the DR. In our case, we decided to define two DRs: one for PCE > 60% and one for PCE > 20%. In the case of the TFET, the DR increased by 200% when we used the CDN topology instead of the CDC topology (conventional CCDD). We also observed that the TFET always offered a much higher DR than 32 nm (1 to 4 dB larger). In addition, the conventional topology (CDC) designed with the 32 nm iPDK displayed a lower PCE_{peak} (−4%) compared to the one designed with the TFET. This peak is slightly improved when we use the CDN topology

for the TFET but is widely degraded with the 32 nm and the latter can only offer good performance for a DR > 20% (Figure 7a). Note that it was reported that a PCE of about 40% in other works used the same topology in 180 nm technology (planar). On the other hand, the TFET technology demonstrated that low voltage activation greatly increases the PCE for such design strategy, offering new options for the designer. It is important to highlight that the TFET physics model used in this work is limited to V_G = 0.8 V. If one considers larger voltage, low ON-currents caused by the conduction mechanism of the TFET would increase the resistance current in the triode regime (high R_{ON}), and the ambipolarity phenomenon would increase the reverse current leakage in OFF state. As a result, the PCE most importantly decreases for large V_G and P_{in} with the TFET.

As compared with our previous work [8–10], we would have expected an improvement of the PCE with the body-bias (CDB) topology with the 32 nm; this topology is not applicable for TFET technology since no back contact is physically possible [28]. However, in Figure 7a, we can observe that there was no significant change between the CDC and CDB topology. We can assume that for such topology, the conventional planar 32 nm faced large electrostatic effects that prevented a good control from the back gate. We would suggest for a future work to apply to this topology the FDSOI technology to answer this question. On the other side of the VCE, Figure 7b, the maximum value is limited at 65% for the CDC and CDB topologies with the 32 nm technology, while the TFET-based circuits show VCE at 15% lower. However, an improvement of 60% is observed, while the CDN topology is considered with the TFET.

The output voltage (V_{out}) is plotted in Figure 8a as a function of the input power (P_{in}) and the input voltage (V_{in}) in Figure 8b. The 1 V-sensitivity extracted in Figure 8a shows that TFET-based circuits presented a better sensitivity with a 10% improvement with the CDC topology (−14 dBm) and 30% with the CDN topology (−15.6 dBm). Regarding the 32 nm-based circuits, sensitivity was at best −12.5 dBm with the CBC, CDB, and CBN topologies. We also introduce the Yield Factor, which is defined as DR (>60%)/Sensitivity (1 V).

This one is the maximum when we consider the CDN topology with the TFET technology, which is interpreted as the circuit that offers the largest DR and the lowest sensitivity for the different studied cases. All the FOM and performance assessments are summarized in Table 2.

As a result, for the 32 nm with conventional CCDD, we obtained within the DR (>60%) a V_{out} of 0.55 to 0.75 V (VCE maximum of 65.5%) providing an output power ranging from 8.4 to 19.4 µW with a V_{out} = 0.7 V for a PCE_{peak} of 64%. An attempt to improve the performance by controlling the V_{TH} by a bulk contact (CDB topology) did not significantly improve these results, and, more critically, the DR barely improved (4 dB against 3.5 dB), suggesting that the back bias is not effective for this technology for the CCDD topology since reverse currents for a larger bias cannot be sufficiently controlled this way. By comparison, the conventional CCDD using the TFET present within the DR (>60%) has a V_{out} ranging from 0.37 to 0.72 V (VCE max of 53%), providing an output power ranging from 6.2 to 19.5 µW. It is worth remembering that an increase from 3.5 to 5 dB was obtained with the TFET in comparison with the 32 nm obtained with the CDC circuit. This also led to a 1 dB improvement of the 1 V-sensitivity. Interestingly, the most significant performance improvement was obtained with the CDN topology. Indeed, it was reported that with planar technology, this topology shows good VCE at the price of a reduced PCE with a 50 kΩ-load [6]. In our previous work, we already observed that the scaling from 90 nm to 32 nm was not so advantageous since the obtained VCE remained close to the one from the conventional CCDD topology for a PCE in the range of only 25–35%. In this present work, we obtained similar PCE with V_{out} within the DR (>20%), which ranged from 0.25 to 0.6 V for an output power from 4 to 36 µW. In that case, the 1 V-sensitivity was not lower than 12.5 dB, suggesting a circuit producing an output of 1 V for a P_{in} = 224 µW. However, and as shown in Figures 7 and 8, the design of the CDN topology that used the TFET technology showed interesting results. In that case, a maximum VCE of 82% with a peak of PCE of 70% was obtained. In that case, within the DR > 60%, a V_{out} ranging from

0.45 to 1 V (0.9 at PCE_{peak}) with an output power ranging from 6.17 µW to 35 µW (13 µW at the peak) and a 1 V-sensitivity of −15.6 dB (the lowest) was obtained. In other terms, the 1 V-level output was produced in the range of the considered DR (60%), which meant a good power yield; note that it was the largest DR since it was about 8 dB.

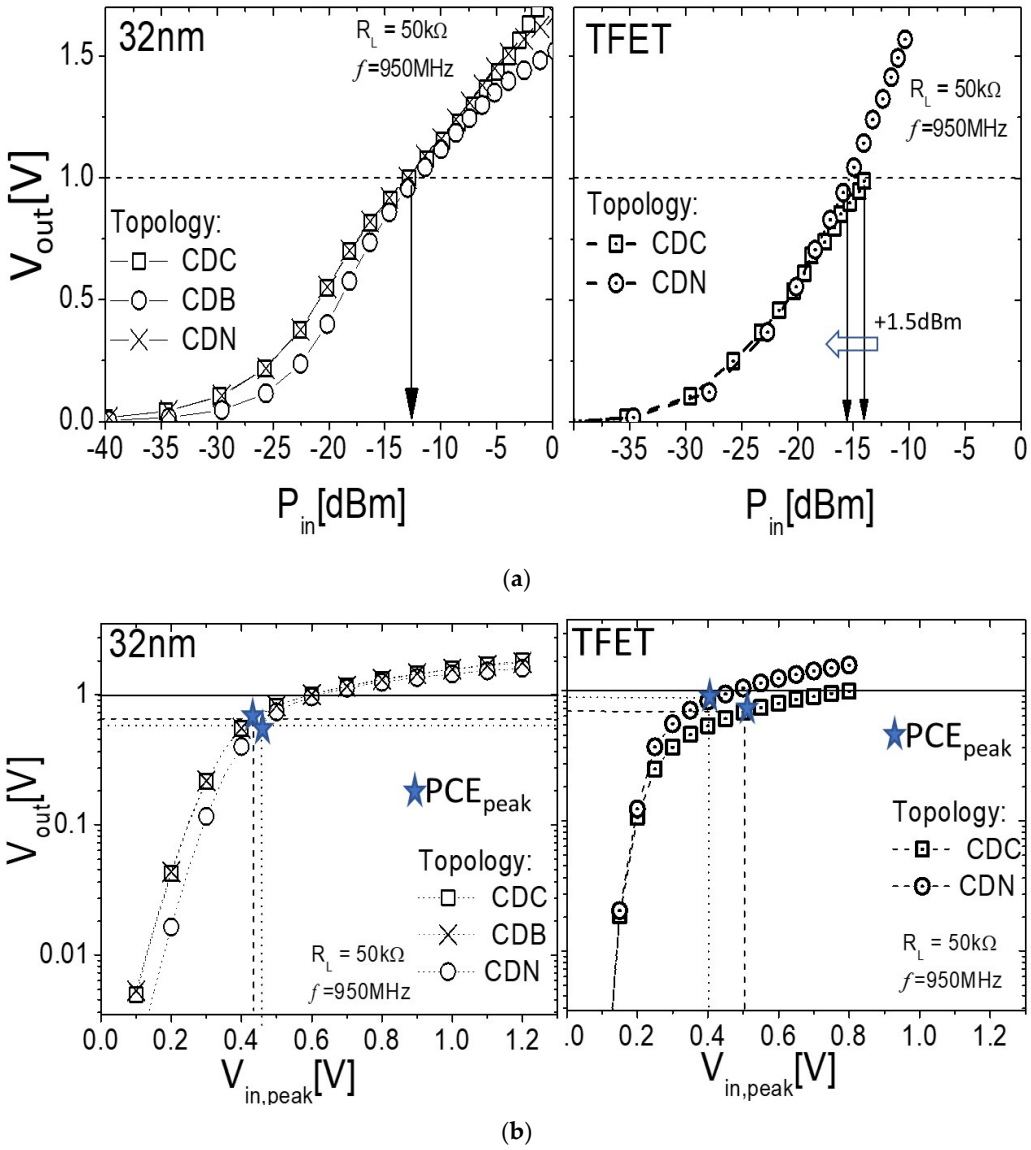


Figure 8. Output Voltage (V_{out}) as a function of (**a**) the Input Power (P_{in}) and (**b**) the input Voltage (P_{in}).

Table 2. FOMs and performance assessments.

	CDC		**CDB (Only 32 nm)**	**CDN**	
Techno	32 nm	TFET	32 nm	32 nm	TFET
PCE_{peak} (%)	64	64	64	23	70
VCE_{peak} (%)	65.5	53	65	63	82
$Vout@PCE_{peak}$[V]	0.65	0.7	0.65	0.6	0.9
$P_{in}@PCE_{peak}$ [dBm]	−18.5	−19.5	−18.5	−19.4	−20.2
DR (>60%) [dBm]	3.5	5	4	N/A	8
Sensitivity@ 1 V [dBm]	−12.5	−14	−12.5	−12.5	−15.6
Yield Factor (%)	28	36	32	-	51

As a result, the TFET-based rectifier/multiplier enables a good PCE for larger input power. It is worth remembering that the advantages of the TFET are a low switching energy at the gate resulting from a subthreshold slope below the 60 mV/dec planar technology limit, along with a V_{TH} in the range of 200 mV and an extremely high output impedance [22,32]. Furthermore, the used TFETs were unidirectional, producing an extremely low reverse leakage current [20,21,32]. All these features explain the very good PCE performance with both topologies (Table 2) and the highest V_{out} values for $V_{in} \approx V_{TH}$ and low P_{in} (Figure 8). However, in the triode regime ($V_{in} >> V_{TH}$), the TFET yielded a low output current in ON state and too large a reverse current caused by ambipolarity in OFF state for large amplitude input signal. Additionally, we may expect improvement of the TFET technology to obtain a higher DR [33].

To conclude, the rectifier circuit needs an active switching device that can work with a low power budget. This means that in the range of small signals, as mostly observed for the RF-DC converter, topologies such as the CDN can keep improving performance through scaling only if we switch to other technologies than planar, and the TFET is a very good example for the purpose of this goal.

5. Conclusions

Conventional and based CCDD circuit topologies have been considered to implement multipliers for RFEH systems. These circuits have been optimized for the 32 nm planar and TFET nonplanar technologies by including the parasitic effect, resulting in a layout implementation. The performance metrics based on PCE and VCE FOM were extracted and compared. It resulted that the conventional circuit topology designed with TFET technology presented better dynamic range (PCE > 60%) and 1 V-Sensitivity (1 dB) performance than the one designed with the 32 nm. The performance improvement became considerable during the design of the CDN topology: the TFET circuit simulations demonstrated a +3 dB of DR (60%) and a reduction of almost 3 dB for the 1 V-sensitivity. Furthermore, the latter showed a 1 V output within the DR (>60%).

We conclude that from 32 nm, the planar technology shows some weakness for such a circuit. For instance, the body bias contact topology does not bring better DR, suggesting a V_{TH} control less efficient than expected and likely explained by weak control of electrostatic. A FDSOI-based design could answer this problem. On the other hand, the specific features of the TFET, such as a low switching energy at the gate resulting from a subthreshold slope below the 60 mV/dec with a V_{TH} in the range of 200 mV and an extremely high output impedance, support superior performance with specific topology. Furthermore, TFET technology opens new perspectives for CCDD bridge circuits to proposes solutions regarding the future needs with multiplier rectifier circuits used for RFEH systems.

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References

1. Clavelier, L.; Deguet, C.; Di Ciccio, L.; Augendre, E.; Brugere, A.; Guguen, P.; Le Tiec, Y.C.; Moreau, H.; Rabarot, M.; Signamarchaix, T.; et al. Engineered Substrates for Future More Moore and More than Moore integrated device. *IEEE IEDM* **2010**, 2.6.1–2.6.4. [CrossRef]
2. Poon, C.Y.; Lo, B.P.L.; Yuce, M.R.; Alomainy, A.; Hao, Y. Body sensor networks: In the era of big data and beyond. *IEEE Rev. Biomed. Eng.* **2015**, *8*, 4–16. [CrossRef]
3. Hsieh, P.; Chou, C.; Chiang, T. An RF Energy Harvester With 44.1% PCE at Input Available Power of −12 dBm. *IEEE Trans. Circuits Syst. I Regul. Pap.* **2015**, *62*, 1528–1537. [CrossRef]

4. Khan, D.; Abbasizadeh, H.; Kim, S.-Y.; Khan, Z.H.N.; Shah, S.A.A.; Pu, Y.G.; Hwang, K.C. A Design of Ambient RF Energy Harvester with Sensitivity of −21 dBm and Power Efficiency of a 39.3% Using Internal Threshold Voltage Compensation. *Energies* **2018**, *11*, 1158. [CrossRef]
5. Wang, J.; Jiang, Y.; Dijkhuis, J.; Dolmans, G.; Gao, H.; Baltus, P. A 900MHz RFEH System in 40 nm CMOS Technology with Efficiency Peaking at 47% and Higher than 30% over 22 dB Wide input Power Range. In Proceedings of the 43rd IEEE European Solid State Circuits Conference (ESSCIRC), Leuven, Belgium, 11–14 September 2017.
6. Ballo, A.; Bottaro, M.; Grasso, A.D. A review of power management integrated circuits for ultrasound-based energy harvesting in implantable medical devices. *Electronics* **2021**, *11*, 2487. [CrossRef]
7. Sokrani, M.R.; Khodan, M.; Hamidon, M.N.B.; Kamsani, N.A.; Rokhani, F.Z.; Bin Shafle, S. An RF Energy Harvester System Using UHF Micropower CMOS Rectifier Based on a Diode Connected CMOS Transistor. *Hindawi Sci. World J.* **2014**, *24*, 963709.
8. Kotani, K.; Sasaki, A.; Ito, T. High-Efficiency Differential-Drive CMOS Rectifier for UHF RFIDs. *IEEE J. Solid-State Circuits* **2009**, *44*, 3011–3018. [CrossRef]
9. Ballo, A.; Bottaro, M.; Grasso, A.D. A review of charge pump topologies for the power management of IoT nodes. *Electronics* **2019**, *8*, 480. [CrossRef]
10. Chong, G.; Ramiah, H.; Yin, J.; Rajendran, J.; Mak, P.; Martins, R.P. A Wide-PCE-Dynamic-Range CMOS Cross-Coupled Differential-Drive Rectifier for Ambient RF Energy Harvesting. *IEEE Trans. Circuits Syst. II: Express Brief* **2021**, *68*, 1743–1747. [CrossRef]
11. Procel, L.-M.; Paredes, J.; Trojman, L. Comparison of Different Technologies for Transistor Rectifiers Circuits for Micropower Energy Harvesters. In Proceedings of the Latin American Electron Devices Conference (LAEDC), Armenia, Colombia, 24–27 February 2019; pp. 1–4.
12. Rivadeneira, D.; Villegas, M.; Procel, L.M.; Trojman, L. Optimization of Active Voltage Rectifier/Doubler Designed in 90 nm Technology. In Proceedings of the IEEE LASCAS, San Jose, Costa Rica, 25–28 February 2020; pp. 1–4.
13. Trojman, L.; Rivadeneira, D.; Villegas, M.; Acurio, E.; Lanuzza, M.; Procel, L.-M. RF-DC Multiplier for RF Energy Harvester based on 32 nm and TFET technologies. In Proceedings of the IEEE LASCAS, Arequipa, Peru, 21–24 February 2021; pp. 1–4.
14. Gupta, N.; Makosiej, A.; Amara, A.; Vladimirescu, A.; Costin, A. *State-of-the-Art TFET Devices. Chapter 2 of Book: TFET Integrated Circuits*; Springer Link: Berlin/Heidelberg, Germany, 2020; pp. 5–15.
15. Datta, S.; Liu, H.; Narayanan, V. Tunnel FET technology: A reliability perspective. *Microelectron. Reliab.* **2014**, *54*, 861–874. [CrossRef]
16. Gupta, N.; Makosiej, N.; Amara, A.; Vladimirescu, A.; Costin, A. *SRAMs, Chapter 3 of Book: TFET Integrated Circuits*; Springer Link: Berlin/Heidelberg, Germany, 2020; pp. 17–43.
17. Arevalo, A.; Liautard, R.; Romero, D.; Trojman, L.; Procel, L. New Insight for next Generation SRAM: Tunnel FET vs FinFET for Different Topologies. In Proceedings of the 32nd Symposium on Integrated Circuits and Systems Design (SBCCI), Sao Paulo, Brazil, 26–30 August 2019; pp. 1–6.
18. Potocny, M.; Stopjakova, V.; Kovac, M. Self Vth-Compensating CMOS On-Chip Rectifier for Inductively Powered Implantable Medical Devices. In Proceedings of the 2018 IEEE 21st International Symposium on Design and Diagnostics of Electronic Circuits & Systems (DDECS), Budapest, Hungary, 25–27 April 2018.
19. Chouhan, S.S.; Halonen, K. A 0.18 μm CMOS voltage multiplier arrangement for RF energy harvesting. Analog Integr. *Circ. Sig. Process* **2017**, *92*, 343–353.
20. Strangio, S.; Settino, F.; Palestri, P.; Lanuzza, M.; Crupi, F.; Esseni, D.; Selmi, L. Digital and analog TFET circuits: Design and benchmark. *Solid State Electron.* **2018**, *146*, 50–65. [CrossRef]
21. Baravelli, E.; Gnani, E.; Gnudi, A.; Reggiani, S.; Baccarani, G. TFET Inverters With n-/p-Devices on the Same Technology Platform for Low-Voltage/Low-Power Applications. *IEEE Trans. Electron. Devices* **2014**, *61*, 473–478. [CrossRef]
22. Horst, F.; Farokhnejad, A.; Zhao, Q.-T.; Iniguez, B.; Loes, A. 2-D Physics-Based Compact DC Modeling of DG TFETs. *IEEE Trans. Electron. Devices* **2019**, *66*, 132–138. [CrossRef]
23. Costin, A.; Gupta, H.A.; Amara, A.; Vladimirescu, A. 30-nm Tunnel FET with Improved Performance and reduced Ambipolar Current. *IEEE Trans. Electron. Devices* **2011**, *58*, 1649–1654.
24. Luong, G.V.; Strangio, S.; Tiedmann, A.; Lenk, S.; Trellenkamp, S.; Bourdelle, K.K.; Zhao, Q.T.; Manti, S. Experimental demonstration of strained Si nanowire GAA n-TFETs and inverter operation with complementary TFET logic at low supply voltages. *Solid-State Electron.* **2016**, *115*, 152–159. [CrossRef]
25. Saffarin, P.; Basaligheh, A.; Moez, K. An RF-to-DC Rectifier with High Efficiency over wide input power range for RF Energy Harvesting Applications. *IEEE Trans. Circuits Syst. I Regul. Pap.* **2019**, *66*, 4862–4875. [CrossRef]
26. Xie, Z.; Wu, Z.; Wu, J. Technique Review for differential Drive Crossing Coupling Rectifier in RF Energy Harvester. Environment and Material Science (PEEMS). In Proceedings of the International Conference on Power, Energy, Dhaka, Bangladesh, 14–16 March 2019.
27. Moghaddam, A.; Chuah, J.H.; Ramiah, H.; Ahmadia, J.; MaK, P.-I.; Martin, R.P. 73.9%-Efficiency CMOS Rectifier Using a LDCF Self-Body-Biasing Technique for Far-Field RF Energy-Harvesting Systems. *IEEE Trans. Circ. Syst. I: Regul. Pap.* **2017**, *64*, 992–1002. [CrossRef]

28. Gao, H.; Matter-Kammerer, M.; Milosevic, D.; Linnartz, J.-P.; Baltus, P. A design of 2.4GHz rectifier in 65 nm CMOS with 31% efficiency. In Proceedings of the IEEE 20th Symposium on Communications and Vehicular Technology in the Benelux (SCVT), Namur, Belgium, 21 November 2013.
29. Ouda, M.; Khalil, W.; Salama, K. Wide-Range Adaptive RF-to-DC Power Converter for UHF RFIDs. *IEEE Microw. Wirel. Compon. Lett.* **2016**, *26*, 634–636. [CrossRef]
30. Haddad, P.-A.; Raskin, J.-P.; Flandre, D. Efficient passive energy harvesters at 950 MHz and 2.45 GHz for 100 μW applications in 65 nm CMOS. In Proceedings of the 23RD IEEE International Conference on Electronics, Circuits and Systems (ICECS), Monte Carlo, Monaco, 11–14 December 2016.
31. Lanuzza, M.; Strangio, S.; Crupi, F.; Palestri, P.; Esseni, D. Mixed Tunnel-FET/MOSFET Level Shifters: A New Proposal to Extend the Tunnel-FET Application Domain. *IEEE Trans. Electron Devices* **2015**, *6*, 3973–3979. [CrossRef]
32. Strangio, S.; Palestri, P.; Lanuzza, M.; Crupi, F.; Esseni, D.; Selmi, L. Assessment of InAs/AlGaSb Tunnel-FET Virtual Technology Platform for Low-Power Digital Circuits. *IEEE Trans. Electron Devices* **2016**, *63*, 2749–2756. [CrossRef]
33. Settino, F.; Lanuzza, M.; Strangio, S.; Crupi, F.; Palestri, P.; Esseni, D.; Selmi, L. Understanding the Potential and Limitations of Tunnel FETs for Low-Voltage Analog/Mixed-Signal Circuits. *IEEE Trans. Electron Devices* **2017**, *64*, 2736–2743. [CrossRef]