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# An Optimization Framework for the Design of High-Speed PCB VIAs

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**Abstract:** Signal integrity represents a key issue in all modern electronic systems, which are strongly dominated by the extreme component density usually employed on PCBs and the associated increase in the interconnection density. The use of multi-layer structures with microstrips connected by various types of Vertical Interconnect Accesses (VIAs) calls for design strategies that reduce the impedance mismatch and signal attenuation. The paper proposes a thorough analysis of the effects associated with the VIA geometry and presents a parametric evaluation of them. The obtained results represent the starting point for a possible design procedure that manages the geometric aspects of differential VIAs, aiming to optimize their electrical performance while reducing their occupation of PCB area. The optimization technique considers a differential VIA as a four-port circuit whose characteristics are evaluated with suitable Figures of Merit (FoMs), thus striving for an optimal design obtained with closed-loop iterations. The analysis is performed in both the time (TDR: Time-Domain Reflectometry) and frequency domains (S and Z parameters), thus allowing a dramatic reduction in the number of cases to be analyzed. The procedure is thoroughly described and validated using simulation results.

**Keywords:** signal integrity; high-performance PCB; PCB interconnection optimization; VIA hole design



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## 1. Introduction and State-of-the Art

In recent decades, technological advances have forced a qualitative leap in the design of Printed Circuit Boards (PCBs) given the new requirements in terms of size reduction, increased operating speed, and component density. To meet these needs, PCB design evolved towards multi-layer structures with vertical interconnections between the different levels [1,2] with so-called VIAs, whose tight connection with technological progress was clearly described by [3]. On the other hand, Signal Integrity (SI) issues require a careful evaluation of the performance of VIA interconnections [4]. Their optimization usually implies the correction of the geometric design with the aim of the minimization of such issues. Initial efforts were concentrated on single-VIA optimization and its electrical models [5] with the presence of stitching VIAs and vertical ground interconnections between layers [6]. Many papers in the literature [7,8] and industrial white papers [9] have treated the design of differential VIAs with the aim of performance improvements. Vasa, Mallikarjun et al. [10] showed how the correct choice of an impedance that optimizes the matching between a line and a VIA improves the signal propagation in the PCB. A valid approach to this problem is based on the impedance at the input port when a differential signal is applied on it: $Z_{DD_{11}}$ [11]. In Reference [12], Pan et al. demonstrated that a differential VIA structure calls for the optimization of all associated parameters at the same time. In Reference [13], Asif et al. showed that even though all of the geometrical parameters affect the performance of differential VIAs, their influences are different. In particular, they demonstrated that

the insertion loss $S_{DD21}$ and return loss $S_{DD11}$ of a differential VIA for a differential input signal have different sensitivities. In detail, for these S-parameters, the antipad and pitch variations are in contrast with radius size variations.

These parameters are a natural extension of single-VIA analysis. For differential structures, it is necessary to consider the inter-modal conversion [14]. This is described by the mixed scattering terms, $S_{DC21}$ and $S_{DC12}$, which account for the two-way conversion between differential and common-mode signals, thus giving a measure of the Electromagnetic Interference (EMI), emissivity (differential-to-common-mode conversion), and susceptivity (common-to-differential-mode conversion) [14]. Since the mixed-mode and single-ended scattering parameters are both linear representations, it is possible to use them as a reference during the number and position evaluation of stitching VIAs. The insertion of stitching VIAs can be used to improve the performance in terms of modal conversion and insertion loss once the structure of the differential couple has been optimized [12,15,16]. The cited papers evidence the need for asymmetrical VIA organization, as any asymmetry increases the modal-conversion contributions [16,17]. In particular, Chen et al. [15] showed how symmetrical structures should be used in association with the optimization of ground VIA positions by demonstrating that correct positioning can provide better results when compared to random placement of more ground VIAs.

The VIA stub effect is a common limiting issue for both single and differential VIAs. Such an effect occurs any time the VIA length is greater than the distance between the planes to be connected, introducing a behavior similar to that of a transmission-line stub. This means that the signal components at any possible stub resonance frequency are strongly attenuated [7]. Shin et al. [17] showed that, given the layer stack-up, no possible differential VIA variation affects such attenuation, but the stack-up itself strongly dominates it through the ground VIA. A resonance shift to higher frequencies is obtained when all of the ground layers in the stack-up are used. Typically, the back-drilling technique is adopted to mitigate this problem. This technique consists of the removal of the unused portion of a VIA with destructive drilling [18]. Alternative solutions are terminators [19] or specific absorbing materials [20].

Many CAD tools are available for electromagnetic (EM) PCB analysis, such as Ansys HFSS and Keysight PathWave Advanced Design System (ADS). Many works have exploited the capabilities of ADS [13,21].

In this paper, we propose a procedure that manages the structural terms of the differential VIA to optimize their performance starting from an initial reference structure. The object of the process is the enhancement of the VIA's electrical performance and the minimization of the area of the PCB's surface covered by it. The proposed strategy starts from a parametric analysis of the VIA's characteristics using closed-loop iterations to refine the geometrical parameters and considering the differential VIA as a four-port element. At each step of the analysis, some suitable Figures of Merit (FoMs) are evaluated based on frequency- and time-domain electrical magnitudes, namely:

- Mixed-mode S-parameters: $S_{DD_{21}}$ , $S_{DC_{21}}$, $S_{DD_{11}}$, $S_{CD_{21}}$;
- Port impedance: $Z_{DD_{11}}$;
- Impedance evaluated though reflectometric time-domain analysis, $TDR$.

Figure 1 depicts the relationships between terminals that define the ports and the associated input–output signals used in the definition of the FoMs. In particular, for the mixed-mode configuration and impedance evaluation, two terminals define a single port, which is in opposition to the single-mode configuration. This is due to the different natures of the considered signals, as indicated in the legend in Figure 1. The scattering matrices linked to the mixed-mode and single-mode configurations show how the S-parameters' FoMs are extracted from them. For the impedance term, the configurations, stimulus type, and data representation are displayed. Such FoMs are mathematically connected. In addition, they can be extracted from a single simulation on the ADS platform, as described in the forthcoming sections.

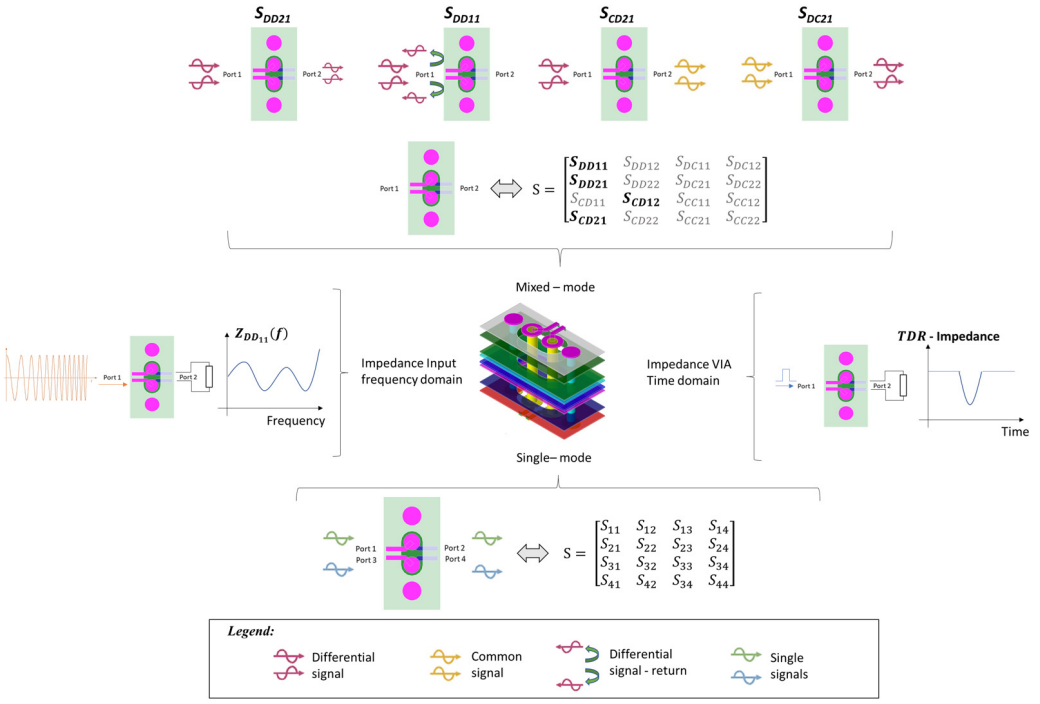


**Figure 1.** Figures of Merit and configuration of VIA ports.

The paper is organized as follows: In Section 2, we explore the possible VIA structures for high-speed PCBs, along with design constraints. In Section 3, we describe the proposed procedure, which is relative to a reference stack-up. In Section 4, we illustrate the CAD simulation setup and the simulation results and validate the approach. Section 5 reports some comments on the obtained results. Finally, conclusions close this work.

## 2. VIA Structures for High-Speed PCBs: Design and Constraints

In high-speed PCBs, there are three main structures that are usually employed to interconnect different layers, and they are graphically sketched in Figure 2.

- Stacked VIA structure, which is realized by placing a micro-VIA connecting layers $i$ and $i+1$ and another micro-VIA connecting layers $i+1$ and $i+2$.
- Through-hole VIA, which is realized through the insertion of an interconnection passing all of the layers and connecting the uppermost layer with the bottom-most one, as well as by equivalently inserting a stub into the section.

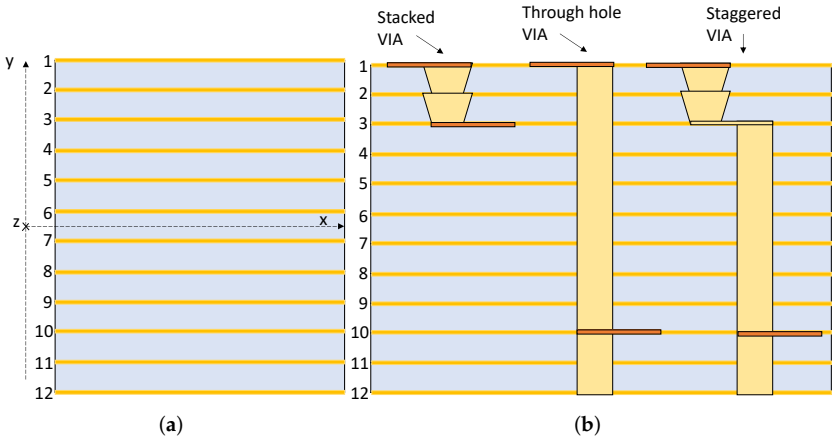


**Figure 2.** Reference structures: (a) An $N = 12$ layer stack-up; (b) different VIA structures.

- Staggered VIA structure, which is realized by placing a micro-VIA connecting layers $i$ and $i+1$, another micro-VIA connecting layers $i+1$ and $i+2$, and a buried VIA connecting $i+2$ and $j$. The structure also comprises a stub in the section connecting layers $k$–$j$;

We will denote with $\Delta_{\{i,j\}}$ the hole diameter of the VIA connecting layer $i$ to layer $j$, $i, j = 1, \cdots, N$, $(i \neq j)$, of an $N$-layer stack-up.
We summarize here the main design rules exposed in the IPC document and other design references [22,23] that constrain the design of VIA structures.

We define the pad size, $Pad$, as the circular copper area around the VIA, and we determine the Outer-layer Annular Ring (OAR) as the radius of the circular ring. The first design rule to follow is:

$$Pad \geq \Delta_{\{i,j\}} + 2 \cdot \mathrm{OAR} \tag{1}$$

We assume this parameter to be equal for each of the layers associated with the same VIA without distinguishing between the inner and outer layers. Once the pad size has been defined, denoting by $s$ the distance between the VIA centers (pitch), the second design rule to follow is [21]:

$$s \geq Pad + PtP \tag{2}$$

where $PtP$ denotes the distance between the pair of differential VIA pads and the $Pad$ of the single VIA.

The last design rule concerns the antipad for the single VIA, which is defined as the clearance area between the pad and the metal plane. Its diameter $\Lambda$ should be such that

$$\Lambda > Pad. \tag{3}$$

For the differential VIA, the antipad area $A_{Tot}$ has an overall extension of

$$A_{Tot} > s \cdot Pad + \pi \cdot \frac{Pad^2}{4} \tag{4}$$

Therefore, the size of an antipad is bound to the pad size, and the choice to use the same pad dimensions in the layers involved by the VIA defines a common minimum antipad value. The same convention is also adopted in the absence of a pad.

As previously shown in Figure 2b, some configurations have micro-VIA elements. Since they have a conical shape, we will consider the hole diameter $\Delta_{\{i,j\}}$ for the target land, that is, the lower diameter [22]. The upper diameter at the capture land is considered to be 50 µm wider according to [22]. In this case, the pad size is calculated as a function of the hole at the target land.

The staggered VIAs are not aligned with the initial drilling section, thus requiring a specific interconnection between the micro-VIA pad and the blind VIA pad. In this scenario, we indicate with $p$ and with $c$, respectively, the two pads' diameters. According to IPC-2226 [22], the length of a single interconnection element is equal to:

$$L_{CV} = \frac{p+c}{2} = \frac{\Delta_{\{2,3\}} + \Delta_{\{3,12\}} + 4 \cdot OAR}{2} \tag{5}$$

The misalignment of the drilling sections in the staggered structure leads to the reformulation of (2) for the specific case. Furthermore, taking into account the slant of the pads' connection section (Figure 3d), $\alpha$:

$$s = PtP + \Delta_{\{1,2\}} + 2 \cdot OAR + 2 \cdot L_{CV} \cdot sin(\alpha) \tag{6}$$

In our reference model, we consider $\alpha = 15°$. The internal metallization thickness of VIA holes depends on the considered type. In particular, for cylindrical VIAs, a 15 µm metal film thickness is adopted. The remaining internal volume of the VIA is filled with a dielectric material whose permittivity is 3.8 $[F/m]$. In this case, an offset term of 30 µm is

added to (1) (i.e., twice the single-film thickness). Instead, micro-VIAs are completely metal-filled, so they do not require an offset term. Thereafter, they are connected to transmission lines with a $Z_0/2$ characteristic impedance, thus giving a differential $Z_0$ impedance, which is the target value for interconnection impedance matching [10].

Once the signal VIA structures have been described, we may define the constraints on stitching VIA structures. In this optimization procedure, we consider sets of two or four stitching VIAs. The stitching VIAs can be described with the relations previously introduced for differential VIAs. In particular, denoting with $Pad_S$, $\Delta_S$, and $OAR_S$ the parameters previously described but with reference to the stitching VIAs, the above-described equations for dimensioning still hold.

The stitching VIA arrangement is described by the parameters $D_{CtC}$ and $D_{Stitch}$ (Figure 3e), where $D_{CtC}$ represents the distance along the $z$-axis between the stitching VIAs and the closest differential VIA, and $D_{Stitch}$ represents the distance between the symmetry axis of the differential pair and a stitching VIA. These values should satisfy the following constraints:

$$D_{CtC} > \frac{\Lambda}{2} + OAR \tag{7}$$

$$D_{Stitch} > OAR_S + \frac{\Delta_S}{2} \tag{8}$$

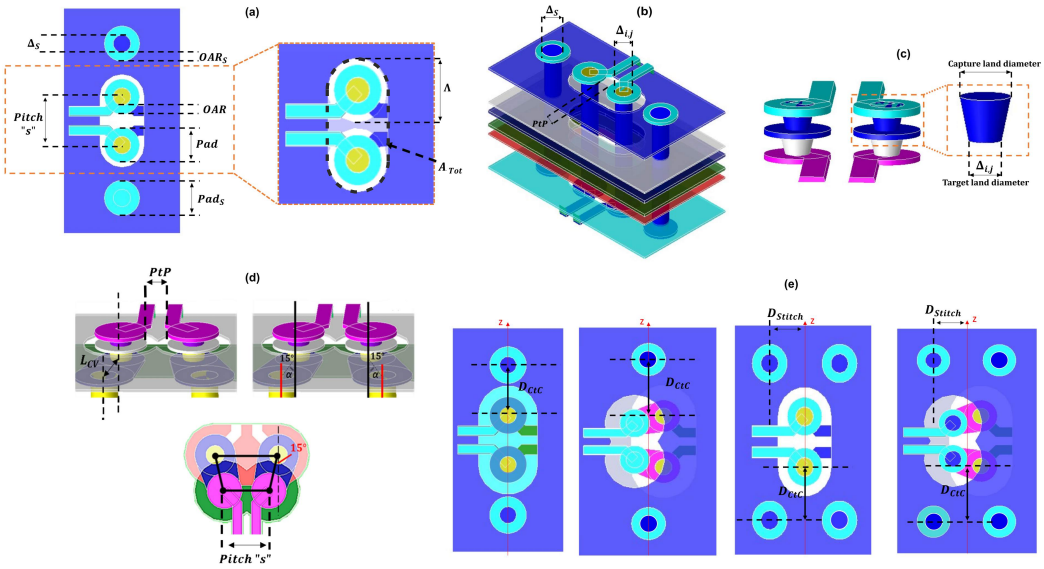


**Figure 3.** Sketch of the geometrical parameters (**a**) Planar view and parameters for the differential pair and the stitching couple (**b**) Nomenclature for the diameters and PtP distances (**c**) Diameters for the capture land and target land of the VIA (**d**) Front view and parameters taking into account the slant (**e**) Stitching VIA parameters.

## 3. Description of the Proposed Approach

In this section, we describe the optimization technique that we are introducing. We start from a reference stack-up of 12 layers defined according to the current constraints on the EM Compatibility (EMC) for the signal and power layers. Thereafter, we introduce some FoMs to address in order to consider the optimization to be reached.

As will be described, we consider as a preliminary test case the stacked VIA, since it is the most commonly employed structure in high-speed PCBs. However, the same procedure can also be applied with slight variations to the through-hole and staggered VIA structures.

### *3.1. Reference Stack-Up*

The reference stack-up for this work is composed of $N = 12$ layers based on PTFE with a relative dielectric permittivity of $\varepsilon_r = 3.45$. The total stack-up thickness is equal to 1.68 mm, with different metal layers whose thickness is determined by their position in the stack. In particular, for the external and core layers, a thickness of 35 $\mu m$ is adopted, and this is reduced to 25 µm for the other layers. Only half of the available layers are used for the device interconnection and the signal planes, while the others represent ground planes. They are symmetrically organized to satisfy the EMC constraints, as indicated in Table 1.

**Table 1.** Specifications of each layer function in our $N = 12$ reference stack-up.

| Plane | Type |
|---|---|
| Layer 1/12 | Signal Plane |
| Layer 2/11 | Power Plane |
| Layer 3/10 | Signal Plane |
| Layer 4/9 | Signal Plane |
| Layer 5/8 | Power Plane |
| Layer 6/7 | Power Plane |

In detail, the substrate thickness between the external layers and power plane is equal to 75 µm; it is 90 µm between power planes and 200 µm between the remaining layers. The proposed stack-up offers a symmetry with respect to the $xz$-plane (Figure 2a). In fact, given the same geometry, a VIA interconnecting the first layer with the generic $k^{\text{th}}$ layer has the same SI characteristics as a VIA interconnecting the $12^{\text{th}}$ layer with the $(12-k)^{\text{th}}$ layer. For the VIA optimization process in this work, we consider the stacked VIA structure $L_{1,3}$, which is realized by placing a micro-VIA with $\Delta_{\{1,2\}}$ connecting layers 1 and 2 and another micro-VIA with $\Delta_{\{2,3\}}$ connecting layers 2 and 3, which is also the most common structure for multi-layer interconnections. In fact, even though they are state-of-the-art VIA interconnection structures, the staggered VIA and through-hole VIA structures are still under study because the presence of cross-sectional stub introduces some artifacts in the VIA behavior that are not suitable for high-speed applications.

In Table 2, we summarize the starting configuration parameters, whose mutual relationships are illustrated in Figure 3, while respecting the rules exposed in the IPC document and the main design [22,23]. In particular, for the two-stitching-VIA case, the term $D_{Stitch}$ will be considered to be 0 µm. In that case, there is a single VIA stitching for each element of the differential VIA pair. This assumption excludes the possibility of having single stitching VIAs that are misaligned along the $z$-axis, thus avoiding a non-optimal positioning.

**Table 2.** Reference geometry of the stacked VIA structure $L_{1,3}$.

| **Signal VIA Geometry** | |
|---|---|
| Parameter | Size [µm] |
| $\Delta_{\{1,3\}}$ | 150 |
| $\Delta_{\{2,3\}}$ | 150 |
| $OAR$ | 150 |
| $PtP$ | 150 |
| $\Lambda$ | 400 |
| **Stitching VIA Geometry** | |
| Parameter | Size [µm] |
| $\Delta_S$ | 300 |
| $OAR_S$ | 150 |
| $D_{CtC}$ | 600 |
| $D_{Stitch}$ | 0 |

### *3.2. The Optimization Procedure*

The optimization procedure we propose is based on a two-step process. First, VIA's geometric structure is varied according to a systematic strategy that we will describe later. Then, the FoMs are evaluated in the bandwidth of interest. In particular, we strive for (in order of importance):

(I) the maximum $dB(S_{DD21})$ value ;
(II) the minimum $dB(S_{DD11})$, $dB(S_{CD21})$, and $dB(S_{DC21})$ values;
(III) the minimum mean deviation of $Z_{DD11}$;
(IV) the $TDRresponse$ with the minimum deviation from the reference value of $Z_0$.

The comparisons on the S-parameter FoMs are made by evaluating the average $\mu$ and the standard deviation, $\sigma$, in the frequency bandwidth of interest, which is defined as the range from DC up to the frequency $f_{-3dB}$ for which $dB(S_{DD21}) = -3\ dB$.

Obviously, the maximum $dB(S_{DD21})$ value is equal to 0 dB, where the VIA structure is an example of passive elements. The same procedure is adopted to compare the differential impedance $Z_{DD_{11}}$.

For what concerns the TDR response, the deviation is evaluated as the difference between the minimum/maximum values obtained for a specific parameter setting and the nominal $Z_0$ reference impedance value, that is,

$$\beta = Z_0 - z_{TDR_{min}} \tag{9}$$

$$\gamma = z_{TDR_{max}} - Z_0 \tag{10}$$

where $\beta$ and $\gamma$ are the maximum and minimum deviations obtained from the TDR analysis, respectively.

The parameters associated with the structure are varied according to the manufacturing rules for large-scale production, which are reported in Table 3, with the aim of minimizing the analysis range and reducing production costs [23–25].

**Table 3.** Parameter boundary values for the stacked VIA $L_{1,3}$. Values are expressed in μm.

| Parameter | Min Value | Max Value | Min Step | Mid Step | Max Step |
|---|---|---|---|---|---|
| $\Delta_{\{1,2\}}$ | 100 | 150 | 25 | - | 50 |
| $\Delta_{\{2,3\}}$ | 100 | 150 | 25 | - | 50 |
| $OAR$ | 100 | 150 | 25 | - | 50 |
| $PtP$ | 100 | 150 | 25 | - | 50 |
| $\Lambda$ | 500 | 800 | 25 | 50 | 100 |

A systematic strategy is adopted to manage the variation of the initial VIA geometry based on two steps:

1. Differential Pair Optimization (DPO): In this step, we iteratively seek the optimal geometry of the differential VIA by using as a reference two stitching VIAs whose dimensions and positions are fixed. The results of this phase provide the optimal signal VIA.
2. Stitching VIA Optimization (SVO): Using the optimal signal VIA as a starting point, we optimize the stitching VIAs in terms of position, geometry, and number while keeping the input pair geometry fixed. The number of stitches varies between two and four. The results obtained by means of the FoM comparisons identify the best differential–stitching VIA structure, which is referred to as the optimal differential–stitching VIA.

A single-parameter analysis is not the best choice in terms of the time duration of the search for the optimal combinations. Thus, geometric variation is performed on a multi-parameter base, as in other optimization frameworks [12,13].

In particular, during the DPO, two cascaded multi-parameter analyses are performed—$OAR^k@\Delta^k_{\{i,j\}}$ and $\Lambda^k@PtP^k$, with $k$ indexing the iteration $k = 0, \cdots, n$.

These analyses are separately performed given their different sensitivities and dependence on (2) and (3) [13].

Figure 4 summarizes the procedural steps of the proposed optimization method.

The first geometric variation is $OAR^0@\Delta^0_{\{i,j\}}$, and it is implemented over the intervals defined by:

$$\begin{cases} A^0 = [min(OAR), max(OAR)] \\ B^0_{\{i,j\}} = [min(\Delta_{\{i,j\}}), max(\Delta_{\{i,j\}})]. \end{cases} \tag{11}$$

where $A^0$ denotes the interval in which the OAR can vary and $B^0_{i,j}$ designates the range of variation of the drilling diameter with respect to the specified $\{i,j\}$ hole. After the definition of the intervals, the corresponding variation steps are computed using the values listed in Table 3: $step_{OAR}$ and $step_{\Delta_{\{i,j\}}}$. Given the interval and the analysis step for each parameter, it is possible to evaluate the number of cases to consider with $a^0$ and $b^0_{i,j}$:

$$\begin{cases} a^0 = \dfrac{[max(OAR) - min(OAR)]}{step_OAR} + 1 \\ b^0_{i,j} = \dfrac{[max(\Delta_{\{i,j\}}) - min(\Delta_{i,j})]}{step_{\Delta_{\{i,j\}}}} + 1 \end{cases} \tag{12}$$

The overall number of geometrical combinations $\zeta^0$ used for $OAR@\Delta_{\{i,j\}}$ in the analysis is:

$$\zeta^0 = a^0 \cdot b^0_{i,j} \tag{13}$$

where $b_{i,j}$ is equal to the product of all $d_{i,j}$ terms present in the specific configuration in staggered or stacked structures.

The outputs of this step are the configurations that achieve the best performance according to the considered FoMs. This geometry is denoted as $[OAR - \Delta_{\{i,j\}}]^0$ and becomes the starting point for the multi-parameter optimization of $\Lambda^k@PtP^k$.

Analogously with the previous case, we define two intervals:

$$\begin{cases} C^0 = [min(\Lambda), max(\Lambda)] \\ D^0 = [min(PtP), max(PtP)]. \end{cases} \tag{14}$$

Two variation steps are associated with these intervals: $step_\Lambda$ and $step_{PtP}$, respectively. The number of steps to consider is now represented by

$$\begin{cases} c^0 = \dfrac{[max(\Lambda) - min(\Lambda)]}{step_\Lambda} + 1 \\ d^0 = \dfrac{[max(PtP) - min(PtP)]}{step_{PtP}} + 1 \end{cases} \tag{15}$$

and by associating with these the maximum as the initial value, the number of cases $\eta$ is given by:

$$\eta = c^0 \cdot d^0 \tag{16}$$

The case study obtained through these analyses supplies the optimum combination, $[\Lambda - PtP]^0$, associated with the considered $[OAR@\Delta_{\{i,j\}}]^0$ values.

The process is, thus, repeated, as illustrated in Figure 4. The iterations end when the FoM improvements reach a given minimum threshold value. The step size is reduced during these iterations, but the number of cases is kept constant, and the size of the interval is reduced according to Table 3.

In particular, each new $A^k$,$B^k_{\{i,j\}}$,$C^k$,$D^k$ interval considered is centered around the optimum parameter obtained in the previous iterations, with numbers of cases $\{a^0, b^0, c^0, d^0\}$ that are equal to the initial ones.

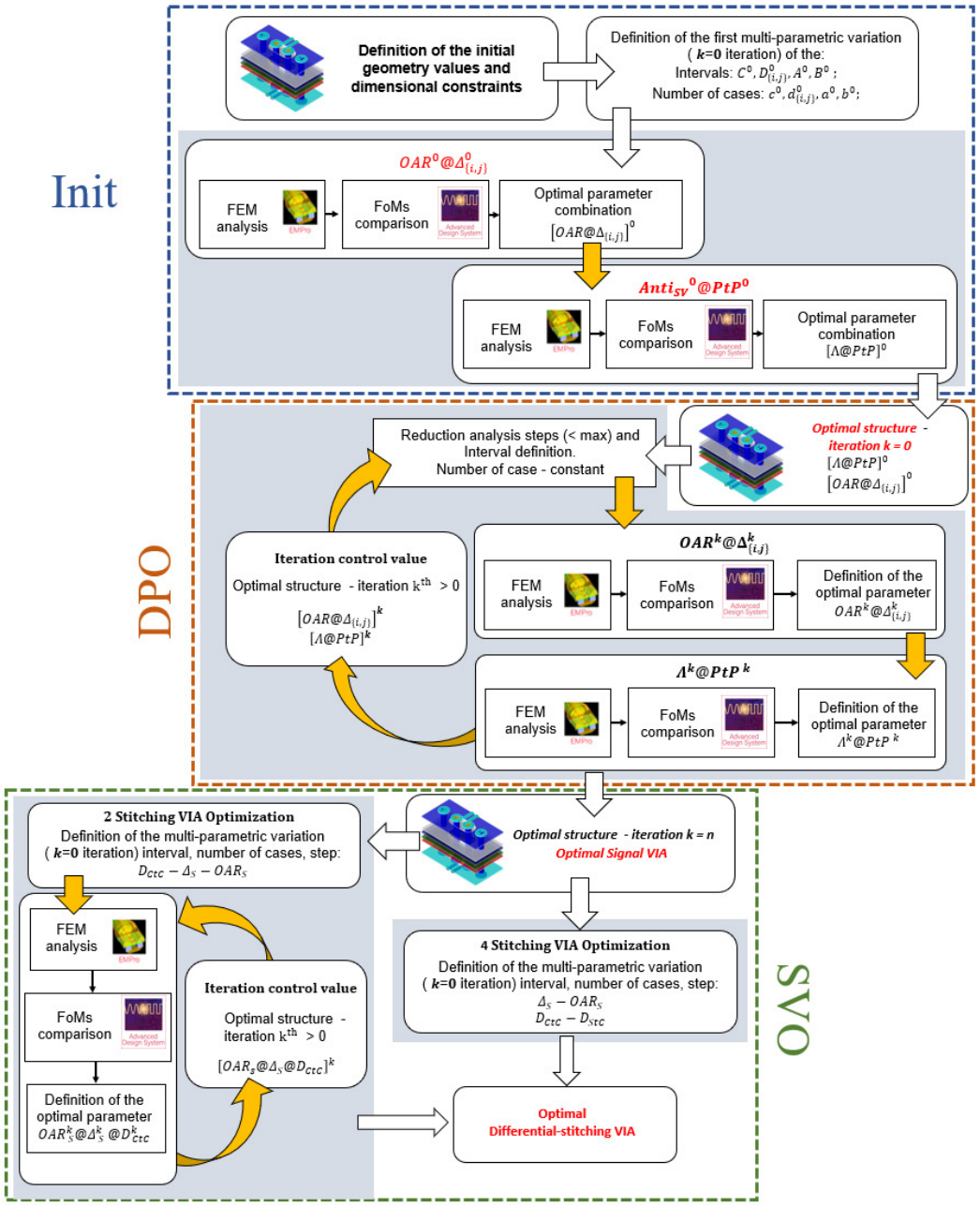


**Figure 4.** The three-step analysis and optimization framework presented in this paper.

When the optimum parameter value at the $k^{\text{th}}$ iteration reaches the maximum or the minimum corresponding value in Table 3, it results in

$$a^k = \left\lfloor \frac{a^0}{2} \right\rfloor; \quad b^k = \left\lfloor \frac{b^0}{2} \right\rfloor; \quad c^k = \left\lfloor \frac{c^0}{2} \right\rfloor; \quad d^k = \left\lfloor \frac{d^0}{2} \right\rfloor. \tag{17}$$

with $\lfloor \cdot \rfloor$ being the integer-part function obtained through truncation. Hence, the analysis interval is halved.

When $k = n$, the optimal signal VIA is obtained. Thus, the SVO subphase begins. For the two-stitching-VIA case, $D_{CtC}$, $\Delta_S$, and $OAR_S$ are varied in the single multi-parameter analysis $OAR_S@\Delta_S@D_{CtC}$ by using the values in Table 4. In parallel, for the four-stitching-VIA case, analogously to what was previously described, the analysis is iteratively performed using two-parameter couples of $D_{CtC}@D_{Stitch}$ and $\Delta_S@OAR_S$, respectively. The result of these optimization processes is the optimal differential–stitching VIA.

**Table 4.** Parameter limit—stitching VIA geometry. Values are expressed in μm.

| **Two Stitching VIAs** | | | | |
|---|---|---|---|---|
| Parameter | Min value | Max value | Min step | Max step |
| $\Delta_S$ | 100 | 150 | 25 | 50 |
| $OAR_S$ | 100 | 150 | 25 | 50 |
| $D_{CtC}$ | 600 | 750 | - | 150 |
| **Four Stitching VIAs** | | | | |
| Parameter | Min value | Max value | Min step | Max step |
| $\Delta_S$ | 100 | 150 | 25 | 50 |
| $OAR_S$ | 100 | 150 | 25 | 50 |
| $D_{CtC}$ | 600 | 750 | - | 150 |
| $D_{Stitch}$ | 100 | 300 | - | 100 |

## 4. Method Validation and Results

In this section, the optimization procedure that was previously analytically described is validated through simulations. In particular, simulation parameters of the Finite-Element Method (FEM) are first described in detail according to the standard specifications. Then, we discuss the obtained results, presenting the benefits of applying such an optimization on differential pairs of stacked VIAs.

### *4.1. Simulation setup parameters*

The proposed procedure was tested using the Keyight® PathWave™ Advanced Design System (ADS) and Electromagnetic Professional (EMPro™) [26]. The stack setup made with the Substrate editor was used for the initial guess of the VIA design considering all of the previously discussed constraints. This initial geometry was analyzed with EMPro (FEM analysis) with the following setup:

- A simulation frequency range of 0 to 70 GHz;
- A 1% error magnitude threshold for the S-parameters on consecutive mesh refinement steps;
- A mesh refinement frequency of 70 GHz;
- A matrix solver with two-order discretization;
- An adaptive simulation (a minimum of 20 points on the simulation frequency range),

where the bandwidth span was defined according to the main digital protocol standards using an 85 Ω interconnection impedance. This value was chosen as a reference, since most high-speed PCB designs adopt this value due to the many advantages it gives over the 100 Ω differential impedance case, such as easier VIA design, smaller dielectric height in the stack-up, an impedance value closer to the impedance profiles of most packages, and so on [27]. The results of the FEM parametric analysis define the VIA models used in the measuring scheme in Figure 5, which provides the FoM values starting from the single-mode S-parameters, as in a real measurement system. The first terms evaluated are the mixed-mode terms $S_{DD_{21}}$, $S_{DD_{11}}$, $S_{DC_{21}}$, and $S_{CD_{21}}$:

$$S_{DD11} = 0.5 \cdot [S_{(1,1)} - S_{(1,3)} - S_{(3,1)} + S_{(3,3)}] \quad (18)$$

$$S_{DD21} = 0.5 \cdot [S_{(2,1)} - S_{(2,3)} - S_{(4,1)} + S_{(4,3)}] \quad (19)$$

$$S_{CD21} = 0.5 \cdot [S_{(2,1)} - S_{(2,3)} + S_{(4,1)} - S_{(4,3)}] \quad (20)$$

$$S_{DC21} = 0.5 \cdot [S_{(2,1)} + S_{(2,3)} - S_{(4,1)} - S_{(4,3)}] \quad (21)$$

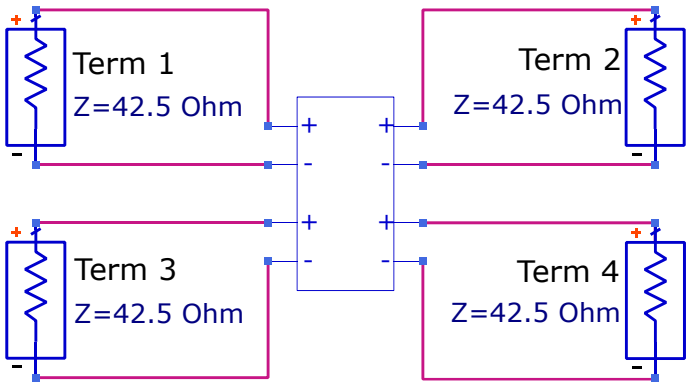


**Figure 5.** Reference schematic circuit for the simulation of the S-parameters. The black-box element in the center contains the EM model of the stack-up for the current simulation.

The impedance term $Z_{DD11}$ is extracted from the $S_{DD11}$ parameter through the use of the equation:

$$Z_{DD11} = 85 \cdot \frac{(1 + S_{DD11})}{(1 - S_{DD11})} \tag{22}$$

Thanks to the setup in Figure 5, the TDR response could also be obtained by using the $S_{DD11}$ parameter and considering the frequency–time relation between the two parameters [14]. The parameter changes were directly managed using an ADS-specific function `tdr_sp_imped()` [28]. The simulation took a 2 ns time window into account, centered the response at 1 ns, and used a Hamming window on 351 samples. The described procedure evidences the links between the FoMs and, thus, the need to consider them simultaneously. From the adaptive FEM analysis, by using a fifth-order interpolating polynomial, we obtained 351 samples with spacings of 200 MHz. These were used to perform the comparisons between the curves.

### *4.2. Simulation Results*

The following section reports the results obtained by applying our procedure with the setup and previously described definitions. The graphs and data obtained in the considered cases are reported for each of the FoMs. A two-legend notation is used to describe the FoMs. The first, which is placed in a box, summarizes the considered cases. The second is placed below each graph, and it shows the data response for every curve.

In this preliminary work, we evaluated the stacked VIA structure $L_{1,3}$. Figure 6 shows the FoMs associated with the initial geometry (Table 2).

Figures 7 and 8 report the results of the simulations associated with the iteration $k = 0$ according to the model in Figure 4. In particular, Figure 7 reports the FoMs obtained starting from the initial $L_{1,3}$ VIA geometry in relation to the $OAR@\Delta_{\{i,j\}}$ parameter variation case. For the specified geometry and case, the values are indicated as $OAR^0@\Delta^0_{\{1,2\}} - \Delta^0_{\{2,3\}}$. The optimal combination obtained, $[OAR@\Delta_{\{1,2\}} - \Delta_{\{2,3\}}]^0$, is the starting point for the optimization of the parameter couple $\Lambda@PtP$. The assumed values are indicated as $\Lambda^0@PtP^0$ (Figure 8). The optimal combination is $[\Lambda@PtP]^0$.

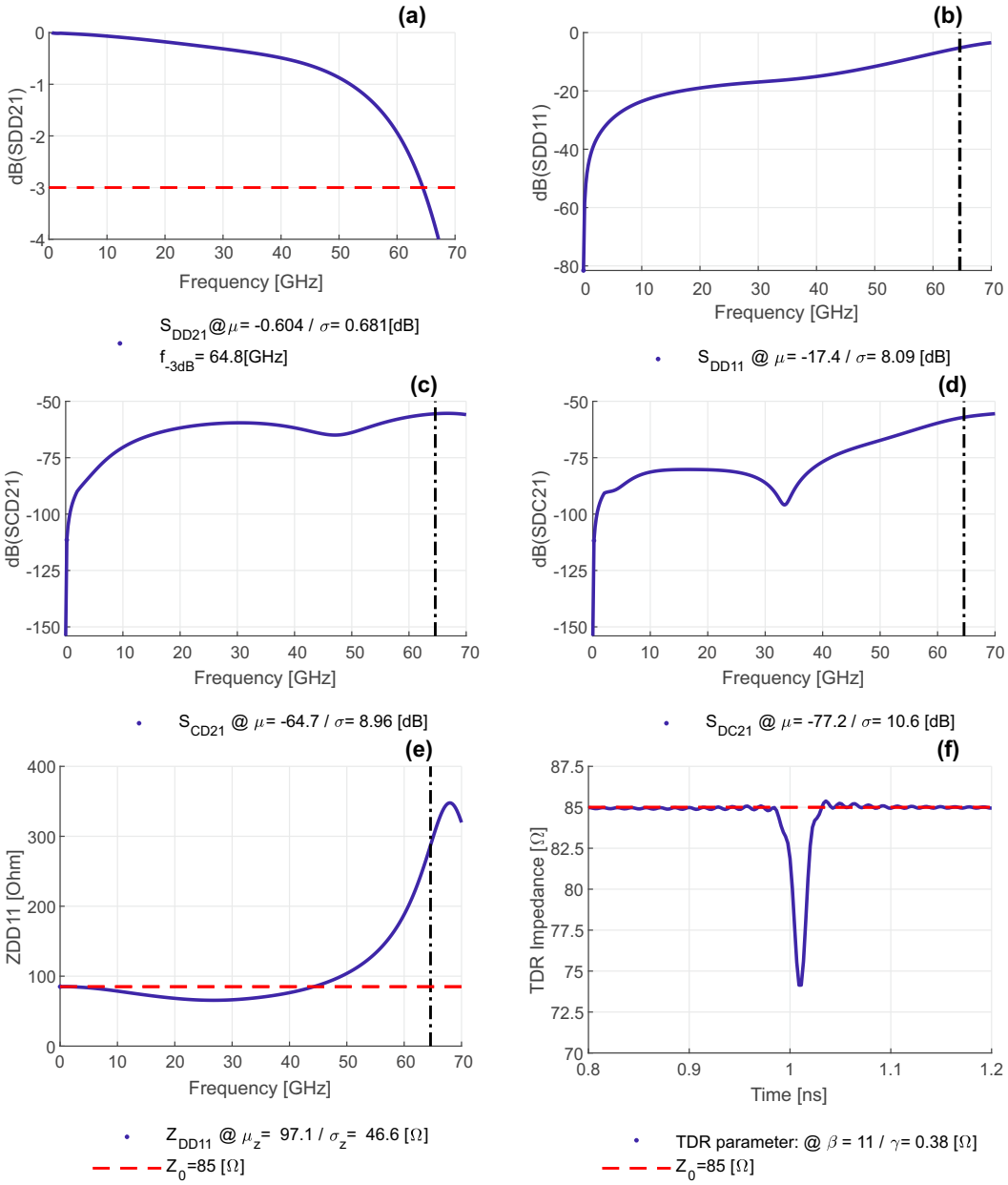


**Figure 6.** FoMs of the reference VIA structure—$L_{1,3}$: (a) $S_{DD21}$; (b) $S_{DD11}$; (c) $S_{DC21}$; (d) $S_{CD21}$; (e) $Z_{DD11}$; (f) TDR response.

According to the previous discussion, the parameters used are:

$$\begin{cases} A^0 \in [100, 150]\ \mu\text{m} \\ B^0_{\{1,2\}} \in [100, 150]\ \mu\text{m} \\ B^0_{\{2,3\}} \in [100, 150]\ \mu\text{m} \\ C^0 \in [400, 800]\ \mu\text{m} \\ D^0 \in [100, 150]\ \mu\text{m} \end{cases} \tag{23}$$

with $a^0 = 2$, $b^0_{\{1,2\}} = 2 = b^0_{\{2,3\}}$, $c^0 = 5$, and $d^0 = 2$, as well as a number of cases:

$$\begin{cases} case_{OAR@\Delta_{\{i,j\}}} = a^0 \cdot b^0_{\{1,2\}} \cdot b^0_{\{2,3\}} = 8 \\ case_{Anti_{SV}@PtP} = c^0 \cdot d^0 = 10 \end{cases} \tag{24}$$

The results of these structural changes are recalled here:

$$\begin{cases} OAR = 100\ \mu\text{m} \\ \Delta_{\{1,2\}} = 150\ \mu\text{m} \\ \Delta_{\{2,3\}} = 100\ \mu\text{m} \\ PtP = 100\ \mu\text{m} \\ \Lambda = 800\ \mu\text{m} \end{cases} \tag{25}$$

These values were obtained by using the maximum variation step, as indicated in Table 3. Figure 9 compares the FoMs of the initial and the new geometry. The step of variation is thus reduced to 25 $\mu m$ for the parameters $OAR$, $\Delta_{\{1,2\}}$, $\Delta_{\{2,3\}}$, and $PtP$ and 50$\mu m$ for $\Lambda$. Respecting the rules defined above and considering the maximum value of the antipad as the central value, the analysis interval is equal to $[700, 900]$ µm, from which the values of 850 µm and 900 µm must be excluded, as they are higher than the maximum limit, resulting in $C^1 = [700, 850]$ µm. The result is, therefore, $c^1 = roof(\frac{c^0}{2})$ =3. For the parameter $PtP$, the analysis interval is $D^1 = [100, 125]$ µm, thus resulting in a number of cases equal to 6. Following this methodological approach, as regards the pair of parameters $OAR@\Delta_{\{i,j\}}$ for $k = 1$, $A^1 = [125, 150]$, $B^1_{\{1,2\}} = [100, 125]$, $B^1_{\{2,3\}} = [100, 125]$, $a^0 = a^1 = 2$, $b^0_{\{1,2\}} = b^1_{\{1,2\}} = 2$, and $b^0_{\{2,3\}} = b^1_{\{2,3\}} = 2$, with a number of cases equal to 8.

Now that the intervals and the steps of variation of the parameters have been defined, the results of the relative FEM simulations are evaluated in Figure 10 for the terms $OAR@\Delta_{\{i,j\}}$ at $k = 1$. The optimal combination does not change. The same result is obtained in the case of $[PtP@\Lambda]^1$.

Given this optimal combination of the parameters $OAR@\Delta_{\{i,j\}}$ and $PtP@\Lambda$, it is possible to assert that we have determined the combination linked to the optimal signal VIA. It is, therefore, possible to pass the optimization of the stitching VIAs. The first topology considered is based on the two-VIA stitching with modifications to the position and geometry. The results are shown in Figure 11. In particular, since the curves exhibit very similar behaviors, we summarize them in single points representing the average values.

Therefore, the parameters considered are $OAR_S@\Delta_S@D_{CtC}$; they are evaluated in a single FOM analysis considering the minimum step of variation for each parameter. The optimal combination is the one associated with $OAR_S@\Delta_S@D_{CtC}$ and with the minimal distance. The optimization performed on the four-VIA stitching was performed in two steps that were linked to the variation of the parameters $D_{CtC}@D_{Stitch}$ and $\Delta_S@OAR_S$. However, the results showed no appreciable differences with respect to the two-stitching VIA case.

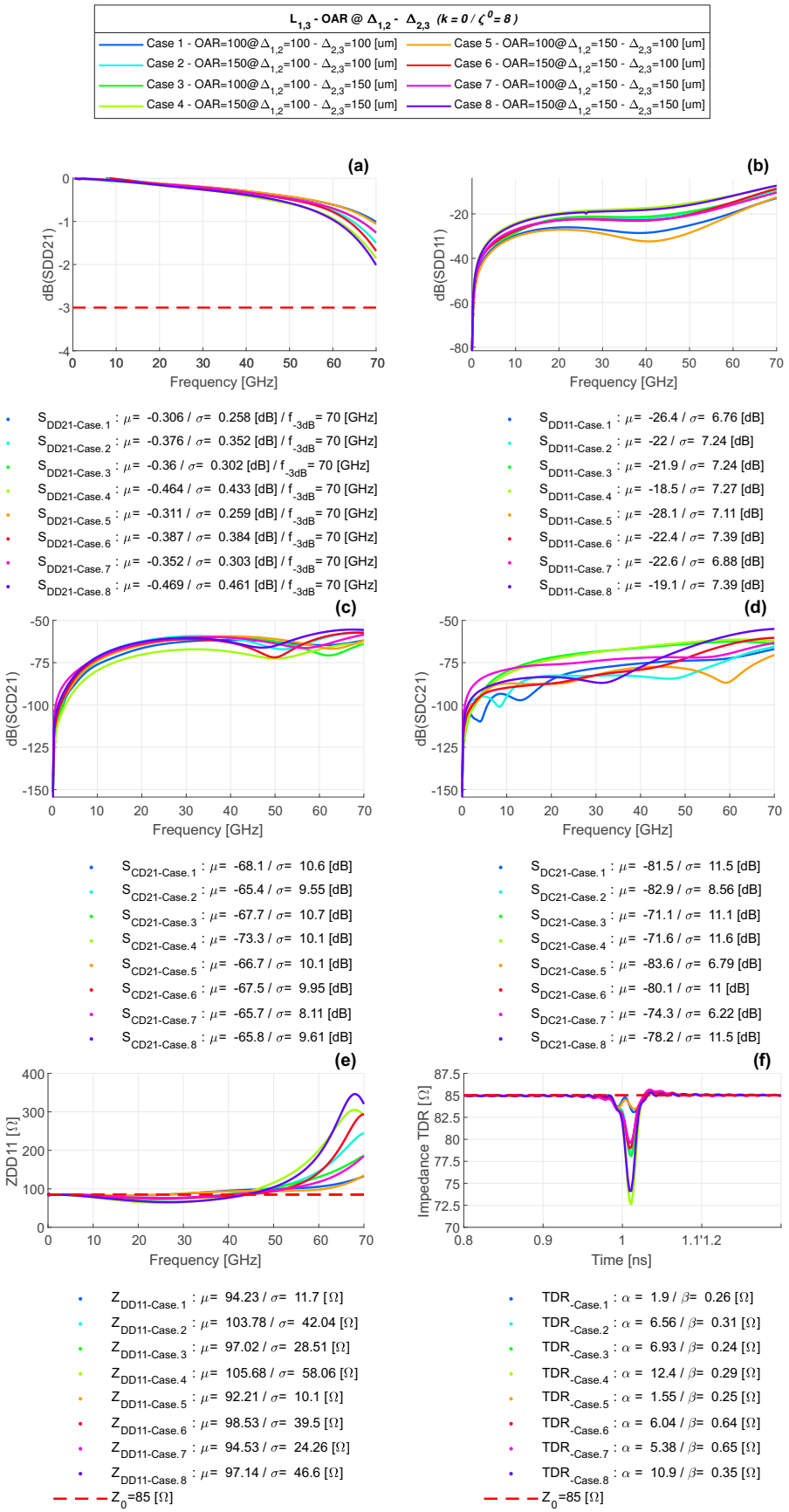


**Figure 7.** FoMs of $OAR@\Delta_{\{1,2\}}@\Delta_{\{2,3\}}$—$L_{1,3}$ (DPO phase—$k = 0$): (a) $S_{DD21}$; (b) $S_{DD11}$; (c) $S_{DC21}$; (d) $S_{CD21}$; (e) $Z_{DD11}$; (f) TDR response.

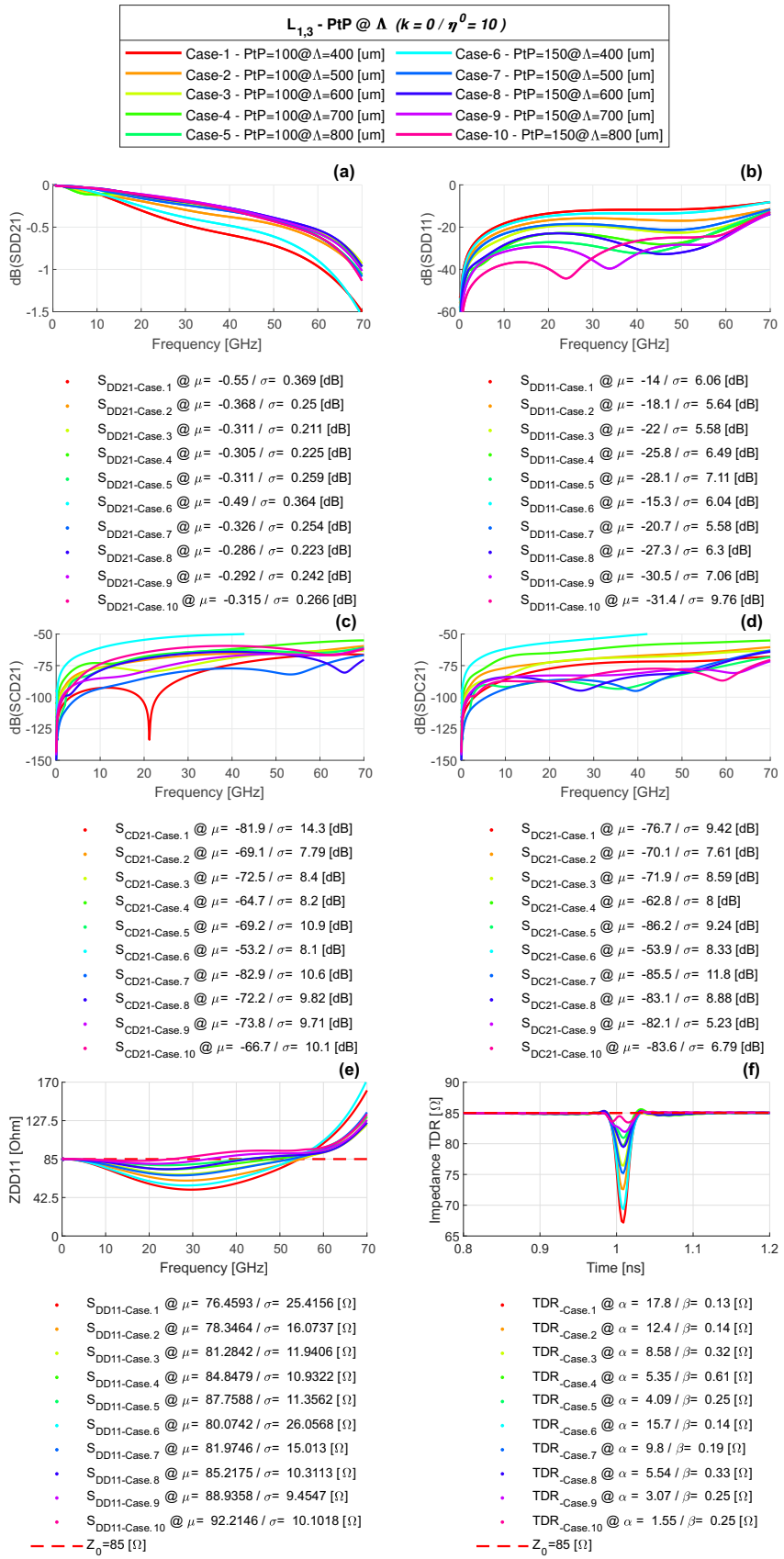


**Figure 8.** FoMs of *PtP*@Λ - $L_{1,3}$—(DPO phase—$k = 0$): (a) $S_{DD21}$; (b) $S_{DD11}$; (c) $S_{DC21}$; (d) $S_{CD21}$; (e) $Z_{DD11}$; (f) TDR response.

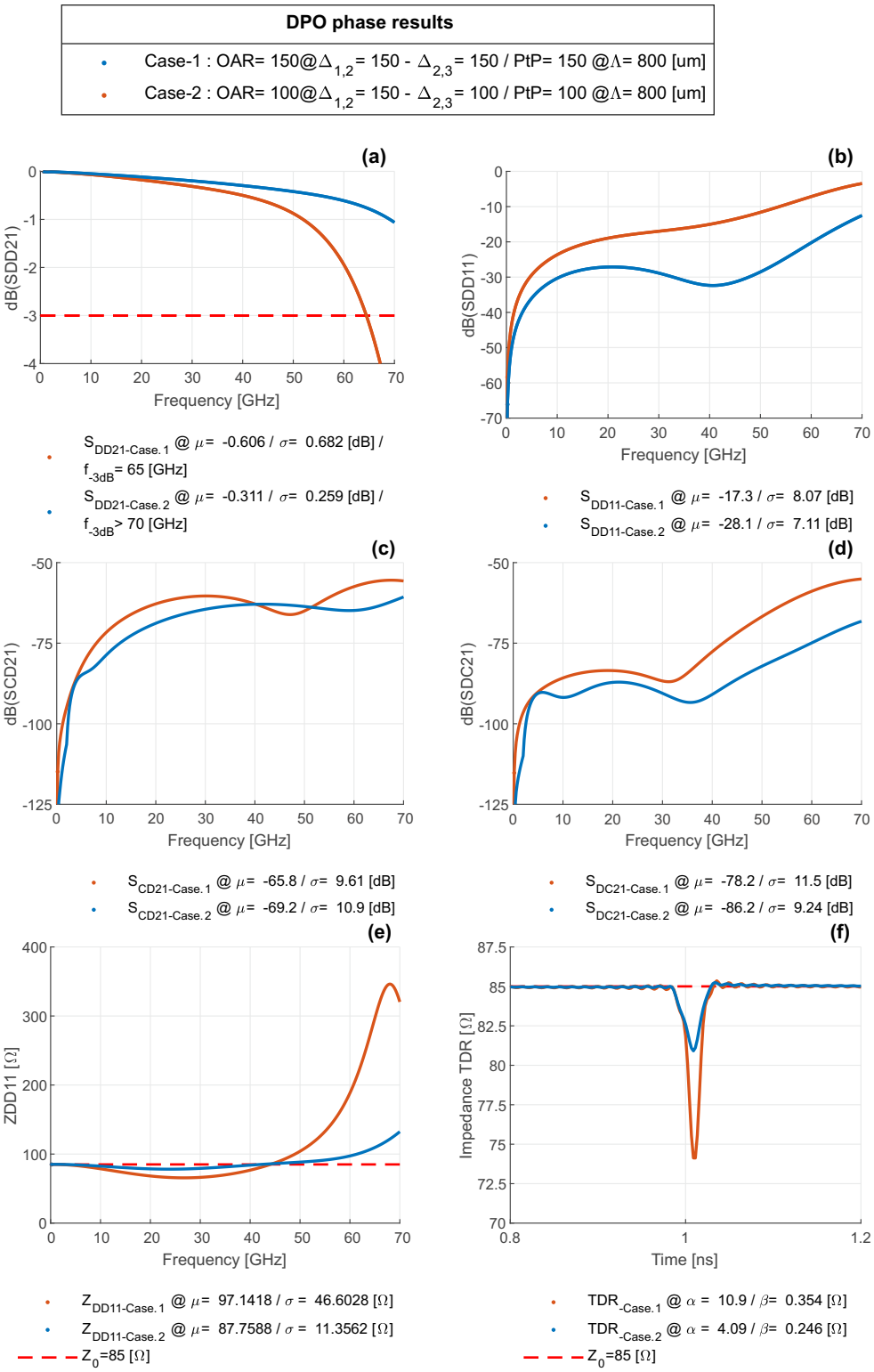


**Figure 9.** DPO results ($k$ = 0)—$L_{1,3}$: (a) $S_{DD21}$; (b) $S_{DD11}$; (c) $S_{DC21}$; (d) $S_{CD21}$; (e) $Z_{DD11}$; (f) TDR response.

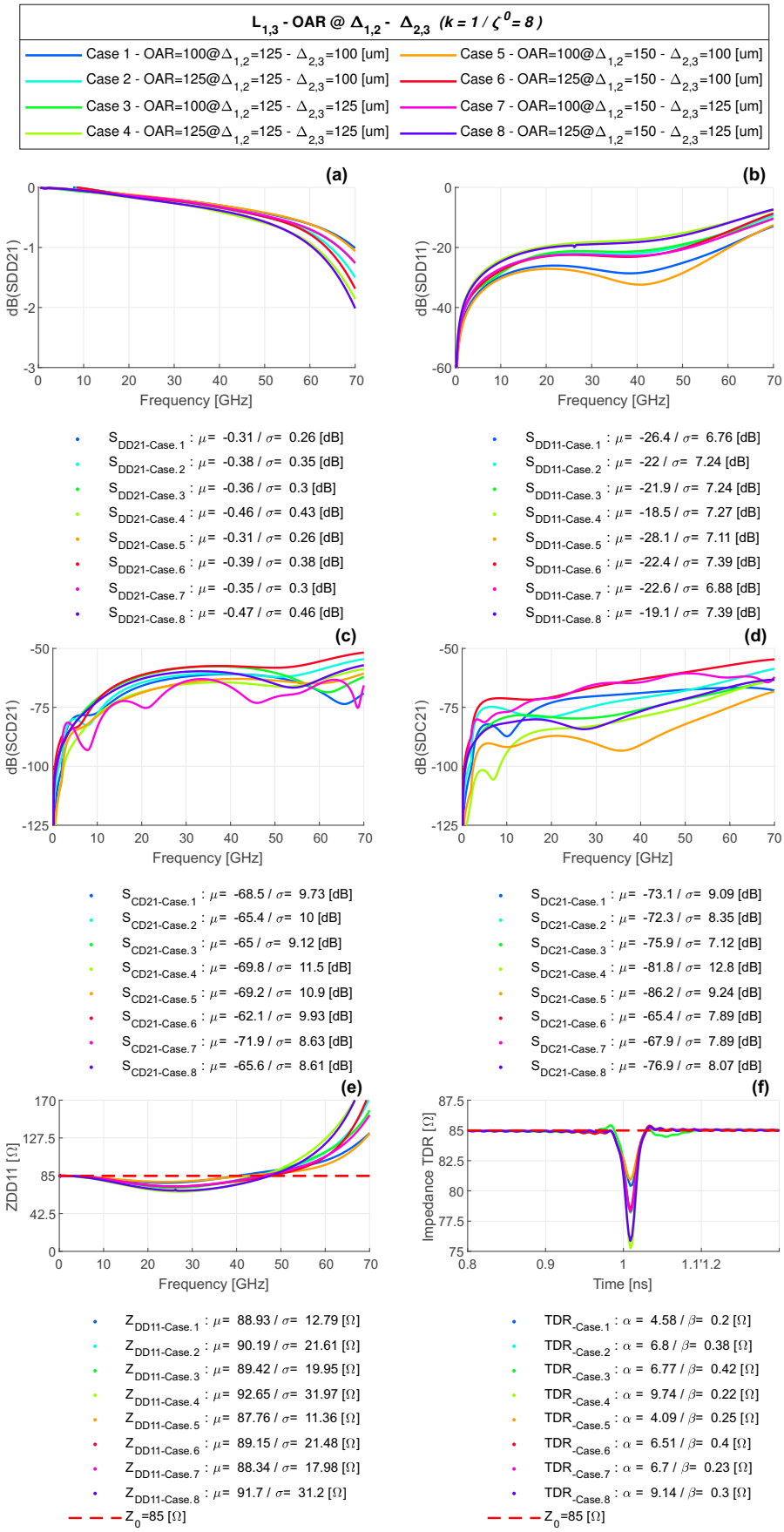


**Figure 10.** FoMs of $OAR@\Delta_{\{1,2\}}@\Delta_{\{2,3\}}$—$L_{1,3}$ (DPO phase—$k = 1$): (a) $S_{DD21}$; (b) $S_{DD11}$; (c) $S_{DC21}$; (d) $S_{CD21}$; (e) $Z_{DD11}$; (f) TDR response.

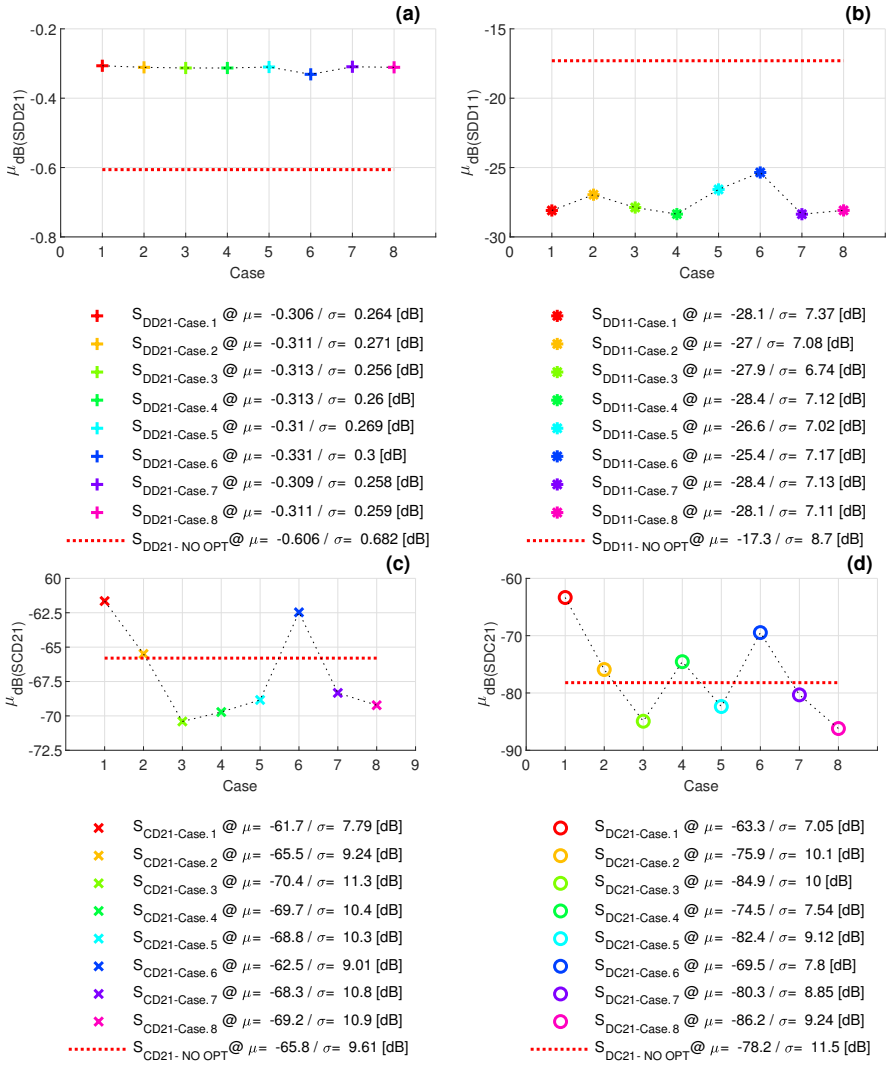


**Figure 11.** FoMs of $D_{CtC}$@$D_{Stitch}$ and $\Delta_S$@$OAR_S$—$L_{1,3}$ (SVO-phase results compared to the DPO output structure): (a) $S_{DD21}$; (b) $S_{DD11}$; (c) $S_{DC21}$; (d) $S_{CD21}$.

## 5. Analysis of the Results and Design Hints

The analysis of the above-reported results allows the definition of a design strategy based on a set of design rules that ease the VIA design procedure:

- A single parameter cannot be optimized without influencing other specifications; the optimization process must be global.
- The antipad design must be optimized in each layer, and may even be a computationally heavy process.
- The antipad dimension is relevant for impedance matching, but its enlargement achieves the goal while concurrently increasing the cross-talk and the modal conversion, thus suggesting a maximum value for it of 800 µm.
- *Pad* is strongly bound to the VIA diameter. An increase in this value must be avoided, as it directly induces a bandwidth reduction.
- An $OAR_s$ of 100 µm minimizes the area coverage and simplifies the analysis. Further enlargements do not give any appreciable benefits.
- Increasing the distance between the VIAs widens the occupied area without any particular benefits.
- The hole diameter must be evaluated as a function of the type of VIA considered. In addition, by widening it above the 200–250 µm range, increased cross-talk has been

reported. Moreover, it determines an increment in the occupation of the PCB's area. However, reducing it below the proposed range results in a bandwidth reduction.
- A stitching VIA diameter $\Delta_s$ below 200 μm increases the cost without any benefits.
- The number of stitching VIAs must be even because an odd value results in a loss of symmetry without any advantages.
- An increment in the number of stitching VIAs does not represent a mandatory solution, as a single optimized pair may offer the same performance with reduced cost and area.

## 6. Conclusions

The procedure described here has provided an optimal definition of a VIA while respecting the rules and constraints of PCB production and minimizing the area of the PCB covered by the VIA itself. The results obtained by the procedure are sometimes better than the target values assumed for the optimization process. Moreover, the procedure described here allows one to greatly reduce the number of iterative simulations that must be performed in order to reach the optimal target values.

Further work is currently in progress in order to extend the procedure to much more complex structures, such as an array where interactions between VIAs cannot be neglected.

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