Article

An Analog Baseband Circuit for Wireless Local Area Networks Transceiver in 55 nm CMOS Technology

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Abstract: The design of the analog baseband circuit is based on 55 nm CMOS technology and is integrated in an IEEE 802.11ax concurrent dual band four antenna transceiver. A low-pass filter (LPF) of the receiver was multiplexed with an LPF-transmitter such that the last three stages of the fifth order LPF-receiver were used by the LPF-transmitter, and the first programmable gain amplifier (PGA) of the receiver was partially multiplexed with the PGA-transmitter such that the PGA-receiver and the PGA-transmitter shared the same operational amplifier and input resistance, thereby reducing the power consumption, noise, linearity, and area of intermediate frequency (IF) of the transmitter designed separately. The typical bandwidth of the IF-receiver is 10/20/40 MHz; that of the IF-transmitter is 12/24/50 MHz. The gain range of the IF-receiver and the IF-transmitter is 0.1–65.5 dB and −10.1 to 3.98 dB, respectively. Under the voltage of 1.5 V, the current of the IF-receiver is 3.86 mA. As for the IF-transmitter, the current is 1.78 mA when supply voltage is 1.5 V. The input referred noise (IRN) of the IF-receiver at 10 MHz bandwidth (BW) and 62 dB gain is 14.52 nV/√Hz, while the IRN of the IF-transmitter at 10 MHz BW and −6 dB gain is 95.16 nV/√Hz. The suppression ability of the DC offset cancellation circuit is 35.08/80.9/110.1/113 dB. The area of the analog baseband circuit is 0.17 mm².

Keywords: analog baseband circuit; IF-receiver; IF-transmitter

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1. Introduction

Wi-Fi is one of the most popular wireless technologies and provides high-speed network services at a low cost [1]. The IEEE 802.11 protocol has undergone an upgrade in the a/b/g/n/ac/ax version; its data throughput is getting higher and higher [2,3]. Transceivers are widely used in computer and mobile electronic products; protocols used vary with different applications [4].

The analog baseband circuit (ABB), which can also be called the intermediate frequency (IF) circuit, is one of the core modules of wireless local area networks (WLAN) transceivers. The analog baseband circuit can be divided into the receiving analog baseband circuit and the transmitting analog baseband circuit, that is, the IF-receiver and the IF-transmitter. The IF-receiver realizes the signal amplification and the channel selection, while the IF-transmitter realizes signal attenuation and out-of-band filtering.

The system on-chip is a complete system that integrates a single chip in addition to the antenna. The antenna on-chip integrates the antenna into the circuit board to obtain the electromagnetic interface-free space necessary for antenna communication [5]. The system on-chip demands a traditional 50 Ω interface and a lossy RF interconnection, while the antenna on-chip can solve this problem [6]. Nevertheless, the antenna on-chip possesses limitations on the narrowband and low radiation efficiency [5]. Meanwhile, the antenna on-chip is integrated in millimeter wave and terahertz circuits, which requires using expensive

high frequency ground signal ground (GSG) probes, bulk waveguides and horn antennas, and which is not conducive to large-scale production [7]. In contrast, the analog baseband circuit was integrated into the system on-chip in this research.

In 2017, the system-on-a-chip (SoC) block diagram proposed by T. M. Chen, et al. demonstrated that the RX mode and the TX mode adopted different filters, where a 960 MS/s 10 bit TX digital to analog converter (DAC) was followed by a pair of simple first order passive RC filters [8]. In 2020, different filters were used in a 4×4 dual band Wi-Fi 802.11ax transceiver proposed by E. Lu, et al. A second order baseband filter was used in the TX mode with an I/Q transimpedance amplifier, followed by a programmable second order Butterworth opamp-RC filter/programmable gain amplifier (PGA) used in the RX mode [9]. In 2021, a radio frequency (RF) transmitter architecture proposed by M. Mansour, et al. showed that the low-pass filter (LPF) and the variable gain amplifier (VGA) of the receiver were used in the RX mode, while the LPF-transmitter and the PGA-transmitter were used in the TX mode [10]. The area of the chip determines its price; a smaller area is the key specification for chip competitiveness. In view of this characteristic, an analog baseband circuit based on the LPF and PGA of transceiver multiplexing was proposed, that is, the IF-receiver and the IF-transmitter LPF and PGA were multiplexed, respectively. The IF-receiver and the IF-transmitter share the same IF circuit, which saves area overhead of the IF-transmitter. LPF can be order reconfigurable, bandwidth reconfigurable and gain reconfigurable.

When designing LPF, it is necessary to consider the filter prototype (Butterworth or Chebyshev) and selection of Gm-C or active RC. For the first problem, filter suppression response and group delay response must be considered. Due to the strict adjacent channel suppression of IEEE 802.11 and the rectangular spectrum of orthogonal frequency division multiplexing (OFDM), the Chebyshev filter is more suitable and uses lower filter orders than the Butterworth filter. Moreover, the OFDM signal is not sensitive to fluctuation of group delay [11]. As for the second question, the amplifier of the Gm-C filter was open-loop, so it was easy to obtain high-frequency characteristics and low power consumption; however, linearity was very poor. The amplifier of the active RC filter was closed-loop, so linearity was excellent; however, R and C are easily affected by process, voltage, and temperature (PVT), which further changes frequency characteristics. IEEE 802.11b/g/n/ac/ax applications require high linearity of the receiver. The OFDM of the active RC filter with 1024 quadrature amplitude modulation (QAM) requires high linearity and a wide dynamic range, so it is more suitable for WLAN [12–14].

In this paper, the analog baseband circuit design was based on 55 nm CMOS technology. The IF-receiver designed included LPF with 5th order active RC Chebyshev, PGA with closed-loop structure resistor feedback, and a DC offset cancellation (DCOC) circuit with continuous time feedback. Moreover, the IF-transmitter designed included multiplexed 3rd order active RC Chebyshev LPF and multiplexed closed-loop resistor feedback PGA. The area of the IF-transmitter was reduced by multiplexing. Through the analysis of Cadence software and Spectre simulator, simulation results verified the performance of the design.

2. Architecture

In the receiver of zero-IF or low-IF architecture, the input signal of the analog-to-digital converter (ADC) was 0 dBm during normal operation; the dynamic range from the antenna to baseband was 0–104 dB. Most of the gain was provided by the IF-receiving circuit. In this design, the low noise amplifier (LNA) and the receiving mixer (RXMIX) provided a gain dynamic range of 0–24 dB and 0–14 dB, respectively, while the IF-receiver provided a gain dynamic range of 0–66 dB. Signal level output from the transmitter digital-to-analog converter (DAC) was relatively large, about 0 dBm. The gain dynamic provided by the IF-transmitter ranged from –10 to 4 dB. Therefore, the gain budget of each module was different from the design above on account of different applications [15].

The system architecture of the zero-IF transceiver based on IF multiplexing is shown in Figure 1. The low pass filter of the receiver was multiplexed with the LPF-transmitter

to the last three stages of the fifth order LPF-receiver used by the LPF-transmitter. The architecture of ABB is shown by dotted line. Both I and Q channels of the receiver included LNA, RXMIX, LPF, PGA and DCOC; both I and Q channels of the transmitter included LPF, PGA, transmitting mixer (TXMIX) and power amplifier (PA). On the one hand, multiplexed LPF achieved a gain from -10 to 18 dB, in which the gain of the LPF-receiver was 0 – 18 dB with a 6 dB/step gain coarse adjustment control, while the gain of the LPF-transmitter was -10 to 4 dB with 2 dB/step gain coarse adjustment control. On the other hand, the gain of the first PGA multiplexed was 0 – 24 dB; the gain coarse adjustment control of the PGA-receiver was 2 dB/step; the gain of the PGA-transmitter was 0 to 2 dB with 0.5 dB/step gain fine adjustment control. The second PGA was only used in the RX mode and realized gain was 0 – 24 dB with 2 dB/step gain coarse adjustment control.

Figure 1. System architecture of zero-IF transceiver based on IF multiplexing.

The LPF-receiver needs to have strong frequency selectivity and a steep transition band. The main function of the LPF-transmitter is to filter out noise at a sampling frequency of DAC that is at least twice the useful signal frequency. Therefore, the transition band of the LPF-transmitter can be relatively slow, and the order of the LPF-transmitter is obviously less than that of the LPF-receiver. In this design, the order of the filter is configurable. The LPF-receiver is the 5th order, and the LPF-transmitter is the 3rd order [16]. Typical bandwidth (BW) of the LPF-receiver and the LPF-transmitter are $10/20/40$ MHz and $12/24/50$ MHz, respectively. As a result, PGA needs to have a wider bandwidth than 50 MHz [15].

3. LPF Implementation

3.1. Operational Amplifier

LPF, PGA, and DCOC in the analog baseband circuit adopt a two-stage fully differential operational amplifier. The operational amplifier adopts a fully differential architecture, which can effectively suppress the common mode signal of the circuit, reduce the even harmonic distortion of the circuit, and even have larger output swing when the chip voltage decreases continuously. However, a disadvantage of this architecture is that the common mode output level cannot be determined accurately because of the small gain of the external feedback common mode loop. In our design, the common mode feedback circuit was adopted, which could keep output of DC fixed and which did not change with PVT; the model is shown in Figure 2. The stability of the operational amplifier was taken into the structure of a fully differential operational amplifier. More problems appeared when the stability of the operational amplifier operated as three-stage and above, which needs to be solved by a more complex circuit. Therefore, the two-stage operational amplifier was adopted in this paper. The reasons why the PMOS different pair transistor was adopted by first level input are as follows: Firstly, PMOS has low noise compared with NMOS under a certain current. Although the area of PMOS is large, its matching is better than NMOS (NMOS is suitable for high speed). Moreover, with a decrease in power supply voltage, the common mode range became smaller, and the PMOS transistor needed to be used. Finally, the operational amplifier emphasizes symmetry. The common source stage with source

negative feedback was adopted in order to reduce power consumption of the second stage. In order to ensure stability of the two-stage operational amplifier, a miller compensation capacitor was added between the first stage and the second stage. Miller compensation technology was adopted to realize pole segmentation and to improve phase margin and stability of the operational amplifier. However, zero will be introduced in the right half plane to produce a -90° phase shift. The transistor was connected in a series, which could make the compensation capacitor directional in order to cut off the feedforward path and eliminate this positive zero. Open-loop DC gain and unity gain frequency of the operational amplifier were 64.76 dB and 1.74 GHz, respectively. It consumed 0.48 mA from 1.5 V supply voltage.

Figure 2. The structure of two stage Miller fully differential operational amplifier.

3.2. Programmable Capacitor Bank and Resistor Bank

Analog baseband filters (LPF-receiver and LPF-transmitter) can realize bandwidth and gain reconfiguration. Bandwidth reconfiguration can be changed only by controlling the size of the capacitor bank, which is independent of the resistor bank. The capacitance bank adopted is shown in Figure 3. Each capacitor C was composed of a capacitor bank in a dotted line. $1C$ corresponds to the capacitor value when the LPF bandwidth is 40 MHz. The number of C in the connection circuit is controlled through the transistor gate (TG) switch. For instance, $2C$ is the capacitance value when the LPF bandwidth is 20 MHz and $4C$ is the capacitance value when the LPF bandwidth is 10 MHz. The area of the layout was further saved by the multiplexing capacitor C .

Figure 3. Bandwidth reconfigurable capacitor bank.

Typical bandwidth of the LPF-receiver is 10/20/40 MHz, and that of the LPF-transmitter is 12/24/50 MHz. The function of resistance R was to avoid the peak phenomenon of LPF in passband.

Gain reconfiguration is changed by adjusting the size of the resistor bank. Resistor bank is applied to both the LPF-receiver and the LPF-transmitter [16]. R_1 to R_n are different values corresponding to different gains. In order to control the proportional relationship between resistors accurately, all resistors were composed of a standard unit resistor in series or in parallel. The unit resistor used in this design was 2 Kohms, which was selected by multiple adjustments from the perspective of area and matching.

3.3. Multiplexing LPF-Transceiver

An active high-order filter can be composed of first order and double biquad. The advantages of this filter are its simple design and its easy calibration. Output impedance of each stage is very low, which is actually 0. However, it is highly sensitive to element mismatch and is only suitable for a low-quality factor filter. The high-order filter composed by the method of trapezoidal filter synthesis was less sensitive to component mismatch and is more suitable for high-precision filters. Therefore, in our design, the RLC trapezoidal filter synthesis method was adopted to realize the full differential structure of the 3rd/5th order configurable filter [16].

Appropriate gain and bandwidth were configured according to signal size and bandwidth requirements. The LPF-receiver was multiplexed with the LPF-transmitter, which possesses great flexibility and which can save the area of the LPF-transmitter. That is, the LPF-receiver is 5th order, and the LPF-transmitter is 3rd order, multiplexing the last three operational amplifiers of the LPF-receiver and corresponding capacitor bank.

4. Programmable Gain Amplifier

The programmable gain amplifier can be divided into closed-loop and open-loop according to the structure of the core amplifier circuit. The former adopts the feedback mode, which possesses high accuracy and linearity, while gain change of PGA with open-loop structure will affect the bandwidth of the circuit. Therefore, the resistor feedback mode of the closed-loop structure was applied to the PGA-receiver and the PGA-transmitter in this design. The main function of PGA is gain amplification; the bandwidth should be greater than the maximum bandwidth of the filter. In order to ensure flatness of the amplitude frequency response of PGA in the passband, the feedback capacitor bank was added. The final single ended structure model is shown in Figure 4.

Figure 4. Structure of single ended closed-loop PGA.

If the operational amplifier provided was ideal, we used $1/Z_2 = 1/R_2 + 1/(1/sC_2) = (R_2C_2s + 1)/R_2$, and then use of the node relationship and circuit transfer function is

$$H(s) = -\frac{R_2}{R_1} \frac{1}{sC_1R_2 + 1} \quad (1)$$

while actual gain and bandwidth of operational amplifier are limited. The transfer function of the operational amplifier is

$$A(s) = \frac{A\omega_a}{s + \omega_a} \quad (2)$$

where A is the DC gain of the operational amplifier, ω_a is the -3 dB bandwidth of the amplifier, and the actual circuit transfer function is

$$H(s) = -\frac{R_2}{R_1} \frac{1}{\frac{(s+A\omega_a)(sC_1R_2+1)}{A\omega_a} + \frac{R_2}{R_1} \frac{s+\omega_a}{A\omega_a}} \quad (3)$$

Therefore, it can be derived that the corner frequency is

$$\omega_0 = \sqrt{\frac{A\omega_a R_1 + R_2 \omega_a}{R_1 R_2 C_1}} \quad (4)$$

and the quality factor is

$$Q = \sqrt{\frac{(A\omega_a R_1 + R_2 \omega_a) R_2 C_1}{(1 + \frac{R_2}{R_1} + A\omega_a R_2 C_1) \sqrt{R_1}}} \quad (5)$$

In order to ensure the smoothness in the passband and the attenuation out of band of the amplitude frequency response, conditions need to be met: $Q \leq 1$. DC gain of PGA can be obtained $H(0) = -(AR_2)/(AR_1 + R_2)$ in the condition of C_1 meeting requirements. Therefore, gain required by the PGA-receiver and the PGA-transmitter can be obtained by adjusting the resistor bank R_2 . The first PGA was partially multiplexed in the RX mode and the TX mode. The gain of the PGA-receiver was 0–24 dB with 2 dB/step, of which 0–2 dB was divided into 0.5 dB/step, that is, gain of the PGA-transmitter. The second PGA was only used in the RX mode, and the gain was 0–24 dB with 2 dB/step.

5. DC Offset Cancellation

When zero-IF architecture was applied to the transceiver, the RXMIX output before the IF-receiver showed a large DC offset, which strongly affected the circuit dynamic range. In order to keep the receiver working normally, the DCOC circuit must be added in the IF-receiver to increase the spurious-free dynamic range. Continuous feedback technology was adopted in the design of DCOC; DC offset at output of the module was fed back to the input of the module to compensate for the offset voltage. The DCOC circuit consists of three stages. The offset voltage output of RXMIX amplified by the LPF-receiver was calibrated through the first stage of DCOC; then, the offset voltage output of the first stage DCOC, amplified by the first stage PGA-receiver, was calibrated through the second stage of DCOC. Finally, the offset voltage amplified by the first two stages of the PGA-receiver was calibrated through the third stage of DCOC. The schematic diagram of the single ended DCOC circuit is shown in Figure 5.

Using the node relationship, equations can be obtained as follows:

$$\left(\frac{V_{in} - V_x}{R_1} + \frac{V_y - V_x}{R_4}\right)R_2 = V_x - V_{out} \quad (6)$$

$$\left(\frac{-V_{out} - V_t}{R_3}\right)\frac{1}{sC_1} = V_t - V_y \quad (7)$$

$$(0 - V_x)A_{1(s)} = V_{out} \quad (8)$$

$$(0 - V_t)A_{2(s)} = V_y \quad (9)$$

Figure 5. Structure of DC offset cancellation circuit.

The same kind of operational amplifier is used in our system and transfer function of the circuit as below:

$$H(s) = -\frac{R_2}{R_1} \frac{1}{1 + \frac{1}{A_1(s)} + \frac{R_2}{A_1(s)R_1} + \frac{R_2}{A_1(s)R_4} + \frac{R_2}{R_4} \frac{1}{sR_3C_1(1 + \frac{1}{A_2(s)}) + \frac{1}{A_2(s)}}} \quad (10)$$

Near zero frequency, $A_1(s) \approx A_1(0) \approx \infty$, $A_2(s) \approx A_2(0) \approx \infty$, the transfer function is:

$$H(s) \approx -\frac{R_2}{R_1} \frac{1}{1 + \frac{R_2}{R_4} \frac{1}{sR_3C_1 + \frac{1}{A_2(0)}}} \quad (11)$$

DC gain is:

$$H(0) \approx -\frac{R_2}{R_1} \frac{1}{\frac{R_2}{R_4} \frac{1}{\frac{1}{A_2(0)}}} \approx -\frac{R_4}{R_1} \frac{1}{A_2(0)} \quad (12)$$

The circuit could suppress the DC offset, and the DC gain attenuation was $1/A_2(0)$ times the original.

High-pass cutoff frequency was set in an elimination DC loop, that is, the transfer function is equivalent to the high-pass filter, and the cut-off frequency is:

$$\omega_0 = \left(\frac{R_2}{R_4} + \frac{1}{A_2(j\omega_0)} \right) \frac{1}{R_3C_1} \approx \frac{R_2}{R_4} \frac{1}{R_3C_1} \quad (13)$$

Under the condition that the cut-off frequency remains unchanged, C_1 and R_3 do not need to be large if R_2/R_4 is reduced, such that the area occupied by the DCOC module can be reduced. By adjusting the resistor bank R_3 , the high-pass cutoff frequency was 13.8 Hz/207.8 Hz/3.3 kHz/545 kHz.

6. RC Calibration Circuit

In order to calibrate the influence of PVT on the RC time constant of the filter, the RC calibration circuit was designed. The capacitor bank used in the circuit was the same as that used in filter; the structure is shown in Figure 3. A combination of binary code and thermometer code was adopted. When the decoder changed the input of 6-bit binary code from “100000” to “000000” or “111111”, the equivalent capacitance was changed from 50 C to 18 C or 81 C and the variation range was -64% to 62% . The advantage of this design is that there is a sufficient bandwidth adjustment margin. The structure of the RC calibration circuit is shown in Figure 6.

Figure 6. The structure of RC calibration circuit.

Switches S_1 , S_2 , and S_3 were controlled by a clock signal with a frequency of 10 MHz, which was introduced outside the chip and which was obtained by a frequency divider. In phase ϕ_1 , S_2 was on, and C and C_1 were charged by a constant current source. In phase ϕ_2 , S_1 and S_3 were turned on, C was discharged, and the charge of C_1 was transferred to C_3 through S_3 . It could be concluded that the negative terminal voltage V_C of the operational amplifier was $V_C = I * (T/2)/C$. According to the virtual short characteristics of the operational amplifier, the positive terminal voltage V_{REF} of the operational amplifier was $V_{REF} = V_C$; V_{REF} and V_{CAL} ($V_{CAL} = I * R$) were two inputs of the comparator. When $V_{REF} = V_{CAL}$, it can be seen that $RC = T/2 = 1/(2f)$. If clock frequency f of the charge and discharge of C was constant, the product of R and C was a certain value. Therefore, as long as the clock signal controlling charge and discharge of the capacitor bank C with a certain frequency is provided, changes of R and C in LPF under various PVT conditions can be compensated by changing the value of the capacitor bank C .

If voltages at both ends of the comparator are unequal, that is, if $V_{REF} \neq V_{CAL}$, the result is sent to a counter algorithm control module to judge and adjust the control code of the capacitor bank and then fed back to the capacitor bank C. After calibration, the control code of the calibrated capacitor bank was output to a digital filter and sent to the baseband. Then, at last, the capacitor bank value of the analog low-pass filter was controlled by the baseband.

Within the frequency accuracy range required, deviation caused by change in the RC time constant with voltage and temperature after calibration could be ignored. Therefore, the RC calibration circuit completed a calibration when the receiver was powered on and obtained the capacitance control code. After calibration, the RC calibration circuit was turned off to reduce power consumption.

7. Simulation Results

The design of the analog baseband circuit was implemented in a 55 nm process. The layout of the analog baseband circuit is shown in Figure 7. The order from left to right is first level DCOC, LPF-receiver, first level PGA, second level PGA, second level DCOC and third level DCOC. The purpose of this design was to compact the layout as much as possible according to a schematic diagram. The total area of ABB was $661\text{ }\mu\text{m} \times 263\text{ }\mu\text{m}$, which is about 0.17 mm^2 . Among them, the LPF-receiver and the LPF-transmitter were multiplexed, and the first PGA-receiver and PGA-transmitter were partially multiplexed. In addition, the area of the LPF-receiver and the area of the LPF-transmitter was $302\text{ }\mu\text{m} \times 263\text{ }\mu\text{m}$ (about 0.08 mm^2) and $181\text{ }\mu\text{m} \times 263\text{ }\mu\text{m}$ (0.048 mm^2), respectively. After multiplexing the LPF-transmitter, the area was reduced by about 37.5% [16]. The total area of the PGA-receiver and the PGA-transmitter was 0.013 mm^2 without multiplexing. After partially multiplexing the PGA-transmitter (i.e., multiplexing the operational amplifier of the PGA-transmitter), area was reduced by about 18%.

Figure 7. Layout of analog baseband circuit.

The results of the frequency response of simulation are shown in Figure 8. The bandwidth of a typical IF-receiver is 10/20/40 MHz and that of a typical IF-transmitter is 12/24/50 MHz. LPFs in RX mode and TX mode in the analog baseband circuit were multiplexed; the gain characteristics of the respective LPFs are shown in [16]. The gain of the LPF-receiver was 0.1–17.96 dB with 6 dB/step, while the gain of the LPF-transmitter was –10.12 to 1.97 dB with 2 dB/step. After the first stage, PGA of the IF-receiver and the PGA-transmitter were partially multiplexed; the gain characteristics of the PGA1-receiver and PGA-transmitter are shown in Figure 9. The gain of the PGA1-receiver was 0.2–23.83 dB with 2 dB/step. The gain of the PGA-transmitter was –0.02 to 1.98 dB, the step of which was about 0.5 dB.

Figure 8. Simulated frequency response: (a) IF–receiver (b) IF–transmitter.

Figure 9. Simulated gain characteristics: (a) PGA1–receiver (b) PGA–transmitter.

Gain characteristics of the second stage PGA of the IF-receiver are shown in Figure 10. The gain of the PGA2-receiver was 0.1–24.1 dB with 2 dB/step. The total adjustable gain of the IF-receiver and the IF-transmitter in the simulated analog baseband circuit was 0.1–65.5 dB and –10.1 to 3.98 dB, respectively. The ability of DCOC to suppress low-frequency signals and local amplification is shown in Figure 11. When the bandwidth

of the IF-receiver was 10 MHz and the gain was 62 dB, by adjusting the value of the resistor bank R_3 , the suppression ability of the DCOC circuit on low-frequency signals can be 35.08 dB, 80.9 dB, 110.1 dB, and 113 dB, respectively. DC offset from RXMIX was eliminated effectively by the suppression ability. The frequency response under different temperature corners and voltage values is shown in Figure 12. The voltage of core circuits of the IF-receiver and IF-transmitter was provided by 1.5 V voltage generated by LDO. AC simulation resulted in eighteen groups of data with a voltage value (1.45/1.5/1.55 V) generated by LDO and temperature ($-25/0/55/85/105/125$ °C). It can be seen that there was little change in the above temperature and voltage.

Figure 10. Simulated gain characteristics of PGA2-receiver.

Figure 11. Simulated ability of DCOC to suppress low-frequency signals and local amplification.

Figure 12. Frequency characteristic for different values of temperature and voltage: (a) IF-receiver (b) IF-transmitter.

The simulated output voltage sinusoidal signal in the time domain is depicted in Figure 13. Input sinusoidal signals of the IF-receiver and IF-transmitter were -62 dBm and 0 dBm with the same frequency of 6 MHz; gain was 62 dB and -6 dB, respectively. It can be seen that setup time of both was less than 200 ns to ensure stable gain required after gain switching. Monte Carlo simulation results are illustrated in Figure 14. The output V_{os} of the IF-receiver and IF-transmitter were $(-498.2$ nV, 521 nV) and $(-15.79$ μ V, 15.73 μ V), respectively.

Figure 13. Simulated time domain response: (a) IF–receiver (b) IF–transmitter.

Figure 14. Simulated Monte-Carlo: (a) IF–receiver (b) IF–transmitter.

The key specifications of the IF-receiver and IF-transmitter are shown in Tables 1 and 2, respectively.

Table 1. The key specifications of IF-receiver.

Parameter	This Work
Technology	55 nm CMOS
LPF-receiver Order/Type	5th Active RC Chebyshev
Supply Voltage (V)	1.5
Current @1.5 V (mA)	3.86
Power (mW)	5.79
Typical IF-receiver BW (MHz)	10/20/40
–3 dB BW (MHz)	6.36–70.31
Pass-band gain (dB)	0.1–65.5
Pass-band ripple (dB)	<0.5
Stop band rejection @20/40/80 MHz offset for 10/20/40 MHz IF-receiver, Gain: 62 dB	24.48/22.24/12.23
DCOC suppression ability (dB)	35.08/80.9/110.1/113
IRN (nV/ $\sqrt{\text{Hz}}$) @Gain: 62 dB, BW: 10 MHz	14.52
IMD3 (dB)/Pout (dBm)@Gain: 62 dB, Vin: –62 dBm, BW: 10 MHz	–51.7/3.52
Settling Time (ns)	<200

Table 2. The key specifications of IF-transmitter.

Parameter	This Work
Technology	55 nm CMOS
LPF-transmitter Order/Type	3rd Active RC Chebyshev
Supply Voltage (V)	1.5
Current @1.5 V (mA)	1.78
Power (mW)	2.67
Typical IF-transmitter BW (MHz)	12/24/50
−3 dB BW (MHz)	7.7–124
Pass-band gain (dB)	−10.1 to 3.98
Pass-band ripple (dB)	<0.5
Stop band rejection @24/48/100 MHz offset for 12/24/50 MHz IF-transmitter, Gain: −6 dB	−26/−25.3/−23.14
IRN (nV/√Hz) @Gain: −6 dB, BW: 10 MHz	95.16
IMD3 (dB)/Pout (dBm)@Gain: −6 dB, Vin: 0 dBm, BW: 10 MHz	−50.7/−6.2
Settling Time (ns)	<200

8. Comparison Table

The results of comparing some key specifications between the IF-receiver and the state-of-the-art proposed are shown in Table 3. In terms of gain range, compared with references [17–21], a large gain range of 0.1–65.5 dB was achieved in this article. In terms of bandwidth, in addition to the passive filter type adopted in reference [17], the bandwidth of which can be up to 1400 MHz, a large bandwidth of 6.36–70.31 MHz was achieved in our design. In terms of IRN@max gain, compared with that in references [17,20], the value of IRN@max gain was 14.36 nV/√Hz which possessed a small IRN in this study. In terms of power consumption, compared with that in references [17,18,20], active 5th order LPF with a power consumption of 5.79 mW was adopted in this research, which showed low power consumption. In terms of DC suppression, DCOC was adopted in this study and in reference [17]. The high-pass cutoff frequency in Reference [17] was 7 kHz, which is lower than that in this study, with a value of 13.8 Hz/207.8 Hz/3.3 kHz/545 kHz. In terms of area, the area in this study was 0.17 mm², which is lower than that of references [17,18,20,21] with the value of 0.1/0.67/0.36/0.43 mm², respectively. The results reveal that the advantages of the IF-receiver designed herein are its large gain range (0.1–65.5 dB), wide BW (6.36–70.31 MHz), small IRN (14.36 nV/√Hz), low power consumption (5.79 mW), and small area (0.17 mm²). Moreover, DCOC multi-position controlling high pass cut-off frequency (13.8 Hz/207.8 Hz/3.3 kHz/545 kHz) was added to IF-receiver circuit. Thus, DC offset from RXMIX is effectively eliminated by suppressing DC.

Table 3. Comparison with state-of-the-art IF-receiver.

Parameter	[17]	[18]	[19]	[20]	[21]	This Work ^a
Technology Node	65 nm CMOS	65 nm CMOS	65 nm CMOS	130 nm SiGe	28 nm CMOS	55 nm CMOS
Topology	3 PGAs+5th filter	3 PGAs+2nd HPF+5th LPF	VGA+4th filter	PGA+HPF+5th LPF	HPF+PGA+4th AAF	2 PGAs+5th LPF
Filter Type	Active Butterworth	Active Butterworth ^b	passive	Active Chebyshev ^b	/	Active Chebyshev
Supply (V)	1.2	2.5	1.8	3.3	0.9	1.5
Power (mW)	6	40	/	30	1.98	5.79
BW (MHz)	0.07–10	5/10	Up to 1400	0.25–1.3	0.02–0.6	6.36–70.31
Gain Range (dB)	18.2–70.6	0–42	2.7–23.8	0–59.5	47–77 ^c	0.1–65.5
IRN (nV/ $\sqrt{\text{Hz}}$)	15.8	/	/	14.7 ^d	NF = 13 dB	14.36
@max gain DCOC	Yes	No	No	No	No	Yes
High-pass cutoff frequency (Hz)	7 K	100 K/200 K/ 1 M/5 M	/	100–1000	/	13.8/207.8/ 3.3 K/545 K
Area (mm ²)	0.1	0.67	/	0.36	0.43 ^c	0.17

^a represents simulation results; ^b represents LPF type; ^c represents receiver, including analog baseband; ^d represents simulation results of low-noise/high-linearity mode.

9. Conclusions

In this work, the design of the analog baseband circuit for the WLAN transceiver was proposed. The 5th order active RC Chebyshev LPF, PGA in closed-loop structure resistor feedback mode, and DCOC in continuous time feedback mode were adopted by the IF-receiver. Multiplexed 3rd order active RC Chebyshev LPF and partially multiplexed closed-loop resistor feedback PGA were adopted by the IF-transmitter. The area of the IF-transmitter designed separately was reduced by multiplexing. Simulation results showed that the gain range of the IF-receiver was 0.1–65.5 dB, the bandwidth range was 6.36–70.31 MHz, and the power consumption was 5.79 mW at 1.5 V voltage. Meanwhile, the gain range of the IF-transmitter was –10.1 to 3.98 dB, the bandwidth range was 7.7–124 MHz, and the power consumption was 2.67 mW at 1.5 V voltage. The total area of the analog baseband circuit was about 0.17 mm², which was integrated in an IEEE 802.11ax concurrent dual band four antenna transceiver.

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