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Realization of an Electronically Tunable Resistor-Less Floating Inductance Simulator Using VCII

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Abstract: In this paper, a new implementation of an electronically tunable resistor-less floating inductance simulator using a second-generation voltage conveyor (VCII) is presented. The proposed circuit is resistor-free (benefiting from the intrinsic resistors at the Y terminals of the employed VCII) and composed of three VCII and a single grounded capacitor. Using a control current (I_{con}), the value of impedance at the Y terminal of the VCII is varied, whereby the value of the simulated inductance is tuned. The proposed circuit is designed at a transistor level using 0.18 μm TSMC CMOS parameters and ± 0.9 V supply voltage. PSpice simulations are carried out to confirm the effectiveness of the proposed circuit. For a range of I_{con} from 0 μA to 50 μA , the value of the simulated L can be varied from $-576 \mu\text{H}$ to $-324 \mu\text{H}$ and from $+316 \mu\text{H}$ to $+576 \mu\text{H}$ for negative and positive simulators, respectively, in the frequency range of 100 kHz–3 MHz. Favorably, the value of the series resistance remains below 76 Ω . Simulation results show an error value below 4.8% and power consumption variation is from 1.64 mW to 1.92 mW. Moreover, application of the proposed circuit as a standard band-pass RLC filter is also included.

Keywords: VCII; floating inductance simulator; low voltage; low power; RLC band-pass filter

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1. Introduction

In the integrated circuit technology, the use of inductors, especially with large values, is impractical, mainly due to the large-occupied area. Accordingly, instead of bulky physical inductors, simulated inductors are used to overcome this problem. In this approach, active building blocks (ABBs) along with capacitors and resistors are used to synthesize the equivalent of inductors in a specified frequency range. More importantly, unlike physical inductors which suffer from a limited adjustment range of 15% [1], the value of simulated inductors can be easily adjusted. For those with electronic tuning capability, it is possible to adjust the value of simulated inductors electronically through a control current or voltage which is considered advantageous for providing full integration. Floating and grounded simulated inductors find wide applications in the design of filters and oscillators as well as in the cancellation of unavoidable parasitic capacitances [1–4]. The industry's recent trend toward integration and miniaturization has made the inductance simulator design a popular research topic.

A survey of recent literature reveals that various approaches are used in the realization of floating inductors [5–15]. In [5], a digitally tunable floating inductor using two current differential amplifiers (CDAs), two resistors and an array of five floating capacitors, each one connected to a switch, is reported. The value of the achieved inductor is changed by controlling the bits applied to the switches. The main drawback of this approach is the large number of floating capacitors used in the implementation and the need for digital controlling. Another approach based on four second-generation current conveyors (CCII), one grounded capacitor, two grounded resistors and an array of ten floating resistors,

each one connected to a switch, is reported in [6] for a digitally programmable floating inductance. The equivalent value of the resistor array is changed by controlling the bits applied to the switches; therefore, the value of the achieved simulated inductor is defined. Compared to the digitally programmable floating inductor of [5], the circuit of [6] does not employ floating capacitors. However, its operation depends on the matching between two resistors connected to the Y and X terminals of the first CCII. Moreover, to precisely define the value of the achieved inductor, the value of the resistors connected to switches must be trimmed carefully. The solution reported in [7] utilizes three current differencing transconductance amplifiers (CDTAs) and one grounded capacitor. Electronic tunability is achieved by changing the transconductance of the used ABBs through increasing the bias current, which results in high power consumption. In [8], only one differential voltage current conveyor transconductance amplifier (DVCCCTA) is used as ABB. Electronic tuning is performed through increasing the bias current, which sacrifices power consumption and the quality of the achieved inductor. The latter occurs because, by increasing the bias current, the value of the parasitic resistors connected in parallel to the simulated inductor are reduced, which limits its overall performance. In [9], one dual output differential difference current conveyor (DO-DDCC), two resistors and one grounded capacitor are used to design a floating inductor simulator. Unfortunately, the achieved inductance lacks electronic tuning capability, and its operation relies on the matching between the used resistors. The topology reported in [10] utilizes one differential voltage current conveyor (DVCC), one current controlled current conveyor (CCCII), one grounded resistor and one floating capacitor. Using the electronic controlling capability of CCCII, the achieved inductor is electronically tunable. However, as the bias current is increased to change the value of the achieved inductor, power consumption is increased accordingly. In addition, the topology is not desirable from an integration point of view due to the used floating capacitor. In [11], an attempt is made to design a floating inductor simulator using active building blocks only, which utilizes one current controlled conveyor transconductance amplifier (CCCTA) and one operational amplifier (OA). Although it is claimed that the proposed topology is capacitor free, its operation relies on the compensation capacitor used in the internal structure of OA. In addition, the circuit suffers from high power consumption and limited frequency range due to the limited frequency performance of OA. In [12], two differential voltage-to-current converters, two resistors and one capacitor are used. In [13], another topology using two differential difference current conveyors, two resistors and one grounded capacitor is introduced. The circuit reported in [14] employs two modified current feedback operational amplifiers (MCFOAs), two resistors and one grounded capacitor. The main weakness of [12–14] is the lack of electronic tunability. In [15], a different topology based on CCII $\pm$, one dual output transconductance amplifier (DO-OTA), one resistor and one floating capacitor is used. It is electronically tunable, but it employs a floating capacitor. In addition, as the bias current of DO-OTA is increased to tune the value of the simulated capacitor, the value of the parasitic parallel resistors is reduced, which causes the quality of the simulated inductor to deteriorate.

Recently, a new active building block called a second-generation voltage conveyor (VCII) [16–20], which is the dual circuit of well-known CCII, has been employed in the design of grounded impedance simulators [21,22]. Comparison shows that the simulated grounded capacitors and inductors using VCII exhibit many advantages, namely, simpler realizations, reduced error, reduced parasitics, lower power consumption, etc., over simulated grounded impedances utilized by other ABBs. From the reported results in [21,22], the use of VCII in realizing impedance simulators looks quite promising. In this paper, we aim to employ VCII in realizing a floating inductor simulator. The proposed topology is resistor-less and uses three VCII and one grounded capacitor. Instead of passive resistors, the internal resistors at the Y terminals of the used ABBs are used. The proposed topology has the capability to simulate both positive and negative inductors. The value of the simulated inductor is easily adjusted by a control current which is used to change the value of the Y terminal impedance of the used VCII. To provide low voltage operation, the

$$\begin{bmatrix} I_{X+} \\ I_{X-} \\ V_{Z+} \\ V_{Z-} \\ V_Y \end{bmatrix} = \begin{bmatrix} \beta_+ & \frac{1}{r_{x+}} + sC_{x+} & 0 & 0 & 0 \\ -\beta_- & 0 & \frac{1}{r_{x-}} + sC_{x-} & 0 & 0 \\ 0 & \alpha_+ & 0 & r_{z+} & 0 \\ 0 & 0 & \alpha_- & 0 & r_{z-} \\ r_Y & 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} I_Y \\ V_{X+} \\ V_{X-} \\ I_{Z+} \\ I_{Z-} \end{bmatrix} \quad (2)$$

In (2), the current gain between Y and X+ are shown by β_+ while the one between Y and X− are shown by $-\beta_-$ with ideal values of unity. The voltage gain between the X+ and Z+ terminals is shown by α_+ and the voltage gain between the X− and Z− terminals is shown by α_- with ideal values of unity. Here, r_{x+} , r_{x-} , r_{z+} and r_{z-} are parasitic impedances at the X+, X−, Z+ and Z− terminals, respectively, with ideal values of infinite, infinite, zero and zero, respectively. The parasitic resistor r_Y is designed at a non-zero value which can be electronically varied through I_{con} . In (1) and (2), the parasitic capacitors at the X terminals are shown by C_{x+} and C_{x-} which have ideal values of zero.

In the ideal case analysis, the values of β and α are assumed to be unitary. The parasitic impedances at the X and Z ports are assumed as infinite and zero, respectively. The values of the Y port impedances are shown by r_{Y1} , r_{Y2} and r_Y for $VCII^-_1$, $VCII^+_2$ and $VCII^\pm$, respectively.

By these assumptions, the operation of the proposed circuit of Figure 1 can be analyzed as follows. Using (2) for V_{Z+} and V_{Z-} we have:

$$V_{Z+} = V_1, \quad V_{Z-} = V_2 \quad (3)$$

where V_1 and V_2 are input voltages. At the Y terminals of $VCII^-_1$ and $VCII^+_2$, proportional currents are produced through r_{Y1} and r_{Y2} as:

$$i_{Y1} = \frac{V_{Z+}}{r_{Y1}} = \frac{V_1}{r_{Y1}} \quad (4)$$

$$i_{Y2} = \frac{V_{Z-}}{r_{Y2}} = \frac{V_2}{r_{Y2}} \quad (5)$$

Using (1), (4) and (5), the current produced at C is found as:

$$i_C = \frac{V_1}{r_{Y1}} - \frac{V_2}{r_{Y2}} \quad (6)$$

By assuming $r_{Y1} = r_{Y2} = r$, from (6), V_C is found as:

$$V_C = \frac{V_1 - V_2}{sCr} \quad (7)$$

From (2), V_C is transferred to the Z_1 terminal where it is converted to a proportional current through the Y terminal impedance of $VCII^\pm$ as:

$$i_Y = \frac{V_1 - V_2}{sCrr_Y} \quad (8)$$

where r_Y is the electronically variable impedance at the Y terminal of $VCII^\pm$. From (8), the value of the simulated inductor is found as:

$$L_{eq} = Crr_Y \quad (9)$$

To achieve negative impedance values, we need to change the connection of the Z terminals of $VCII^\pm$ and the Y terminals of $VCII^-_1$ and $VCII^+_2$, as shown in Figure 2. Similarly, it can be shown that the simulated inductor of Figure 2 is:

$$L_{eq} = -Crr_Y \quad (10)$$

Figure 2. The proposed floating negative inductor simulator.

3. Non-Ideal Analysis

Figure 3 shows the proposed inductor simulator topology in which all parasitic elements of the used ABBs are shown. A complete non-ideal analysis of the proposed circuit can be performed as follows.

Figure 3. The floating inductor simulator with parasitic elements.

Using (1) and performing a simple analysis using the Kirchhoff current and voltage laws (KCL, KVL) i_{Y1} and i_{Y2} are found as:

$$i_{Y1} = \frac{V_{Z+}}{r_{z+} + r_{Y1}} = \frac{\alpha^+ V_1}{r_{z+} + r_{Y1}} \quad (11)$$

$$i_{Y2} = \frac{V_{Z-}}{r_{z-} + r_{Y2}} = \frac{\alpha^- V_2}{r_{z-} + r_{Y2}} \quad (12)$$

Again using (1) and performing a KCL analysis, V_C is found as:

$$V_C = [\beta_1 i_{Y1} - \beta_2 i_{Y2}] \frac{r_{eq}}{1 + sC_{eq}r_{eq}} \quad (13)$$

where:

$$r_{eq} = \left(\frac{1}{r_{x1}} + \frac{1}{r_{x2}} \right)^{-1} \quad (14)$$

$$C_{eq} = C_{x1} + C_{x2} + C_1 \quad (15)$$

Inserting (11) and (12) into (13) results in:

$$V_C = \frac{r_{eq}}{1 + sC_{eq}r_{eq}} \left[\frac{\beta_1 \alpha^+ V_1}{r_{z+} + r_{Y1}} - \frac{\beta_2 \alpha^- V_2}{r_{z-} + r_{Y2}} \right] \quad (16)$$

Using (1), (2) and (16), i_Y is found as:

$$i_Y = \frac{\alpha_1 r_{eq}}{1 + sC_{eq}r_{eq}} \left[\frac{\beta_1 \alpha^+ V_1}{r_{z+} + r_{Y1}} - \frac{\beta_2 \alpha^- V_2}{r_{z-} + r_{Y2}} \right] \quad (17)$$

From the matrix equation of (2), by ignoring the effect of r_{x+} and r_{x-} , I_1 and I_2 are:

$$I_1 = \frac{\alpha_1 r_{eq} \beta^+}{(1 + sC_{eq}r_{eq})(r_{z1} + r_Y)} \left[\frac{\beta_1 \alpha^+ V_1}{r_{z+} + r_{Y1}} - \frac{\beta_2 \alpha^- V_2}{r_{z-} + r_{Y2}} \right] \quad (18)$$

$$I_2 = -\frac{\alpha_1 r_{eq} \beta^-}{(1 + sC_{eq}r_{eq})(r_{z1} + r_Y)} \left[\frac{\beta_1 \alpha^+ V_1}{r_{z+} + r_{Y1}} - \frac{\beta_2 \alpha^- V_2}{r_{z-} + r_{Y2}} \right] \quad (19)$$

Assuming $(r_{z+} + r_{Y1}) = (r_{z-} + r_{Y2}) = r'$ and $(r_{z1} + r_Y) = r''$, (18) and (19) become:

$$I_1 = \frac{\alpha_1 r_{eq} \beta^+}{(1 + sC_{eq}r_{eq})r' r''} [\beta_1 \alpha^+ V_1 - \beta_2 \alpha^- V_2] \quad (20)$$

$$I_2 = -\frac{\alpha_1 r_{eq} \beta^-}{(1 + sC_{eq}r_{eq})r' r''} [\beta_1 \alpha^+ V_1 - \beta_2 \alpha^- V_2] \quad (21)$$

By defining the voltage gain and current gain parameters of the used VCII as:

$$\beta_1 = 1 \pm \varepsilon \quad (22)$$

$$\beta_2 = 1 \mp \varepsilon \quad (23)$$

$$\alpha^+ = 1 \pm \varepsilon' \quad (24)$$

$$\alpha^- = 1 \mp \varepsilon' \quad (25)$$

$$\beta^+ = 1 \pm \varepsilon'' \quad (26)$$

$$\beta^\mp = 1 \mp \varepsilon'' \quad (27)$$

where $\varepsilon \ll 1$, $\varepsilon' \ll 1$ and $\varepsilon'' \ll 1$ are gain errors, and inserting (22)–(27) into (20) and (21) and simplifying the results gives:

$$I_1 \approx \frac{\alpha_1 r_{eq} \beta^+}{(1 + sC_{eq}r_{eq})r' r''} [1 - (\pm \varepsilon \pm \varepsilon' \pm \varepsilon'')](V_1 - V_2) \quad (28)$$

$$I_2 \approx -\frac{\alpha_1 r_{eq} \beta^-}{(1 + sC_{eq}r_{eq})r' r''} [1 - (\pm \varepsilon \pm \varepsilon' \pm \varepsilon'')](V_1 - V_2) \quad (29)$$

From (28), (29) L_{eq} and its series impedance R_{seri} are found as:

$$L_{eq} \approx C_{eq}r' r \quad (30)$$

$$R_{seri} = \frac{r' r''}{r_{eq}} \quad (31)$$

As can be seen from (30), the value of L_{eq} can be varied by r_Y . From (14) and (31), it is also deduced that as the value of r_{eq} is much larger than r_{Y1} , r_{Y2} and r_Y , the value of R_{seri} is low. The equivalent circuit of the proposed capacitor simulator is shown in Figure 4, where L_{eq} is the proposed electronically tunable equivalent floating inductor. r_x and C_x are the parasitic parallel resistance and capacitance and R_{seri} is the parasitic series resistance of the simulated inductor. Similar analysis can be performed for the negative inductance simulator which is not repeated here.

Figure 4. The equivalent circuit of the proposed floating L simulator.

4. CMOS Implementation of VCII

A simple realization of the internal structure of $VCII^\pm$ is shown in Figure 5a. The input section at the Y port is composed of transistors M_1 and M_2 , I_{con} , I_{B1} and I_{B2} . Transistor M_2 is used in common gate structure and the bias voltage at its gate is provided by diode connected transistor M_1 . The impedance at the Y terminal is:

$$r_Y = \frac{1}{gm_{M2}} \quad (32)$$

where gm_{M2} (with usual meaning of symbols) is:

$$gm_{M2} = \sqrt{\mu C_0 \frac{W_{M2}}{L_{M2}} (I_{con} + I_{B1})} \quad (33)$$

From (33), by increasing the value of I_{con} , the value of gm_{M2} will be increased and according to (32), the value of r_Y will be reduced. To reduce power consumption, I_{con} is added to the drain of M_2 to keep the bias current at other branches constant. To set the zero-offset voltage at Y port, I_{con} is also added to the drain of M_1 . This is performed by transistors M_{B11} – M_{B16} .

The input current applied to the Y terminal is transferred to the X+ terminal through a simple current mirror made of M_3 and M_4 . On the other hand, the input current at the Y terminal is transferred to the X– terminal by transistors M_3 , M_4 , M_{10} – M_{12} . The voltage produced at the X+ terminal is transferred to the Z+ terminal through a voltage buffer made of M_5 – M_9 . Similarly, the voltage produced at the X– terminal is transferred to the Z– terminal through a voltage buffer of M_{14} – M_{18} . Transistors M_{Bi} for $i = 1$ – 10 are used for biasing. A simple analysis gives the parasitic elements at the X+, X– Z+ and Z– terminals as:

$$r_{X+} = r_{oM4} \parallel r_{oMB3} \quad (34)$$

$$C_{X+} = C_{dsM4} + C_{dgM4} + C_{dsMB3} + C_{dgMB3} \quad (35)$$

$$r_{X-} = r_{oM12} \parallel r_{oMB10} \quad (36)$$

$$C_{X-} = C_{dsM12} + C_{dgM12} + C_{dsMB10} + C_{dgMB10} \quad (37)$$

$$r_{Z+} = \frac{1}{gm_{M9} gm_{M5} (r_{oM8} \parallel r_{oM6})} \quad (38)$$

$$r_{Z-} = \frac{1}{gm_{M18}gm_{M14}(r_{oM15}||r_{oM17})} \quad (39)$$

where for i th transistor, r_{oM_i} is the drain-source impedance, gm_{M_i} is the transconductance and r_{oMB_i} is the drain source impedance and Cds_{M_i} and Cdg_{M_i} are the drain-source capacitance and drain-gate capacitance of the related transistor.

Figure 5. CMOS implementation of (a) electronically controllable $VCII^\pm$, (b) $VCII^+$ and (c) $VCII^-$.

The implementation of the VCII^+ and the VCII^- are shown in Figure 5b,c, respectively. Here, transistor M_2 is configured in a common gate structure and the diode connected transistor M_1 provides proper biasing at the gate of M_1 . A simple current mirror made of M_3 and M_4 in Figure 5b, and current mirrors made of M_3 and M_4 , and M_5 and M_6 in Figure 5c, are used to transfer the Y port input current to the X ports. The voltage produced at the X ports is transferred to the Z ports by a voltage buffer made of M_5 – M_9 in Figure 5b and M_7 – M_{11} in Figure 5c.

Parasitic elements are found as:

$$r_{Y1} = r_{Y2} = \frac{1}{g_{mM2}} = \left[\sqrt{\mu C_0 \frac{W_{M2}}{L_{M2}}} I_{B1} \right]^{-1} \quad (40)$$

$$r_{Z1} = \frac{1}{g_{mM9} g_{mM5} (r_{oM8} \parallel r_{oM6})} \quad (41)$$

$$r_{Z2} = \frac{1}{g_{mM11} g_{mM7} (r_{oM10} \parallel r_{oM8})} \quad (42)$$

$$r_{X1} = r_{oM4} \parallel r_{oMB3} \quad (43)$$

$$r_{X2} = r_{oM6} \parallel r_{oMB7} \quad (44)$$

$$C_{X1} = C_{dsM4} + C_{dgM4} + C_{dsMB3} + C_{dgMB3} \quad (45)$$

$$C_{X2} = C_{dsM6} + C_{dgM6} + C_{dsMB7} + C_{dgMB7} \quad (46)$$

5. Simulation Results

PSpice simulations of the proposed floating inductors of Figures 1 and 2 based on 0.18 μm CMOS technology and supply voltage of ± 0.9 V are performed. The aspect ratios for the used PMOS and NMOS transistors are 9 $\mu\text{m}/0.9$ μm and 27 $\mu\text{m}/0.9$ μm , respectively. The values of the bias currents are $I_B = I_{B1} = I_{B2} = I_{B3} = 20$ μA . All bias currents are realized by simple current mirrors. The performance parameters and parasitic elements of the used ABBs are reported in Table 1.

Table 1. The simulated characteristics of $\text{VCII}^\pm$, VCII^+ and VCII^- .

	$\text{VCII}^\pm$	VCII^-	VCII^+
r_Y	$I_{con} = 0$ μA	3.43 k Ω	
	$I_{con} = 25$ μA	2.18 k Ω	3.43 k Ω
	$I_{con} = 50$ μA	1.8 k Ω	
	r_X	$r_{X+} = 240$ k Ω , $r_{X-} = 244$ k Ω	240 k Ω
r_Z		$r_{Z-} = r_{Z+} = 48$ Ω	48 Ω
	α	$\alpha_+ = \alpha_- = 0.981$	0.981
	$I_{con} = 0$ μA	$\beta_+ = 1.007$, $\beta_- = 1.04$	
	$I_{con} = 25$ μA	$\beta_+ = 0.988$, $\beta_- = 1.03$	1.042
β	$I_{con} = 50$ μA	$\beta_+ = 0.999$, $\beta_- = 1.023$	1.002
	C_x	$C_{X+} = 48$ fF, $C_{X-} = 64$ fF	74 fF
Power dissipation		0.352–0.625 mW	0.242 mW

For $C_1 = 50$ pF, Figure 6 shows the phase and magnitude frequency response of the proposed floating inductor for $I_{con} = 0$ μA , $I_{con} = 25$ μA and $I_{con} = 50$ μA . The proposed circuit frequency range is from 100 kHz to 3 MHz.

Table 2 shows the value of the achieved inductance for different values of I_{con} for both theoretical and simulated values. As can be seen, the error for L_{eq} remains below 4.8%. Fortunately, the maximum value of R_{seri} remains at 76 Ω .

Figure 6. Frequency response of magnitude and phase for the proposed (a) positive and (b) negative floating inductor simulator.

Table 2. Deviation between theoretical and ideal values at different control currents.

	I_{con}	Calc. R_{seri}	Sim. R_{seri}	Calc. Leq	Sim. Leq	% of Error in Leq
Negative simulator	0	97 Ω	76 Ω	588 μH	−576 μH	−2%
	25 μA	61 Ω	50.2 Ω	374 μH	−382 μH	2.1%
	50 μA	51 Ω	43 Ω	309 μH	−324 μH	4.8%
Positive simulator	0	97 Ω	76 Ω	588 μH	576 μH	−2%
	25 μA	61 Ω	49 Ω	374 μH	366 μH	−2.9%
	50 μA	51 Ω	42 Ω	309 μH	316 μH	2.3%

To test the time domain response of the proposed inductor simulator, a sinusoidal input voltage with a peak-to-peak value of 80 mV and frequency of 1 MHz is used as the input signal to the simulated inductor. The output signal phase is 93.6° and -86.4° for positive and negative types, respectively. The resulting outputs are shown in Figure 7.

The functionality of the proposed floating inductor is tested on a standard RLC band-pass filter for $C_1 = 50$ pF, $R_L = 10$ k Ω shown in Figure 8. Figure 9 shows the frequency response of the RLC band-pass filter for both the ideal and the simulated inductance. The simulated value of f_0 is 1.04 MHz, 1.39 MHz and 2.39 MHz for $I_{con} = 0$ μA , $I_{con} = 25$ μA and $I_{con} = 50$ μA , respectively.

The robustness of the design was tested as well. In particular, Tables 3–5 show the PVT variations of the $VCII^\pm$, $VCII^+$ and $VCII^-$ ABBs, respectively, while in Table 6, the same variations are tested for the actual equivalent inductor value. Simulations have been

reported at different I_{con} levels. Results show that, regardless of the conditions, values always remain within 3% of the nominal ones reported along the manuscript concerning the ABBs parameters, while they remain within 11% when it comes to the equivalent inductor value.

Figure 7. Time domain response of the proposed (a) positive and (b) negative floating inductors.

Table 3. PVT simulation results for $VCII^{\pm}$.

Parameter		P				V (Vdd-Vss)		T (°C)		
		FF	SF	FS	SS	±0.99 V	±0.81 V	−20	25	80
r_Y (Ω)	$I_{con} = 0 \mu A$	3.36 k	3.41 k	3.416 k	3.5 k	3.395 k	3.462 k	2.985 k	3.45 k	3.944 k
	$I_{con} = 25 \mu A$	2.21 k	2.16 k	2.168 k	2.2 k	2.18 k	2.22 k	1.87 k	2.16 k	2.52 k
	$I_{con} = 50 \mu A$	1.75 k	1.78 k	1.79 k	1.81 k	1.76 k	1.86 k	1.52 k	1.77 k	2.11 k
$[r_{X+}, r_{X-}]$ kΩ		[238, 205]	[243, 132]	[240, 243]	[245, 242]	[225, 242]	[242, 248]	[200.1, 200]	[242, 239]	[249, 287.4]
$r_{Z+} = r_{Z-}$ (Ω)		45	47.6	45	49	51	54	54	47.6	50.2
$\alpha+ = \alpha-$		0.981	0.980	0.990	0.980	0.982	0.978	0.980	0.981	0.980
$\beta+, \beta-$	$I_{con} = 0 \mu A$	1.01, 1.047	1.01, 1.046	0.993, 1.029	1.004, 1.026	1.009, 1.057	1.011, 1.065	1.018, 1.066	1.01, 1.047	1.005, 1.03
	$I_{con} = 25 \mu A$	1, 1.038	1, 1.036	1, 1.0368	0.999, 1.035	1.006, 1.046	1.056, 1.006	1.006, 1.055	1, 1.037	0.995, 1.021
	$I_{con} = 50 \mu A$	0.993, 1.031	0.993, 1.029	0.993, 0.980	0.992, 1.028	0.999, 1.049	0.997, 1.009	0.999, 1.047	0.993, 1.03	0.988, 1.015
C_{X+}, C_{X-} (fF)		49, 80	59, 81	61, 77	58, 64	59, 119	34, 60	92, 94	61, 77	68, 81
Power Dissipation (μW)		313–583	353–625	317–605	313–625	332–657	313–553	356–630	353–625	350–620

Figure 8. Application of simulated Floating L as a RLC band-pass filter.

(a)

(b)

(c)

Figure 9. Frequency response of the RLC band-pass filter for different values of I_{con} (a) $0 \mu A$ (b) $25 \mu A$ and (c) $50 \mu A$.

Table 4. PVT simulation results for $VCII^+$.

Parameter	P				V (Vdd-Vss)		−20	T (°C)	
	FF	SF	FS	SS	±0.99 V	±0.81 V		25	80
r_Y	3.38 k Ω	3.43 k Ω	3.44 k Ω	3.49 k Ω	3.4 k Ω	3.5 k Ω	3 k Ω	3.4 k Ω	4 k Ω
r_X	250 k Ω	250 k Ω	250.3 k Ω	252.6 k Ω	250 k Ω	251 k Ω	205 k Ω	249 k Ω	302 k Ω
r_Z	46 Ω	47 Ω	47.1 Ω	48.4 Ω	50 Ω	88 Ω	43 Ω	54 Ω	72 Ω
α	0.981	0.981	0.984	0.983	0.986	0.978	0.980	0.973	0.974
β	1.0026	1.0023	1.0023	0.9966	1.008	0.996	1.008	0.996	0.993
c_x	32 fF	41 fF	38 fF	38.1 fF	32 fF	37 fF	37 fF	39 fF	40 fF
Power dissipation	202 μ W	203 μ W	202 μ W	201 μ W	224 μ W	186 μ W	204 μ W	203 μ W	202 μ W

Table 5. PVT simulation results for $VCII^-$.

Parameter	P				V (Vdd-Vss)		−20	T (°C)	
	FF	SF	FS	SS	±0.99 V	±0.81 V		25	80
r_Y	3.36 k Ω	3.41 k Ω	3.41 k Ω	3.46 k Ω	3.39 k Ω	3.46 k Ω	2.97 k Ω	3.4 k Ω	3.94 k Ω
r_X (k Ω)	211 k Ω	212 k Ω	212.5 k Ω	214 k Ω	199 k Ω	223 k Ω	178.44 k Ω	206.3 k Ω	252 k Ω
r_Z (Ω)	46.5 Ω	47.7 Ω	47.6 Ω	49 Ω	46.2 Ω	52.5 Ω	42 Ω	46 Ω	54 Ω
α	0.981	0.980	0.984	0.980	0.986	0.976	0.980	0.980	0.980
β	1.048	1.046	1.046	1.045	1.0665	1.027	1.066	1.047	1.038
c_x	110 fF	112 fF	115 fF	110 fF	119 fF	130 fF	107 fF	113 fF	115 fF
Power dissipation	190 μ W	200 μ W	190 μ W	190 μ W	228 μ W	187 μ W	191 μ W	190 μ W	189 μ W

Table 6. PVT simulation results for the achieved L_{eq} at different control currents.

		+ L_{eq} (μ H)									− L_{eq} (μ H)								
		I _{con} = 0 μ A			I _{con} = 25 μ A			I _{con} = 50 μ A			I _{con} = 0 μ A			I _{con} = 25 μ A			I _{con} = 50 μ A		
		S. ¹	C. ²	E. ³ (%)	S.	C.	E. (%)	S.	C.	E. (%)	S.	C.	E. (%)	S.	C.	E. (%)	S.	C.	E. (%)
P	FF	538	580	−7.2	360	382	−5.7	309	311	−0.6	539	583	−7.5	361	378	−4.5	310	312	−0.64
	SF	571	597	−4.3	379	341	+11	323	316	+2.2	573	601	−4.6	378	384	−1.5	324	318	+1.9
	FS	571	597	−4.3	379	342	+11	324	323	+0.3	572	603	−5.1	378	386	−2	323	320	+1
	SS	605	622	−2.7	396	389	+1.8	338	320	+5.6	606	628	−3.5	396	400	−1	338	329	+2.7
V (V)	±0.99	523	591	−11.5	362	383	−5.4	317	314	+1	484	591	−11.5	362	390	−7.1	317	312	+1.6
	±0.81	566	606	−6	385	392	−1.8	338	318	+6.2	563	624	−9.8	385	404	−4.7	338	340	−0.6
T (°C)	−20	428	458	−6.5	307	289	+6.2	234	236	−0.8	423	462	−8.4	307	292	+5.2	234	239	−2
	25	568	602	−5.6	356	380	−6.3	308	313	−1.6	569	603	−5.6	357	380	−6	306	313	−1
	80	877	797	+10	483	513	−5.8	423	432	−2	879	810	+8	483	521	−7.3	423	438	+3.4

¹ simulation, ² Calculation, ³ Error.

Monte Carlo simulations have been performed and reported in Table 7 as well. They have been conducted emulating a 1% mismatch in the β parameter with an overall of 50 runs. As can be seen, the spread between minimum and maximum value increases as the control current reduces. This is expected and depends on the fact that the error from the mirroring action of the current mirrors is more relevant at a low bias current. It could be mitigated, for instance, using cascaded structures if the voltage swing is not a strong issue.

A comparison between the proposed circuit and other previously reported ones is presented in Table 8. As can be seen, compared to other works, the proposed circuit provides full integration as it is resistor-free and uses only one grounded capacitor. Although the circuit reported in [11] is also resistor-free, it includes a floating compensation capacitor inside the used OA. Moreover, the proposed floating inductor can provide both positive (+L) and negative (−L) inductance values. Although the circuits reported in [5,6] are electronically tunable, the large number of capacitors and resistors which their values must trim is their weakness. The circuits reported in [7,8,10,11] are electronically tunable but they can provide only +L. The circuits reported in [9,12–15] are not electronically tunable.

Table 7. Monte Carlo for 1% mismatch in β and 50 runs.

		$+L_{eq}$ (μH)				$-L_{eq}$ (μH)			
		Max	Min	Mean	Typical	Max	Min	Mean	Typical
I_{con}	0 μA	1221	453	672	576	1710	459	749	576
	25 μA	580	362	427	366	529	359	416	389
	50 μA	500	316	355	316	431	315	349	324

Table 8. Comparison between proposed circuit and other reported works.

Ref.	Frequency Range	+L/−L	Vdd-Vss	Tuning	#R	#Float. C	ABB
[5]	NA	+L	NA	Digital		5	2CDA
[6]	NA	+L	± 1.5 V	Digital	10	0	4CCII
[7]	1 Hz–1 MHz	+L	± 2.5 V	Yes		0	3CDTA
[8]	100 kHz–10 MHz	+L	± 2 V	Yes	1	0	1DVCCTA
[9]	10 kHz–400 kHz	+L	± 1.5 V	No	2	0	1DO DDCC 1DVCC
[10]	NA	+L	± 1.25 V	Yes	1	1	1CCCII ¹ 1Gm 1CCCII ²
[11]	NA	+L	± 5 V	Yes	0	0	1CCCCTA OA
[12]	1 kHz–10 MHz	+L	± 0.75 V	No	2	0	2DTVC
[13]	<10 MHz	+L	± 0.75 V	No	2	0	2DDCC
[14]	10 kHz–10 MHz	+L	± 1.5 V	No	2	0	2MCFOA
[15]	NA	+L	NA	No	1	1	1CCII $\pm$ 1DO OTA
this	0.1–3 MHz	L $\pm$	± 0.9 V	Yes	0	0	1VCII $\pm$ 1VCII ⁺ VCII [−]

¹ Topology one; ² Topology two.

6. Conclusions

In this paper, we present a new topology for implementing either a positive or negative floating inductor multiplier. One VCII[±], one VCII⁺, one VCII[−] and a single grounded capacitor are used. Instead of passive resistors, intrinsic resistors at the Y terminals of VCII are used. The value of the simulated inductor is tunable by a control current. The circuit enjoys low voltage and low power operation, reduced series resistance and offers fewer errors compared to other works. Non-ideal analysis is given by taking into account the non-ideal gains and parasitic impedances of the active elements that are used. The proposed circuit enjoys a simple implementation and is free from any restricting matching requirements. The application of the proposed circuit as a standard RLC filter is also given to verify its functionality.

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