electronics

MDPI

Article

Research on Topology Recognition Technology Based on Intelligent Measurement Switches

Dezhi Xiong [1] and Jingjuan Du [2,*]

[1] Hunan Province Key Laboratory of Intelligent Electrical Measurement and Application Technology (State Grid Hunan Electric Power Limited Company Power Supply Service Center (Metrology Center)), Changsha 410007, China
[2] School of Control and Mechanical Engineering, Tianjin Chengjian University, Tianjin 300384, China
* Correspondence: dujj@tcu.edu.cn; Tel.: +86-13672199875

Abstract: Distribution network topology identification provides information on low-voltage station areas in a power system. However, it requires either heavy computation or additional measuring equipment. This paper proposes topology identification technology based on intelligent measurement switches. The topology is identified by using the characteristic current measured by the designed intelligent measurement switch. The modulation/demodulation method and information encoding method for the topology identification are presented. The communication protocol stack structure and message encapsulation format of the topology identification unit are designed. The experimental verification and analysis show that the topology identification technology proposed in this paper has a short identification time and an identification accuracy of 100%, and it can be widely promoted and applied in low-voltage distribution networks.

Keywords: topology identification; intelligent measurement switch; smart grids

Citation: Xiong, D.; Du, J. Research on Topology Recognition Technology Based on Intelligent Measurement Switches. *Electronics* **2022**, *11*, 3903. https://doi.org/10.3390/electronics11233903

Academic Editor: Ryszard Sroka

Received: 26 October 2022
Accepted: 22 November 2022
Published: 25 November 2022

1. Introduction

As the State Grid Corporation's investment in the construction of smart grids continues to increase, the construction of smart grids has achieved remarkable results. The functions of smart grids, such as monitoring power quality [1,2], photovoltaic power generation consumption [3,4], line loss management and anti-theft purposes [5,6], are widely used. However, because the topology of the current system is inconsistent with the actual topology, the accuracy of its results are greatly reduced. In a low-voltage distribution network, the lack or inaccuracy of network topology information is a problem worthy of attention. Accurate user-side phases and topological connection relations are of great significance to the operation and maintenance management of a distribution network. Usually, a power company records and manages the network connection information of various power distribution equipment and assets in the enterprise geographic information system. However, a considerable number of enterprise Geographic Information Systems (GISs) only cover medium-voltage distribution networks, and there is little information about low-voltage distribution networks. Due to the extensive coverage of distribution networks, there are rapid changes in power supply and a lack of working resources and effective technical means to establish a low-voltage network topology downstream of the distribution transformer, coupled with frequent line upgrades and an increase in new customers. There is no topology record of low-voltage distribution networks in most domestic power companies' GISs. Manual online investigations are time-consuming and laborious, and there is no automatic system change after a topology change. Y. Li et al. [7] proposed a new method for topology identification based on the inner desynchronization of a Hindmarsh–Rose neural network. Through this method, the original neural network can achieve internal desynchronization, and topology observers can successfully identify unknown topologies. Y. CHEN et al. [8] proposed a novel two-stage method to identify

the connection relationship between distribution transformers and feeders. The proposed two-stage method can help operators correct topology errors. Y. Shen et al. [9] proposed a directed network topology inference method based on joint diagonalization (JD), developed three JD algorithms tailored for network topology inference and demonstrated them using simulation and real data tests. S. Li et al. [10] obtained effective results by fully mining the potentially effective information of the distribution network's big data and by applying it to the identification of the distribution network topology. In order to improve the success rate and efficiency of the automatic identification of low-voltage power distribution topology, C. Xu et al. [11] proposed a record-based topology identification method. This topology identification method has the advantages of simple control logic, fast identification speed and high identification accuracy. Y. Chen et al. [12] proposed a design technique for the topology generation of chapless radio frequency identification (RFID) tags and proposed a topology identification design method that does not require an iterative optimization process. Y. Liu et al. [13] proposed a distribution network topology error identification method based on distribution phasor measurement units (D-PMU) and branch state functions. This method uses telemetry and remote signaling information to identify a single topology error and multiple topology errors in a distribution network. In order to solve the task of blind topology identification, Z. Xiang et al. [14] proposed a topology identification method based on dictionary learning, which improves the accuracy of topology identification. In order to meet the calculation speed requirements of real-time network topology analysis, W. Deng et al. [15] proposed a two-layer calculation method that uses the K-nearest neighbor algorithm for rough judgment and mutual information for precise calculation, which shortens the running time and improves the calculation speed.

Current research mainly focuses on network topology identification and blind topology identification. Waarde et al. [16] studied topology identification for a more general class of so-called heterogeneous networks, in which the dynamics of the nodes were modeled by general (possibly distinct) linear systems. Farajollahi et al. [17] presented a new topology identification algorithm based on measurements from a few line current sensors, together with available pseudo-measurements for nodal power injections. Wang et al. [18] presented topology identification in two-layer complex dynamical networks. Coutino et al. [19] presented state-space network topology identification from partial observations. Zhao et al. [20] presented full-scale distribution system topology identification using a Markov random field. Cavraro et al. [21] presented bus clustering for distribution grid topology identification in a smart grid. It can be seen that research on the identification of the connection relationship between distribution transformers and feeders, as well as topology identification based on the distribution network's big data, has been carried out. Most topology identification methods require either heavy computation or additional measuring equipment.

An intelligent measurement switch is a popular protection device with the function of measuring power in a system. It has current protection functions (overload long delay protection, short circuit short delay protection and short circuit transient protection), voltage protection (over- and under-voltage protection, phase failure protection and frequency protection) and temperature protection functions. It also can also measure node voltage, current, power and frequency. Intelligent measurement switches are installed at all levels of a low-voltage distribution network, and nodes are completely distributed, which is convenient for the complete identification of the topology of the entire station area. Thus, distribution network topology identification based on intelligent measurement switches has the inherent advantage of a low cost. However, research on topology identification technology based on intelligent measurement switches has not yet carried out. This paper presents topology identification technology based on intelligent measurement switches. Firstly, a modulation/demodulation method and an information encoding method for the topology identification are presented. Then, the communication protocol's stack structure and the message encapsulation format of the topology identification unit are designed. Finally, a new type of intelligent measurement switch with the function of topology identification

is designed. In the proposed method, the distribution network's topology is identified by using the characteristic current measured with the designed intelligent measurement switch. Experiments validate the effectiveness of the proposed method.

2. Topology Identification Technology Solution

As mentioned in the Introduction, distribution network topology identification requires either heavy computation or additional measuring equipment. Intelligent measurement switches are installed at all levels of a low-voltage distribution network, and they can be potential devices for topology identification with the advantage of a low cost. This paper presents topology identification technology based on intelligent measurement switches. In the new designed intelligent measurement switch, the control circuit with the topology identification function is mainly composed of the main control unit module, power supply module, metering module, communication module, clock module, topology identification current generation module, etc. The schematic diagram of the control circuit is shown in Figure 1. The intelligent measurement switch developed based on this scheme can accurately identify the physical topology of the low-voltage distribution station area and can realize the online generation of the self-portrait structure diagram of the station area by using this system.

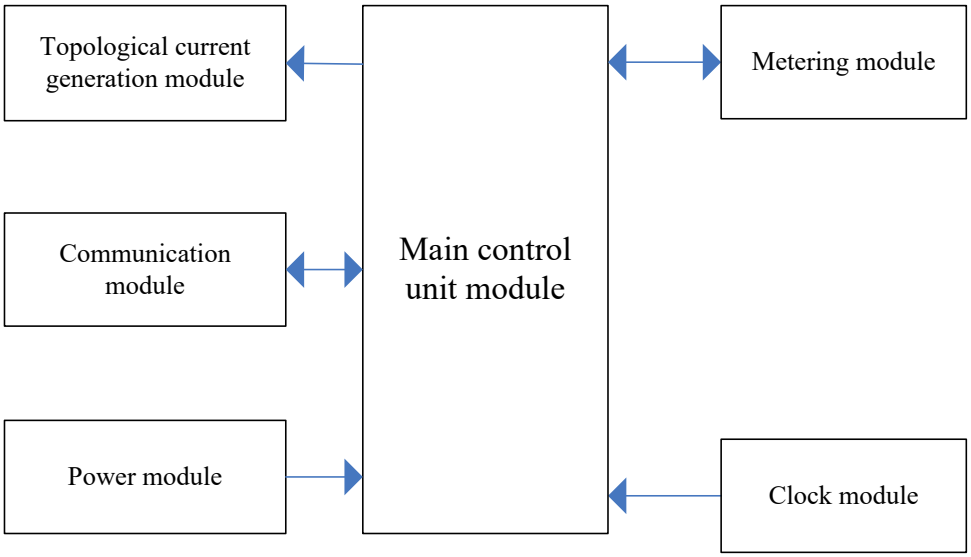

Figure 1. Schematic diagram of control circuit.

The main control unit module is used for the online processing of metering data and of topology identification commands collected by the smart measurement switch, receiving accurate time synchronization tasks set by the terminal and accurately timing the clock module of the smart measurement switch every day to ensure time consistency. The time deviation is less than 9 s. The main control unit module receives the time distribution, sends instruction, sends interval settings, etc., through the communication module, and it sorts and analyzes the collected time stamps to obtain the real physical topology. The main control unit module uses DMA for raw data storage. It reads the data in the DMA, and if it is greater than the critical value and is in the monitoring pulse signal state, the device sending this state is considered to be at the front end of the receiving module. The main control module is a circuit composed of a controller chip whose model is STM32F103RCT6.

The topology identification current generation module is used to generate the current encoding signal that can be recognized by other intelligent measurement switches in the same branch, and it performs voltage zero crossing detection (rising). After detecting the voltage zero crossing (fixed delay 2 ms), it waits for 7 ms and turns on the IO port corresponding to the main control unit module, carrying out a high current pulse injec-

tion. After zero crossing, it automatically shuts down and completes a short-time current pulse injection.

The metering module is used to collect the metering data of the smart measurement switch and to complete the accurate identification of the topology identification current. The metering module collects the topology identification current signal sent by the topology identification module of other smart measurement switches for data analysis. In the low-voltage station area, the network topology from the transformer to the branch box, from the branch box to the meter box and from the meter box to the household meter is automatically drawn, and the data are transmitted to the terminal, which are displayed in the form of an illustration. The metering module receives the topology identification command of the main control unit module, enters the signal monitoring state, receives and parses the current signal from other intelligent measurement switch topology identification generation modules in real time, determines its location and can also use the communication module to obtain the resulting feedback to the terminal.

The power supply module is used to supply power to the intelligent measurement switch. The power supply module includes a rectifier circuit and a voltage-stabilizing circuit. The rectifier circuit and the voltage-stabilizing circuit are connected in a series. The rectifier circuit is used to convert the AC power input from the power grid into DC power. The voltage-stabilizing circuit is used to convert DC power into stable DC power and supply power. The voltage-stabilizing circuit includes a 5 V power supply circuit and a 3.3 V power supply circuit. The 5 V power supply circuit is used to convert the DC power into a stable 5 V power supply voltage and supply power, and the 3.3 V power supply circuit is used to convert the 5 V power supply into a 3.3 V power supply and supply power.

The communication module is used for remote communication between the intelligent measurement switch and the upstream device. The clock module is used to realize accurate clock data for the intelligent measurement switch, and the clock module is a circuit composed of a clock chip of model RX8025T.

3. Key Technology of Topology Identification

3.1. Topology Identification Mechanism Based on the Characteristic Current

The characteristic electric current sending procedure is shown in Figure 2. The main control unit module issues a characteristic current signal sending instruction to the topology identification current generation module, and the topology identification current generation module controls the on and off states of the characteristic load to generate a characteristic current signal on the power line after receiving the instruction.

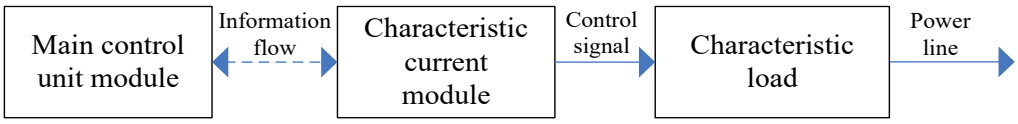

Figure 2. Characteristic current sending process.

The current characteristics of topological identification are shown in Figure 3. The switching frequency can be set, with the default being 833.3 Hz, and both high-level and low-level pulse widths can be set. The characteristic current's carried information can be set, the start symbol is AAH = 10101010C, the control code is E9H = 11101001C and the length of the subsequent extended domain information is variable. Among them, when the code bit is 0, there is no characteristic current transmission, and when the code bit is 1, there is a characteristic current transmission. The length of each bit code's sending time can be set, and the default is 600 ms $\pm$ 15 ms.

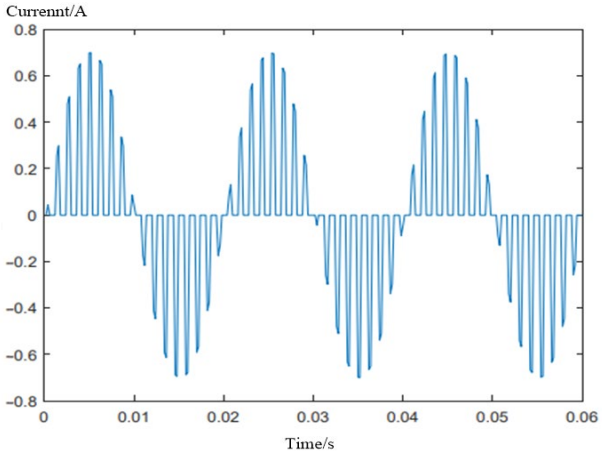

Figure 3. Topological identification of current characteristics.

3.2. Modulation Method Design

3.2.1. Modulation and Demodulation Process

The sending device forms a characteristic current signal and feeds it to the power line through a predetermined modulation method. The identification device CT detects the characteristic current signal, performs corresponding demodulation processing, finally restores the characteristic current signal on the power line to decode data information and makes a logical judgment. The modulation and demodulation process are shown in Figure 4.

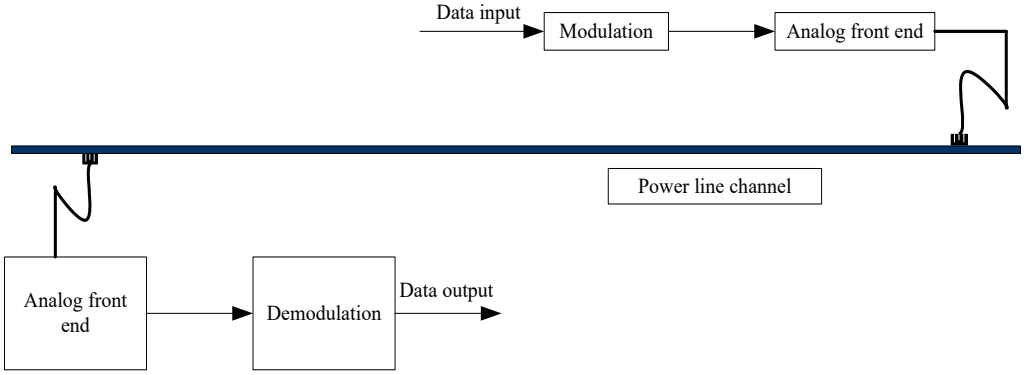

Figure 4. Signal modulation and demodulation process.

3.2.2. Modulation and Demodulation Process

Bulleted lists can be described as follows. Through OOK modulation, the presence or absence of a characteristic current with a fixed bit width is used to represent the '1' and '0' of the digital signal. The modulation carrier frequency f_1 is the switching frequency for sending the characteristic signal. The original information is modulated, and the signal is $m(t)$.

$$m(t) = \begin{cases} 0 \\ A * square(t, DUTY) \end{cases} \quad (1)$$

Among them, A represents the characteristic current amplitude, and DUTY represents the duty cycle of the characteristic signal. The modulation process is shown in Figure 5. For the modulation carrier frequency, the duration of each bit is the set bit width time. If the bit is 1, the frequency is used for switching within the bit duration; if the bit is 0, no switching is performed.

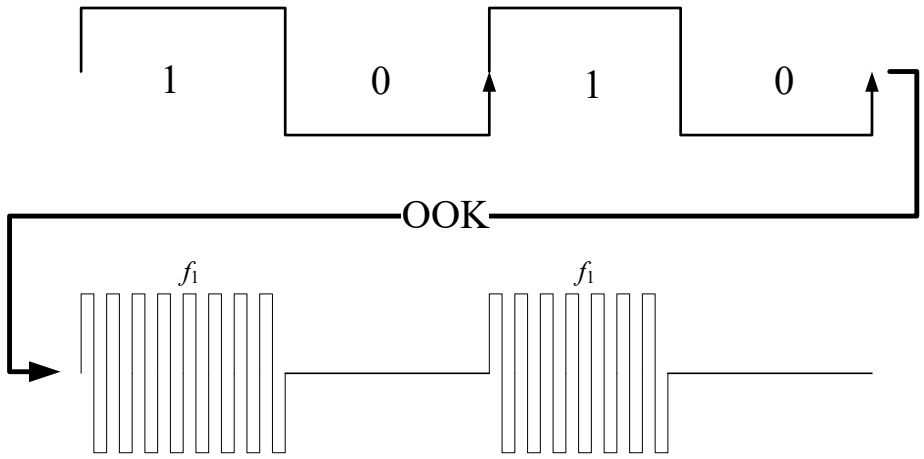

Figure 5. OOK modulation process.

An example of modulation implementation is shown in Figure 6. The modulation carrier frequency defaults to 833.3 Hz, and the duration of each bit is 0.6 s. If the bit is 1, a frequency of 833.3 Hz is used for switching during the duration of the bit; if the bit is 0, switching is not performed.

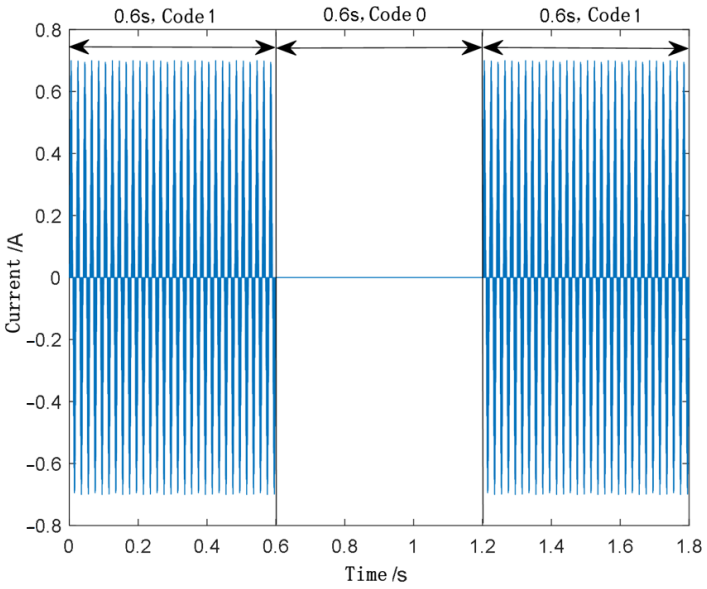

Figure 6. Schematic diagram of OOK modulation realization.

3.3. Topology Identification Program Flow

The topology identification process is shown in Figure 7. After the initialization procedure, the power-consuming terminal sends the 'clear topology data' instruction to all switches. After the topology data are cleared, it sends the 'send topology signal' instruction to the *i*-th switch and waits for 30 s. The *i* switch sends a signal, and the related switch recognizes the signal. The power-consuming terminal sends the 'query topology data' command to all switches, and the related switches return topology signals. Then, it sends the 'send topology signal' command to the $i + 1$th switch until the polling of all the switches to which it belongs is completed. It then analyzes the inquired topology data and forms a topology relationship diagram.

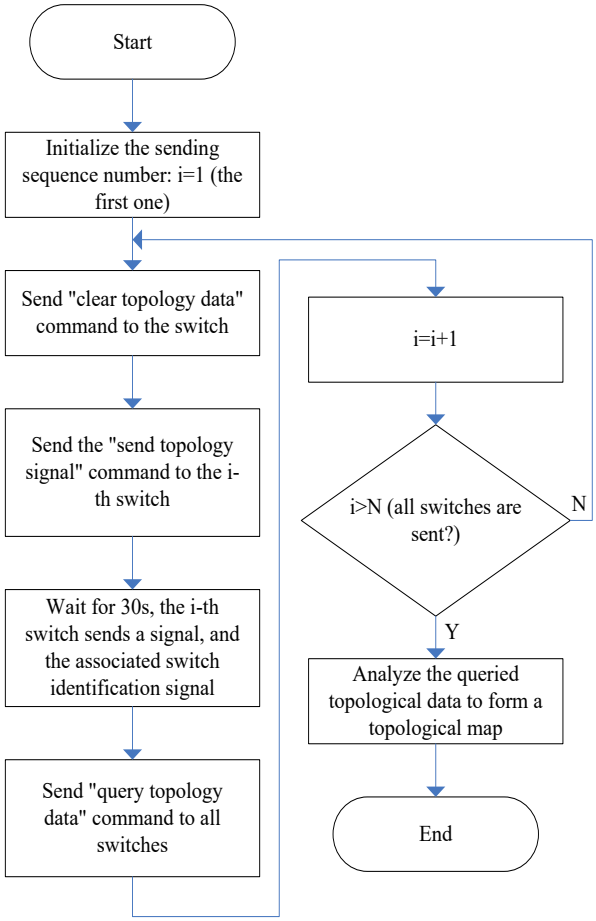

Figure 7. Topology identification process.

3.4. Encoding

Table 1 shows the definition of the coding mode of the topology identification unit. The data frame format is composed of six parts: the data synchronization header, start bit, data bit, insert bit, parity bit and end bit. Among them, the data synchronization header is a 6-bit '1', which means that there is no current time of more than 360 ms; the start bit is a 1-bit '0'. The data bit includes a feature code and a check code, and the feature code consists of 24 bits. The code has 16 bits, with 1 insert bit being inserted every 4 bits, and the insert bit is opposite to the previous data bit. The check bit is 10 bits in total, with 1 insert bit being inserted every 4 bits, and the insert bit is opposite to the previous data bit. The end bit is 1, which consists of the bit '0'.

Table 1. Definition of Topology Identification Unit Coding Method.

Project		Coding Method Definition
Data frame format		Data sync header + start bit + data bit + insert bit + parity bit + end bit
Data sync header		6 digits '1' (i.e., no current time lasting for more than 360 ms)
Start bit		1 bit '0'
Data	Signature	A total of 24 bits, with 1 insertion bit inserted every 4 bits. A total of 30 bits; the inserted bit is opposite to the previous data bit.
	Check code	A total of 16 bits, with an insertion bit inserted every 4 bits. A total of 20 bits; the inserted bit is opposite to the previous data bit.
Check (message authentication code)		A total of 8 bits, with 1 insert bit inserted every 4 bits. A total of 10 bits; the inserted bit is opposite to the previous data bit.
End bit		1-bit '0'

3.5. Communication Protocol Stack Structure

The communication network protocol stack of the topology identification unit is shown in Figure 8. The communication protocol stack has a three-layer structure, which mainly includes a physical layer, a data link layer and an application layer.

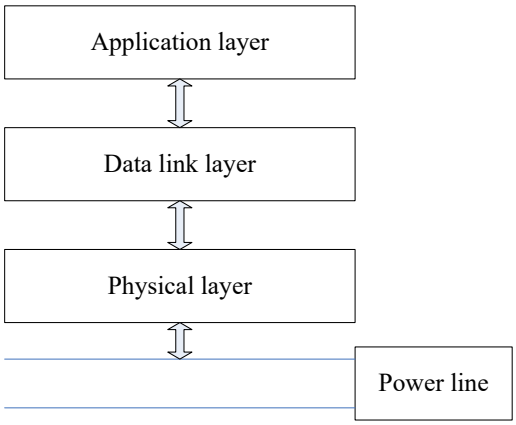

Figure 8. Communication network protocol stack definition.

When the business data are transmitted, they need to be encapsulated according to Figure 9, and they are finally transmitted through the power line. The data message received by the physical layer through the power line is encapsulated in the process of submitting it to the application layer.

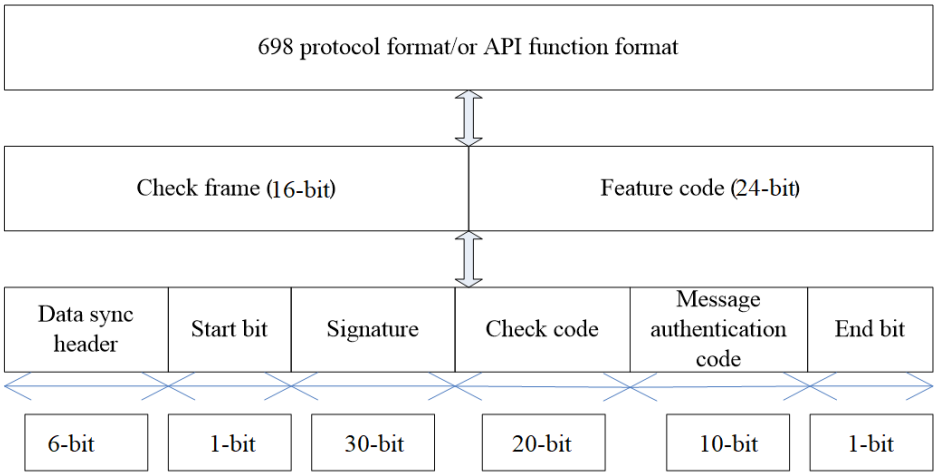

Figure 9. Packet encapsulation format.

The actual data length transmitted on the physical layer is 68-bit, and the maximum length of the physical layer decoding unit is 76-bit. The transmission data can then be decoded all at once. The message authentication code adopts CRC8 check, and the polynomial that is used is X8 + X2 + X + 1.

4. Design of the Intelligent Measurement Switch

4.1. Design of the Power Supply

The principle for the power supply module is shown in Figure 10. The 5 V power supply circuit mainly adopts an LM78L05-type power supply chip, and the 3.3 V power supply circuit mainly adopts an HT7533-1-type power supply chip. After rectification, the power VCC is filtered by capacitors C2 and C3. It inputs to the VR1 chip, and the VR1 chip outputs +5 V of power. The +5 V power supply is filtered through the grounding of

capacitors C4 and C5 and through D1 voltage regulator protection, and then it inputs to the VR2 power chip, which outputs +3.3 V of power that is filtered by capacitors C6 and C7.

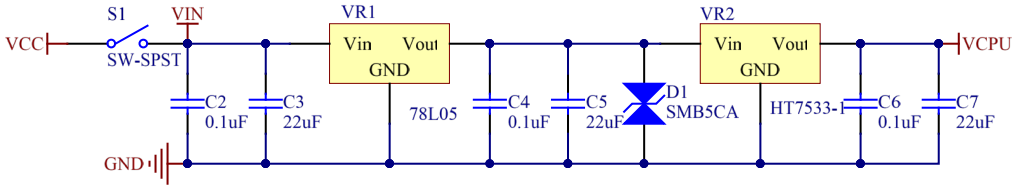

Figure 10. Power module circuit diagram.

4.2. Design of Current Sampling

The principle of current sampling and CT power extraction is shown in Figure 11. The current sampling circuit is used to accurately sample the line current. The external input current signal of the secondary side of the three-way current transformer is converted into a voltage signal by the sampling resistor, rectified by the rectifier bridge (D12, D13 and D14), which is then filtered by the respective RC circuits (R37, R39 and C29 as a group; R41, R44 and C30 as a group; and R47, R50 and C31 as a group). Then, it is amplified by the op-amp constituted by the voltage conversion signal, which is sampled and uploaded to the main control unit.

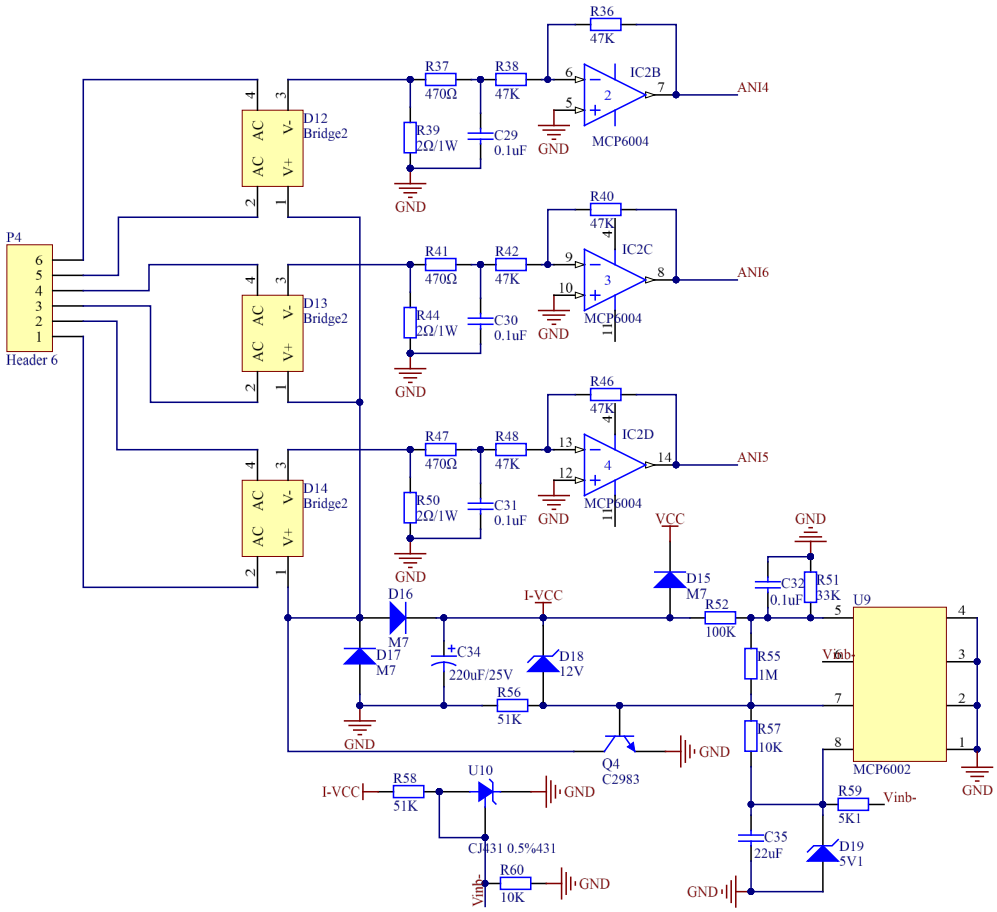

Figure 11. Current sampling and CT power circuit diagram.

The CT pickup circuit is used to provide DC power for the control section (including the main control module, communication module, etc.) in combination with the power supply module when the voltage pickup is abnormal. The current is charged by a D16 half-wave rectifier for electrolytic capacitor C34, which is used as the energy storage element for CT power take-off at 1-VCC. Voltage regulator diode D18 plays the role of protecting the

line from over-voltage. U10 is a voltage regulator triode, which can output a high-precision 2.495 V voltage to stabilize the Vinb- pin of U9 at 2.495 V. U9 acts as a voltage comparator when the Vinb+ voltage is greater than Vinb-, the open high-level output Q4 transistor, so the current flows directly to GND, no longer charging the capacitor. Therefore, 1-VCC voltage can output a stable voltage of 2.495 × (1 + 100 K/33 K) = 10.06 V.

4.3. Design of Functions and Interfaces

The major function of an intelligent measurement switch can be summarized as follows.

(1) HPLC meter reading communication: Data transmission in low-voltage power lines is used in the meter network for data communication and meter reading with meters and concentrators.
(2) Feature current transmitting: A frequency-adjustable current amplitude of 0.38–0.45 A is sent using a constant current load with the support of recording the last ~ten sent records, including the sent start time and end time. The number of local storage records should be no less than 10.
(3) Topology identification: With the characteristic current receiving function, the sampling frequency of the receiving module's current signal is not less than 4 kHz. Identification equipment should support the record storage of the relevant information of the received signal, including the receiving time of the signal's identification, the phase to which the characteristic current belongs, the current size and signal noise, etc. The amount of signal information for storage is not less than 2000 while supporting the reading of historical records, and stored information is not lost when power is lost.

The main technical parameters of the circuit breaker branch identification module are shown in Table 2. The interface-labelling diagram of HPLC topology module for the measurement switch is shown in Figure 12. The main interface's definition and a description of the HPLC topology module for the designed intelligent measurement switch are listed in Table 3.

Table 2. Main technical parameters.

HPLC operating frequency band	2~12 M, 2.5~5.7 M, 0.7~3 M, 1.7~3 MHz
Serial communication rate	1200 bps, 2400 bps, 4800 bps, 9600 bps
Operating frequency	50 Hz (45–55 Hz)
Operating voltage AC	220 VAC (176~264 V)
Operating voltage DC	Analog power supply for communication modules, provided by the base board voltage range; 12 ± 1 V
Operating temperature	−40 °C~+85 °C
Relative humidity	≤75%
Communication tange	Entire distribution substation area
Damp heat	55 °C/90% R.H
Characteristic current emitting Circuit devices: temperature rise	≤70 °C
Add a 100 Ω resistor to the whole board	Temperature rise ≤55 °C

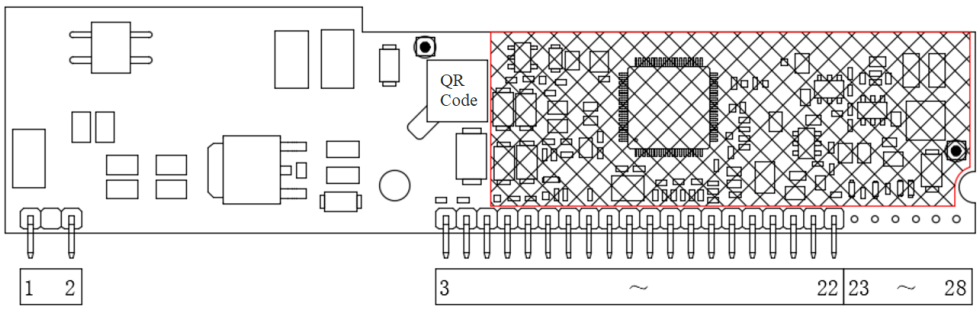

Figure 12. Interface labeling diagram of HPLC topology module for measurement switch.

Table 3. Main interface definition and description of HPLC topology module for measurement switch.

Pin	Input/Output	PIN	Description
1	\	N	220 V zero wire
2	\	L	220 V fire wire
3	\	HPLC_N	HPLC differential coupling signal (coupling transformer required)
4	\	HPLC_P	HPLC differential coupling signal (coupling transformer required)
5	GND	GND	Power ground
6	O	TXD_MCU	TXD serial port for communication with circuit breaker master (for module definition)
7	I	RXD_MCU	Communication with circuit breaker master serial port RXD (for module definition)
8	I/O	GPIO24	GPIO24 port (reserved)
9	I	ZC_A	A-phase over-zero signal input
10	I	EVENT	Event up, active high, need to connect pull-down 10 K resistor
11	I	RST	Module resets the signal input; low-level reset
12	I	IA+	A-phase current transformer positive input ±0.4 V
13	I	IA−	A-phase current transformer negative input ±0.4 V
14	I	IB+	B-phase current transformer positive input ±0.4 V
15	I	IB−	B-phase current transformer negative input ±0.4 V
16	I	IC+	C-phase current transformer positive input ±0.4 V
17	I	IC−	C-phase current transformer negative input ±0.4 V
18	ADC/I/O	ADC3_CH2/PM_GPIO13	ADC3_CH2/PM_GPIO13 (reserved)
19	PWR	3.3 V_OUT	Reserved for external 3.3 V (supercapacitor charging) %; it is recommended to use the bottom 3.3 V to charge the supercapacitor
20	I	12 V_ADC	12 V power-down detection signal input
21	PWR	12 V	Module DC power supply interface; input range of 12 ± 1 V, ripple 2%
22	GND	GND	Power Ground

5. Experiment and Effect Analysis

To verify the proposed topology identification technology and the designed intelligent measurement switch (IMS), we selected nine measurement switches with the topology identification function in the network, whose numbers are as follows: ①, ②, ③, ④, ⑤, ⑥, ⑦, ⑧ and ⑨. In addition, we built the experimental platform in the laboratory environment, as shown in Figure 13. The topology data table obtained through the topology identification process is shown in Table 4.

Table 4. Topology Data Sheet.

Switch to Send Topological Signal	Switches That Recognize Topological Signals	Level
①	① ⑤	2
②	② ⑤ ⑨	3
③	③ ⑤	2
④	① ④ ⑤ ⑥	4
⑤	⑤	1
⑥	① ⑤ ⑥	3
⑦	③ ⑤ ⑦	3
⑧	① ⑤ ⑧	3
⑨	⑤ ⑨	2

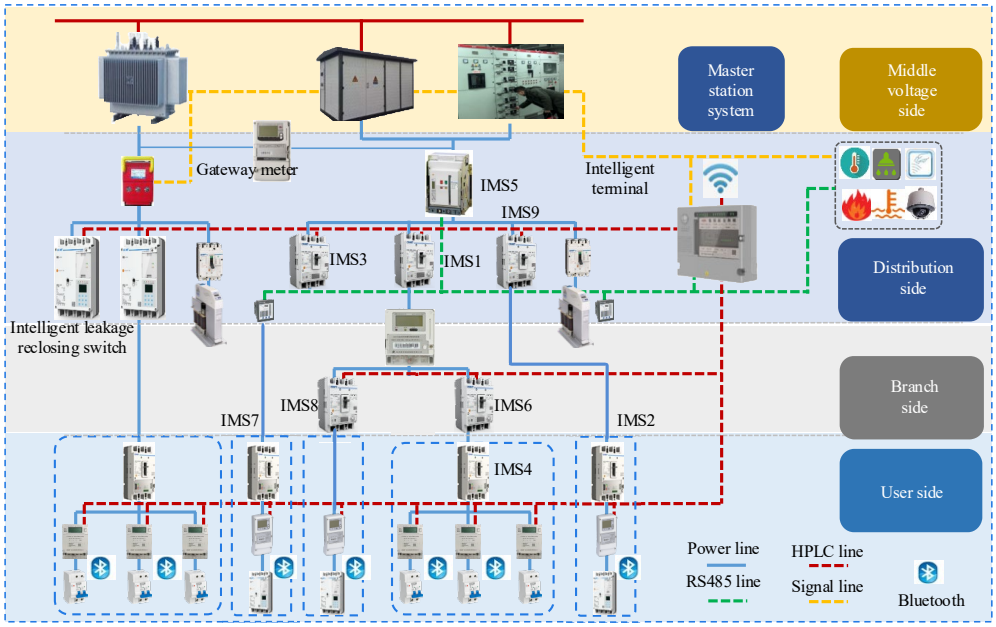

Figure 13. Topology test platform (IMS1 represents intelligent measurement switch ①).

Figures 14–16 show characteristic current values of 1–3 with practical test waveforms. The test results of the intelligent measurement switch are provided in Table 5.

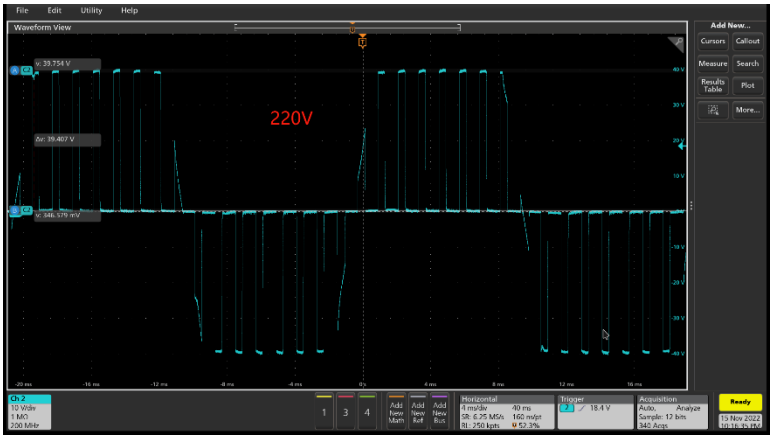

Figure 14. Characteristic current value 1 of practical test waveform.

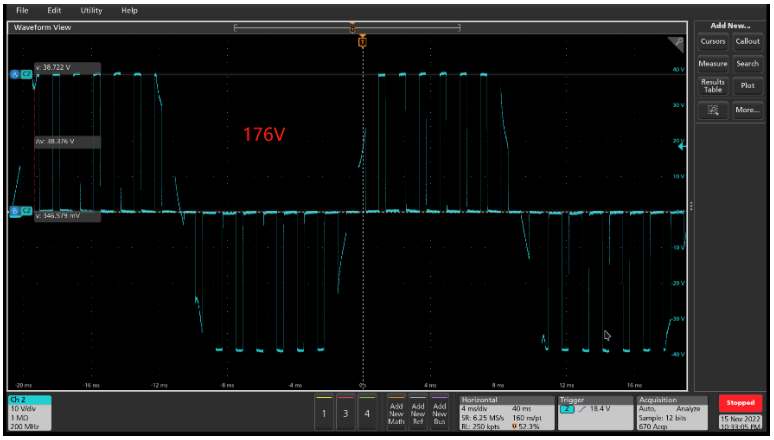

Figure 15. Characteristic current value 2 of practical test waveform.

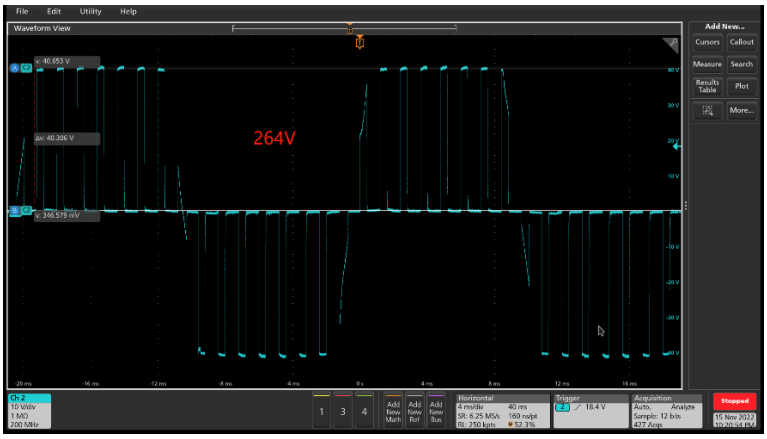

Figure 16. Characteristic current value 3 of practical test waveform.

Table 5. Test results of intelligent measurement switches.

No.	Major Test Items	Test Sub-Item	Center Frequency	Characteristic Code	Test Results
1	Sending device current signal characteristics detection	220 V_50.5 Hz Topology identification detection	833.33 Hz	AAE9	pass
			625 Hz	AAEA	pass
			666.66 Hz	AAE5	pass
			1333.33 Hz	AAE3	pass
		264 V _ 50 Hz Topology identification detection	833.33 Hz	AAE9	pass
			625 Hz	AAEA	pass
			666.66 Hz	AAE5	pass
			1333.33 Hz	AAE3	pass
		176 V _ 50 Hz Topology identification detection	833.33 Hz	AAE9	pass
			625 Hz	AAEA	pass
			666.66 Hz	AAE5	pass
			1333.33 Hz	AAE3	pass
		220 V _ 50.5 Hz Topology identification detection	833.33 Hz	AAE9	pass
			625 Hz	AAEA	pass
			666.66 Hz	AAE5	pass
			1333.33 Hz	AAE3	pass
		220 V _ 49.5 Hz Topology identification detection	833.33 Hz	AAE9	pass
			625 Hz	AAEA	pass
			666.66 Hz	AAE5	pass
			1333.33 Hz	AAE3	pass
2	Identification device identification function detection	220 V _ 50 Hz	833.33 Hz, AAE5 (Noiseless)	AAE5	pass
		220 V _ 50.5 Hz	833.33 Hz, AAE9 (Noise1)	AAE9	pass
		176 V _ 19.5 Hz	625 Hz, AAEA (Noiseless)	AAEA	pass
3	Identification equipment anti-interference capability testing	220 V _ 50 Hz	Noise2	AAE9	pass
		220 V _ 50 Hz	Noise3	AAE9	pass
		220 V _ 50 Hz	Noise4	AAE9	pass
4	Sending device reliability	220 V _ 50 Hz	833.33 Hz Continuous test 20 times under	AAE9	pass
		264 V _ 50 Hz	833.33 Hz Continuous test 20 times under	AAE9	pass
		176 V _ 50 Hz	833.33 Hz Continuous test 20 times under	AAE9	pass
		220 V _ 50.5 Hz	833.33 Hz Continuous test 20 times under	AAE9	pass
		220 V _ 49.5 Hz	833.33 Hz Continuous test 20 times under	AAE9	pass

By utilizing the principle by which the switch itself and its superior switch can detect a topological signal, a topological structure was obtained with the proposed technique, as shown in Figure 17.

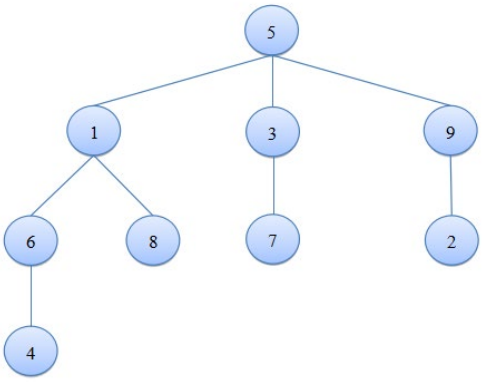

Figure 17. Topological structure obtained with proposed technique. (1~9 means nine measurement switches).

The terminal sends out identification signals sequentially through the communication module. Taking switch ④ as an example, the terminal requires switch ④ to generate a pulse current signal. Switches ⑥, ① and ⑤ can detect the pulse current signal and inform the terminal, and the terminal is able to determine that switches ⑥, ① and ⑤ are the upper nodes of switch ④. When switch ⑥ sends out the pulse current signal, and switches ① and ⑤ can detect the pulse current signal and inform the terminal. The terminal is able to determine that switches ① and ⑤ are the upper nodes of switch ⑥. When switch ① sends out the pulse current signal, only switch ⑤ can detect the pulse current signal, and the terminal is able to judge that switch ⑤ is the upper node of switch ①. The terminal thinks that the hierarchy of the topology is ④→⑥→①→⑤→Smart terminal.

During the experiment, the overall topology identification time was 96 s, and the topology identification accuracy rate was 100%. The results are good because the under-test topology, as shown in Figure 17, is not very complex. Because the under-test topology was built in the laboratory, the number of branches and devices (smart meters) was limited. It should be noticed that, in most practical applications, the accuracy is below 100% because the practical topology is more complex than that of the test.

Table 6 shows the topology identification results from using the distribution network [10], the topology signal exchange information [11] and our method. From Table 6, it can be seen that all three adapted methods can achieve topology identification with 100% accuracy. It should be noticed that the proposed method requires the smallest overhead time.

Table 6. Comparison of identification results.

Method	Number of Levels	Rate of Identification	Overhead Time
Distribution Network [10]	4	100%	12 min
Topology signal exchange information [11]	4	100%	13 min
Our method	4	100%	9 min

The experimental results show that, in the test environment, the topology structure diagram and the topology data table formed by the technology in this paper are accurate and reliable, and the topology identification time is short. It can clearly show the relationship between switches at all levels, and it provides a technical approach in order to accurately locate the fault point and identify the fault type.

6. Conclusions

In view of the defects of existing technology, such as low availability and inconsistencies between a system's topology and the actual topology, this paper proposes a technical solution for topology identification based on intelligent measurement switches, and the topology identification mechanism based on the characteristic current is built. The modulation and demodulation process and the modulation method are designed. The design is clear, and the current characteristics and key parameters of the topology identification are clarified. A complete topology identification process is proposed, the information encoding method and data frame format are given and the communication network protocol's stack structure as well as the message encapsulation format of the topology identification unit are designed. Experimental verification and analysis show that the technical solution proposed in this paper has a short topology identification time, low power consumption and an identification accuracy of 100%. It can effectively solve the defects of existing technology and can be widely promoted and applied in low-voltage distribution networks, so the prospect is very broad.

Author Contributions: Conceptualization, D.X.; Data curation, D.X.; Formal analysis, D.X.; Funding acquisition, D.X.; Investigation, D.X.; Methodology, D.X.; Project administration, D.X.; Resources, D.X.; Software, D.X.; Validation, D.X.; Supervision, J.D.; Writing—original draft, J.D.; Writing—review & editing, J.D. All authors have read and agreed to the published version of the manuscript.

Funding: This research was funded by National Key R & D Program grant number 2022YFF0607700.

Data Availability Statement: Since the study did not report any data, the authors chose to exclude this statement.

Conflicts of Interest: The authors declare no conflict of interest.

References

1. Liu, Y.L.; Jin, T.; Mohamed, M.A.; Wang, Q.J. A novel three-step classification approach based on time-dependent spectral features for complex power quality disturbances. *IEEE Transact. Instrum. Meas.* **2021**, *70*, 3000814. [CrossRef]
2. Song, J.; Zhang, J.; Wen, H. Accurate dynamic phasor estimation by matrix pencil and Taylor weighted least squares method. *IEEE Transact. Instrum. Meas.* **2021**, *70*, 9002211. [CrossRef]
3. Liu, Z.P.; Li, W.K.; Cheng, S.P. Control strategy and design of grid-connected microinverter based on interleaved flyback structure. *China Meas. Test* **2015**, *41*, 73–77+92.
4. Lin, X.F.; Yu, J.R.; Yu, R.X.; Zhang, J.; Yan, Z.Z.; Wen, H. Improving small-signal stability of grid-connected inverter under weak grid by decoupling phase-lock loop and grid impedance. *IEEE Transact. Ind. Electron.* **2022**, *69*, 7040–7053. [CrossRef]
5. Yang, J.X.; Xin, M.Y.; Ou, J.X.; Wang, J.R.; Song, Q. Distribution network line loss location and evaluation method study based on big data. *China Meas. Test* **2019**, *45*, 19–24.
6. Yan, Z.Z.; Wen, H. Electricity theft detection base on extreme gradient boosting in AMI. *IEEE Transact. Instrum. Meas.* **2021**, *70*, 2504909. [CrossRef]
7. Li, Y.; Liu, H.; Li, Z. Topology identification and inner desynchronization of Hindmarsh-Rose neural network. In Proceedings of the 2020 Chinese Control and Decision Conference (CCDC), Hefei, China, 1 August 2020; pp. 1642–1646.
8. Chen, Y.; Chen, J.; Jiao, H.; Guo, Y.; Jiang, W.; Tang, H. Two-stage topology identification method for distribution network via clustering correction. In Proceedings of the 2019 IEEE Innovative Smart Grid Technologies—(ISGT Asia), Chengdu, China, 1 May 2019; pp. 280–284.
9. Shen, Y.; Fu, X.; Giannakis, G.B.; Sidiropoulos, N.D. Topology identification of directed graphs via joint diagonalization of correlation matrices. *IEEE Transact. Signal Inf. Process. Over Netw.* **2020**, *6*, 271–283. [CrossRef]
10. Li, S.; Gao, S.; Wu, J.; Xie, D.; Qi, L. Research on topology identification of distribution network under the background of big data. In Proceedings of the 2020 IEEE 4th Conference on Energy Internet and Energy System Integration (EI2), Wuhan, China, 30 October 2020; pp. 4294–4297.
11. Xu, C.; Lei, Y.; Zou, Y. A method of low voltage topology identification. In Proceedings of the 2020 IEEE Conference on Telecommunications, Optics and Computer Science (TOCS), Shenyang, China, 11 December 2020; pp. 318–323.
12. Chen, Y.; Jiang, T.; Lai, F. Automatic topology generation of 21 bit chipless radio frequency identification tags using a noniterative technique. *IEEE Antennas Wirel. Propag. Lett.* **2019**, *18*, 293–297. [CrossRef]
13. Liu, Y.; Sun, J.; Chen, Q.; Xia, M. Distribution network topology error identification method based on D-PMU and branch state function. In Proceedings of the 2019 IEEE Innovative Smart Grid Technologies—Asia (ISGT Asia), Chengdu, China, 1 May 2019; pp. 821–826.

14. Xiang, Z.; Huang, K.; Deng, W.; Yang, C. Blind topology identification for smart grid based on dictionary learning. In Proceedings of the 2019 IEEE Symposium Series on Computational Intelligence (SSCI), Xiamen, China, 20 February 2020; pp. 1319–1326.
15. Deng, W.; Zhang, Z.; Duan, J.; Qiao, X.; Zhu, L.; Li, Y. Improved topology identification algorithm of distribution network mutual information. In Proceedings of the 2019 IEEE Sustainable Power and Energy Conference (iSPEC), Beijing, China, 1 November 2019; pp. 1791–1795.
16. Van Waarde, H.J.; Tesi, P.; Camlibel, M.K. Topology identification of heterogeneous networks of linear systems. In Proceedings of the 2019 IEEE 58th Conference on Decision and Control (CDC), Nice, France, 1 December 2019; pp. 5513–5518.
17. Farajollahi, M.; Shahsavari, A.; Mohsenian-Rad, H. Topology identification in distribution systems using line current sensors: An MILP approach. *IEEE Transact. Smart Grid* **2020**, *11*, 1159–1170. [CrossRef]
18. Wang, Y.; Wu, X.; Lü, J.; Lu, J.; D'Souza, R.M. Topology identification in two-layer complex dynamical networks. *IEEE Transact. Netw. Sci. Eng.* **2020**, *7*, 538–548. [CrossRef]
19. Coutino, M.; Isufi, E.; Maehara, T.; Leus, G. State-space network topology identification from partial observations. *IEEE Transact. Signal Inf. Process. Over Netw.* **2020**, *6*, 211–225. [CrossRef]
20. Zhao, J.; Li, L.; Xu, Z.; Wang, X.; Wang, H.; Shao, X. Full-scale distribution system topology identification using Markov random field. *IEEE Transact. Smart Grid* **2020**, *11*, 4714–4726. [CrossRef]
21. Cavraro, G.; Bernstein, A. Bus clustering for distribution grid topology identification. *IEEE Transact. Smart Grid* **2020**, *11*, 4080–4089. [CrossRef]