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Analysis of DC-Side Snubbers for SiC Devices Application

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Abstract: Due to parasitic parameters existing in Silicon Carbide (SiC) devices application, SiC devices have poor turn-off performances. SiC diode and SiC MOSFET have severe turn-off overvoltage and oscillation. The DC-side snubber is one simple suppressing method. The simplest circuit is the high-frequency decoupling capacitor in parallel with the bridge leg. However, choosing the component value is empirical. Based on the turn-off terminal impedances of the SiC diode and the SiC MOSFET, the suppressing mechanism of this DC-side snubber is analyzed. The guideline selection for the component value is provided. Furthermore, the DC-side snubber with a damping resistor is analyzed based on the terminal impedances. The design principles are provided. Finally, the validity and effectiveness of the DC-side snubbers were proven based on the double-pulse test platform.

Keywords: SiC MOSFET; turn-off overvoltage; oscillation; DC-side snubber

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1. Introduction

In recent years, Silicon Carbide (SiC) devices have emerged as a kind of promising candidates for high-performance power conversion [1,2]. Compared with state-of-the-art silicon devices, they are featured with higher switching speeds and lower switching loss [3,4]. Therefore, the switching frequency of the power electronic equipment with SiC devices has been continuously pushed up to reduce the size of passive components, which realizes the high-power density [5,6]. However, due to parasitic parameters existing in SiC devices application, SiC devices have poor turn-off performances [7]. SiC diode and SiC MOSFET will have severe turn-off overvoltage and oscillation [8,9]. To avoid damaging the devices, the voltage rating must be enough, which will increase the system cost [10–12].

The turn-off terminal impedance is used to analyze the mechanism of the turn-off voltage and oscillation of the SiC MOSFET [13,14]. The parasitic capacitors of the SiC MOSFET and the loop parasitic inductors resonate, which amplifies the component of the excitation source and results in the turn-off overvoltage and oscillation [15,16]. The turn-off terminal impedance analysis method can be performed to provide the suppressing guidelines.

The suppressing methods for the turn-off overvoltage and oscillation on devices can be classified into two categories. One method is to reduce the switching speed of devices, which can be implemented by increasing the gate resistor. However, poor switching performances will be attained, including the switching delay time and the switching loss [17,18]. Another method is to add snubbers to the circuit. One type of snubber is connected directly to the devices, such as the R¬–C snubber [19,20] and the R–C–D snubber [21,22]. By these device snubbers, the turn-off overvoltage can be decreased, but the turn-on overcurrent and the loss can be increased. Furthermore, the suppressing effectiveness can be weakened by the added parasitic inductors owning to device snubbers. Therefore, device snubbers are used less in high-speed SiC devices application. Another type of snubber is the DC-side snubber, which is one simple suppressing method. The simplest circuit is the high-frequency decoupling capacitor in parallel with the bridge leg [23]. By DC-side snubbers, a portion of parasitic inductors can be decoupled from the switching power loop. However, choosing the component value is empirical. Moreover, the suppressing effectiveness is not good when the bulk of the decoupling capacitor leads

large parasitic inductors to the switching power loop. In a silicon IGBT application, a damping resistor is in series with the high-frequency decoupling capacitor to suppress the turn-off overvoltage [24]. However, the effectiveness will be decreased if parameters are not designed appropriately. Another DC-side snubber in [25] is the high-frequency decoupling capacitor in parallel with the capacitor-damping-resistor branch. The capacitor-damping-resistor branch is used to suppress the low-frequency oscillation on the turn-off voltage. Nevertheless, the low-frequency oscillation cannot be fully eliminated.

Based on previous considerations, this paper aims to design an effective DC-side snubber to suppress the turn-off overvoltage and oscillation for SiC devices application. One contribution from this paper is that the turn-off terminal impedances of the SiC diode and the SiC MOSFET were deduced. By these turn-off terminal impedances, the suppressing mechanisms and design principles of DC-side snubbers can be investigated. Another contribution of this paper is the guideline design for the DC-side snubbers is presented, which can provide the theoretical, not the empirical, design.

The rest of this paper is organized as follows. First, the suppressing mechanism of the simplest DC-side snubber is discussed in detail. Then, the DC-side snubber with the damping resistor is analyzed. Finally, the validity and effectiveness of the DC-side snubbers are verified by experimental results.

2. Suppressing Mechanism of DC-Side Snubber C_{DE}

In a phase-leg configuration, such as boost, buck-boost, half-bridge, and full-bridge, the active switch makes current communication with the freewheeling diode during the turn-on and turn-off transition of the active switch. The basic cell is shown in Figure 1, with one branch being the output current, I_o, one branch being the freewheeling diode, and one branch being the active switch, which was chosen to study. The input voltage source, V_{DC}, is constant. The output current, I_o, is constant. C_{DC} is the DC bulk capacitor. C_{DE} is the DC-side snubber capacitor. The switch, Q, is driven by the double pulse signal. The switching of Q causes current commutation with the external circuit and the diode, D. However, the parasitic elements existing in the circuit need to be considered due to the high-speed switching SiC MOSFET. The parasitic elements in Figure 1 are the gate–source capacitance (C_{GS}), the gate–drain capacitance (C_{GD}), the drain–source capacitance (C_{DS}), the gate inductance (L_G), the drain inductance (L_D), the source inductance (L_S) of the Q and the junction capacitance (C_F), the cathode inductance (L_{C1}), and the anode inductance (L_{A1}) of the diode (D). A SiC diode is employed as the freewheeling diode, which does not have the reverse recovery charge (Q_{rr}) and has a low voltage drop. L'_{bus1}, L'_{bus2}, L''_{bus1}, and L''_{bus2} represent the interconnection parasitic inductors of the PCB traces. L_{CS} are the common source inductances shared by the switching power loop and the gate drive loop. R_G represents the external gate drive resistance. v_P is the gate signal for the SiC MOSFET.

The turn-on switching transition of the SiC MOSFET can be divided into four stages [26], which are the Turn-on Delay Time (Stage 1: t_1–t_2), Current Rising Time (Stage 2: t_2–t_3), Voltage Falling Time (Stage 3: t_3–t_4), and Gate Remaining Charging Time (Stage 4: t_4–t_5). The turn-off switching transition of the SiC MOSFET can be divided into four stages [26], which are the Turn-off Delay Time (Stage 5: t_5–t_6), Voltage Rising Time (Stage 6: t_6–t_7), Current Falling Time (Stage 7: t_7–t_8), and Gate Remaining Discharging Time (Stage 8: t_8–t_9). Figure 2 shows the switching waveforms of the SiC diode and the SiC MOSFET. During Stage 4, the turn-off overvoltage and oscillation of the SiC diode occur. During Stage 7 and Stage 8, the turn-off overvoltage and oscillation of the SiC MOSFET occur.

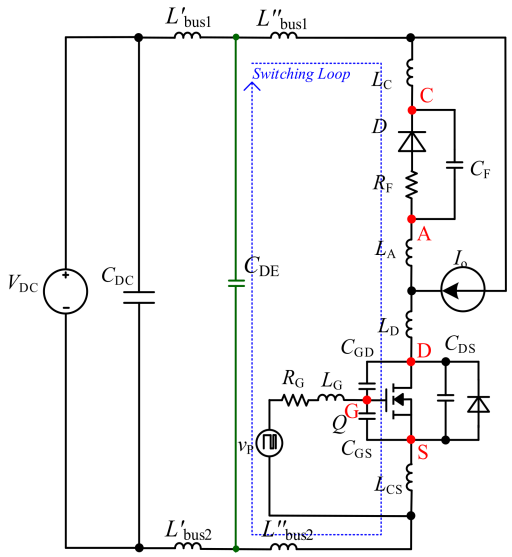


Figure 1. Phase-leg configuration with DC-side Snubber C_{DE}.

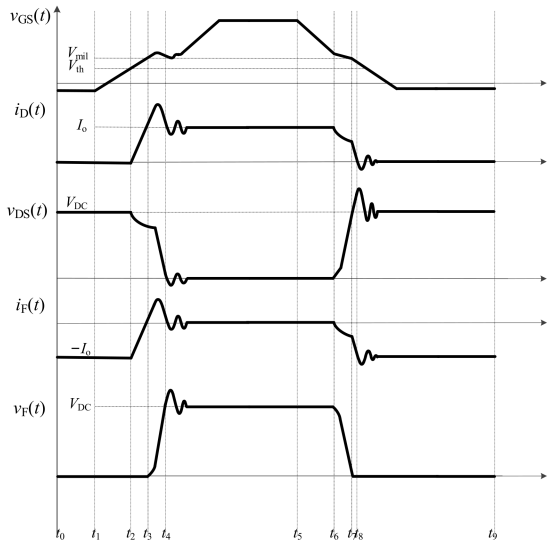


Figure 2. Switching waveforms during the turn-on and turn-off transitions of the SiC MOSFET.

2.1. Analysis of Stage 4

At t_4, the voltage of the SiC diode, v_F, reaches the input voltage, V_{DC}. Then the turn-off overvoltage and oscillation on the SiC diode occurs. In this stage, the SiC MOSFET is equivalent to the on-state resistor (R_{DS_on}). Figure 3a shows the equivalent circuit at this stage, in which L'_P is the sum of L_C, L_A, L_D, L_{CS}, L''_{bus1}, and L''_{bus2}. L'_{bus} is the sum of L'_{bus1} and L'_{bus2}. The parasitic capacitors of the SiC MOSFET are neglected because the SiC MOSFET is in the on-state. The terminal impedance Z_{d_1} is calculated as Equation (1), as the following,

$$Z_{d\_1}(s) = \frac{N_{d\_1}(s)}{D_{d\_1}(s)}, \tag{1}$$

where $N_{d\_1}(s)$ and $D_{d\_1}(s)$ are shown in Appendix A. The amplitude–frequency curves of the terminal impedance Z_{d_1} are shown in Figure 4a, based on the parameters in Table 1. To be consistent with the experimental verification in Section 4, parameters of the SiC MOSFET C2M0080120D and the SiC diode C4D20120A were used. Based on Figure 4a, there are

two resonant peaks existing on the terminal impedance Z_{d_1}. The resonant frequencies are expressed as Equations (2) and (3),

$$f_{d\_1\_1} \approx \frac{1}{2\pi\sqrt{L'_P\left(\frac{C_{DE}C_F}{C_{DE}+C_F}\right)}}, \tag{2}$$

$$f_{d\_1\_2} \approx \frac{1}{2\pi\sqrt{L'_{bus}(C_{DE}+C_F)}}, \tag{3}$$

where $f_{d\_1\_1}$ represents the high-resonance frequency of the terminal impedance Z_{d_1}, and $f_{d\_1\_2}$ represents the low-resonance frequency of the terminal impedance Z_{d_1}. The peak resonant impedances of the terminal impedance Z_{d_1} amplify the excitation source at the resonant frequencies and result in two oscillations overlaying on the turn-off voltage of the SiC diode.

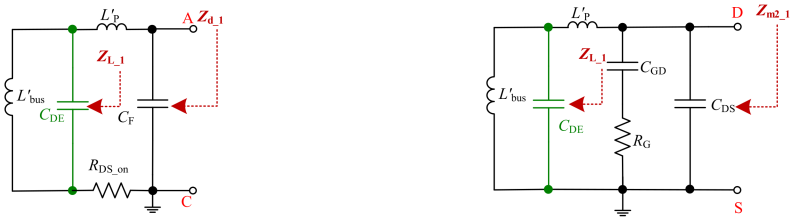


Figure 3. Equivalent circuit with capacitor C_{DE} (**a**) at Stage 4 and (**b**) at Stage 7 and Stage 8.

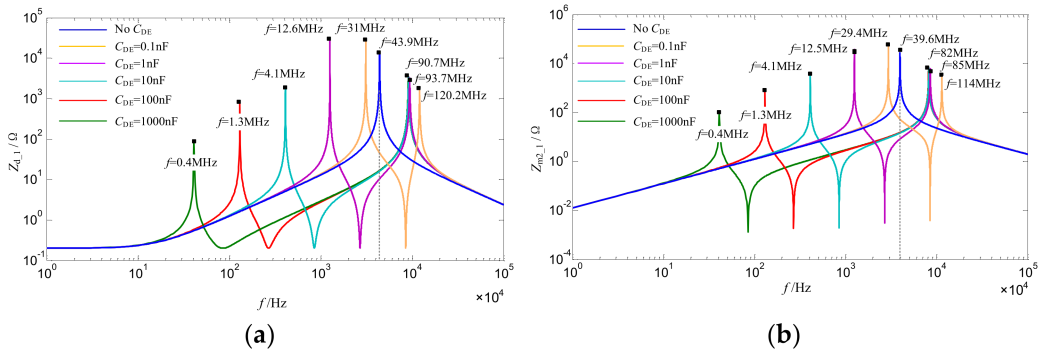


Figure 4. Amplitude–frequency curves of the terminal impedances, Z_{d_1} and Z_{m2_1}, with different C_{DE} (**a**) at Stage 4 and (**b**) at Stage 7 and Stage 8.

Table 1. Parameters for drawing the amplitude–frequency curve.

Parameter	Value	Parameter	Value
R_{DS_on}	0.2 Ω	L'_P	50 nH
C_{GD}	7.6 pF	L'_{bus}	150 nH
C_{DS}	75 pF	R_G	15 Ω
C_F	67 pF		

2.2. Analysis of Stage 7 and Stage 8

At t_7, the SiC diode and the SiC MOSFET make a current commutation, and the turn-off overvoltage of the SiC MOSFET occurs. At t_8, the current commutation comes to an end, and the oscillation on the turn-off voltage of the SiC MOSFET occurs. Figure 3b shows the equivalent circuit at these two stages. The capacitor of the SiC diode is neglected

because the SiC diode is in the on-state. The terminal impedance Z_{m2_1} is calculated as Equation (4),

$$Z_{m2\_1}(s) = \frac{N_{m2\_1}(s)}{D_{m2\_1}(s)}, \tag{4}$$

where $N_{m2\_1}(s)$ and $D_{m2\_1}(s)$ are shown in Appendix A. The amplitude–frequency curves of the terminal impedance, Z_{m2_1}, are based on the parameters in Table 1, as shown in Figure 4b. In Figure 4b, there are two resonant peaks existing on the terminal impedance Z_{m2_1}, which is the same as the terminal impedance Z_{d_1}. The resonant frequencies are expressed as Equations (2) and (3),

$$f_{m2\_1\_1} \approx \frac{1}{2\pi\sqrt{L'_P\left(\frac{C_{DE}C_{oss}}{C_{DE}+C_{oss}}\right)}}, \tag{5}$$

$$f_{m2\_1\_2} \approx \frac{1}{2\pi\sqrt{L'_{bus}(C_{DE}+C_{oss})}}, \tag{6}$$

where $f_{m2\_1\_1}$ represents the high-resonance frequency of the terminal impedance Z_{m2_1} and $f_{m2\_1\_2}$ represents the low-resonance frequency of the terminal impedance Z_{m2_1}, and $C_{oss} = C_{GD} + C_{DS}$. The peak resonant impedances of the terminal impedance Z_{m2_1} amplify the excitation source at the resonant frequencies and result in two oscillations overlaying on the turn-off voltage of the SiC MOSFET.

2.3. Guideline Selection for Capacitor C_{DE}

To realize the decouple of the inductor L'_{bus} from the switching power loop and make inductor L'_{bus} and parasitic capacitors C_F, C_{GD}, and C_{DS} no resonance, capacitor C_{DE} must be much larger than the parasitic capacitors C_F, C_{GD}, and C_{DS} according to Equations (1)–(6). In addition, the impedance Z_{L_1} of the paralleling branches L'_{bus} and C_{DE} at the high-resonance frequency $f_{d1\_1\_1}$ and the high-resonance frequency $f_{m2\_1\_1}$ should be much lower than the impedance of inductor L'_P. In general, the capacitor C_{DE} satisfies the inequality in Equation (7). It is considered that capacitor C_{DE} is large enough than parasitic capacitors C_F, C_{GD}, and C_{DS}.

$$C_{DE} \geq \max(100C_{oss}, 100C_F). \tag{7}$$

The impedance Z_{L_1} of the paralleling branches L'_{bus} and C_{DE} can be expressed as Equation (8). In addition, Equation (9) should be satisfied and simplified as Equation (10).

$$Z_{L\_1}(s) = \frac{L'_{bus}s}{C_{DE}L'_{bus}s^2+1}. \tag{8}$$

$$\begin{cases} \left|j2\pi f_{d\_1\_1}L'_P\right| \gg \left|\frac{j2\pi f_{d\_1\_1}L'_{bus}}{(j2\pi f_{d\_1\_1})^2C_{DE}L'_{bus}+1}\right| \\ \left|j2\pi f_{m2\_1\_1}L'_P\right| \gg \left|\frac{j2\pi f_{m2\_1\_1}L'_{bus}}{(j2\pi f_{m2\_1\_1})^2C_{DE}L'_{bus}+1}\right| \end{cases}. \tag{9}$$

Assuming that $L'_{bus} = nL'_P$. Equation (9) can be simplified as Equation (10),

$$C_{DE} \gg \max\left(\left(1+\frac{1}{n}\right)C_F, \left(1+\frac{1}{n}\right)C_{oss}\right). \tag{10}$$

As simplified steps of Equation (7), Equation (11) represents that capacitor C_{DE} satisfies Equation (10).

$$C_{DE} \geq \max\left(100\left(1+\frac{1}{n}\right)C_F, 100\left(1+\frac{1}{n}\right)C_{oss}\right). \tag{11}$$

In Figure 4, capacitor C_{DE} is set to none, 0.1 nF, 1 nF, 10 nF, 100 nF, and 1000 nF, respectively. When capacitor C_{DE} is larger than 10nF, the peak impedances on the terminal impedances, Z_{d_1} and Z_{m2_1}, are obviously smaller than without the capacitor C_{DE}. In addition, the high-resonance frequencies are scarcely affected by capacitor C_{DE}. However, the low-frequency resonances are still affected by the capacitor C_{DE}. Based on Equations (3) and (6), the low-frequency resonances are caused by the capacitor C_{DE} and inductor L'_{bus}. The voltage fluctuation, Δv_{CDE}, on capacitor C_{DE} can be calculated as Equation (12). Assuming that the limitation of the voltage fluctuation is ΔV_{CDE}, capacitor C_{DE} also needs to satisfy Equation (13).

$$\Delta v_{CDE} = I_o \sqrt{\frac{L'_{bus}}{C_{DE}}} \sin\left(\frac{t}{\sqrt{L'_{bus} C_{DE}}}\right). \tag{12}$$

$$C_{DE} \geq \frac{4I_o^2}{\Delta V_{CDE}^2} L'_{bus}. \tag{13}$$

In summary, the DC-side snubber C_{DE} needs to satisfy Equation (14), and the decoupling of the parasitic inductor L'_{bus} and the suppression for the low-frequency oscillation on the turn-off voltage can be realized.

$$C_{DE} \geq \max(100C_F, 100C_{oss}, 100\left(1+\frac{1}{n}\right)C_F, 100\left(1+\frac{1}{n}\right)C_{oss}, \frac{4I_o^2}{\Delta V_{CDE}^2} L'_{bus}). \tag{14}$$

2.4. Analyzation for the Suppressing Effectiveness of Capacitor C_{DE}

Assume the peak impedances, $Z_{d\_1\_H\_P}$ and $Z_{m2\_1\_H\_P}$, of the SiC diode and SiC MOSFET with the capacitor C_{DE} are $1/\rho$ times the peak impedances, $Z_{d\_H\_P}$ and $Z_{m2\_H\_P}$, without the capacitor C_{DE}. Equations (15)–(18) express the peak impedances without and with the capacitor C_{DE}.

$$Z_{d\_H\_P} = \frac{L'_P + L'_{bus}}{R_{DS\_on} C_F}, \tag{15}$$

$$Z_{m2\_H\_P} = \frac{(L'_P + L'_{bus}) C_{oss}}{R_G C_{GD}^2}, \tag{16}$$

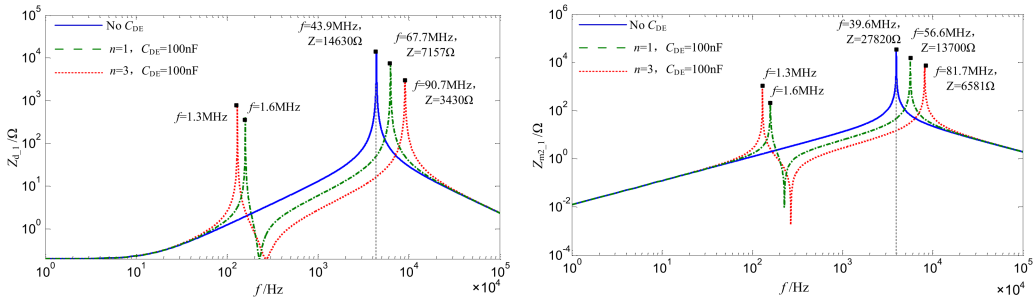
$$Z_{d\_1\_H\_P} = \frac{L'_P}{R_{DS\_on} C_F}, \tag{17}$$

$$Z_{m2\_1\_H\_P} = \frac{L'_P C_{oss}}{R_G C_{GD}^2}. \tag{18}$$

Therefore, Equation (19) can be derived based on the relations between the peak impedances $Z_{d\_H\_P}$, $Z_{m2\_H\_P}$ and $Z_{d\_1\_H\_P}$, $Z_{m2\_1\_H\_P}$.

$$\rho \leq n + 1. \tag{19}$$

Figure 5 presents the amplitude–frequency curves of terminal impedances, Z_{d_1} and Z_{m2_1}, with different n values based on parameters in Table 1. Inductors L'_{bus} and L'_P are set to 50 nH, 150 nH or 100 nH, 100 nH, respectively, which means n = 3 or n = 1. Based on Figure 5, the larger n is, the smaller L'_P is, which represents that the capacitor C_{DE} is closer to the devices, the lower the peak impedance is. Compared to without C_{DE}, the peak impedance of terminal impedances, Z_{d_1} and Z_{m2_1}, with C_{DE} is reduced nearly $n/(n+1)$ times.

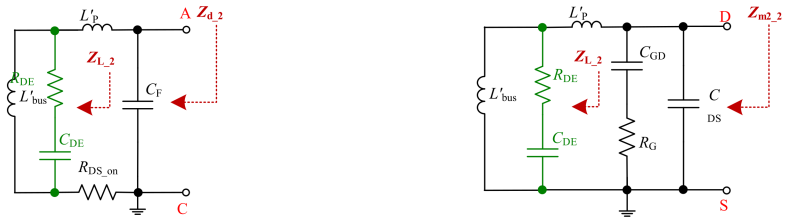


(**a**) (**b**)

Figure 5. Amplitude–frequency curves of terminal impedances, Z_{d_1} and Z_{m2_1}, with different n values (**a**) at Stage 4 and (**b**) at Stage 7 and Stage 8.

3. Analyzation for DC-Side Snubber with Damping Resistor C_{DE}–R_{DE}

When the DC-side snubber C_{DE} cannot be selected large enough to avoid the low-frequency oscillation on the turn-off voltage, the suppressing effectiveness is not good owning to the bigger capacitor with parasitic inductors added to the switching power loop. The DC-side snubber with a damping resistor can be used to solve this problem, which is the high-frequency decoupling capacitor in series with a damping resistor. Figure 6 shows the equivalent circuits with this DC-side snubber. Capacitor C_{DE} is to decouple the parasitic inductor L'_{bus}, and resistor R_{DE} is to dampen the low-frequency oscillation on the turn-off voltage.



(**a**) (**b**)

Figure 6. Equivalent circuits with capacitor C_{DE} and resistor R_{DE} (**a**) at Stage 4, (**b**) at Stage 7 and Stage 8.

If capacitor C_{DE} satisfies Equation (7) and Equation (11) and realizes the decoupling of the inductor L'_{bus} from the switching power loop, the low-frequency resonance is only caused by the capacitor C_{DE} and inductor L'_{bus}. The impedance Z_{L_2} of the paralleling branches L'_{bus} and C_{DE}-R_{DE} can be calculated as Equation (20),

$$Z_{L\_2}(s) = \frac{(C_{DE}R_{DE}s + 1)L'_{bus}s}{C_{DE}L'_{bus}s^2 + C_{DE}R_{DE}s + 1}. \tag{20}$$

Due to the damping resistor R_{DE} that is in series with capacitor C_{DE}, the impedance Z_{L_2} at the high-resonance frequency $f_{d1\_1\_1}$ and the high-resonance frequency $f_{m2\_1\_1}$ should be much lower than the impedance of inductor L'_P. The relations can be expressed as Equation (21),

$$\begin{cases} \left|j2\pi f_{d\_1\_1}L'_P\right| \gg \left|\dfrac{(j2\pi f_{d\_1\_1}C_{DE}R_{DE}+1)j2\pi f_{d\_1\_1}L'_{bus}}{(j2\pi f_{d\_1\_1})^2C_{DE}L'_{bus}+j2\pi f_{d\_1\_1}C_{DE}R_{DE}+1}\right| \\ \left|j2\pi f_{m2\_1\_1}L'_P\right| \gg \left|\dfrac{(j2\pi f_{m2\_1\_1}C_{DE}R_{DE}+1)j2\pi f_{m2\_1\_1}L'_{bus}}{(j2\pi f_{m2\_1\_1})^2C_{DE}L'_{bus}+j2\pi f_{m2\_1\_1}C_{DE}R_{DE}+1}\right| \end{cases}. \tag{21}$$

Assuming that $C_{DE} = m_1 C_F$ and $C_{DE} = m_2 C_{oss}$, Equation (21) can be simplified as

$$\begin{cases} R_{DE} \ll R_{DE1} \\ R_{DE} \ll R_{DE2} \end{cases}, \tag{22}$$

where $R_{DE1} = ((1 - nm_1)^2 - n^2)/((n^2 - 1)(n + 1)m_1))^{1/2}((L'_{bus} + L'_P)/C_{DE})^{1/2}$ and $R_{DE2} = (((1 - nm_2)^2 - n^2)/((n^2 - 1)(n + 1)\, m_2))^{1/2}((L'_{bus} + L'_P)/C_{DE})^{1/2}$. To reduce the scale of the damping resistor R_{DE}, Equation (22) can be simplified as,

$$R_{DE} \leq \min(\frac{1}{5}R_{DE1}, \frac{1}{5}R_{DE2}). \tag{23}$$

Due to its discriminant of Equation (20), the low-frequency resonances on the terminal impedances, Z_{d_1} and Z_{m2_1}, of the SiC diode and SiC MOSFET can be cancelled completely when the damping resistor R_{DE} satisfies Equation (24).

$$R_{DE} \geq R_{DE3}, \tag{24}$$

where $R_{DE3} = 2(n/(n + 1))^{1/2}((L'_{bus} + L'_P)/C_{DE})^{1/2}$. According to Equations (23) and (24), Figure 7 shows the range of the damping resistor R_{DE}. The larger n is, the smaller the range of the damping resistor R_{DE} is.

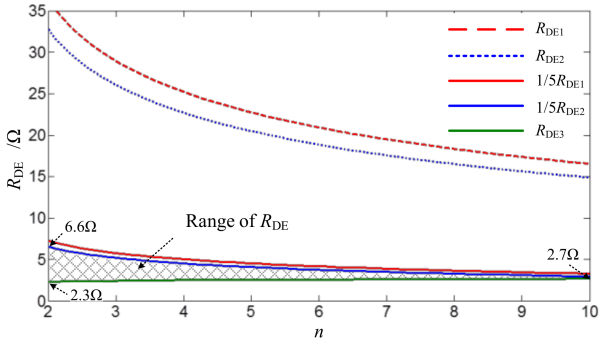


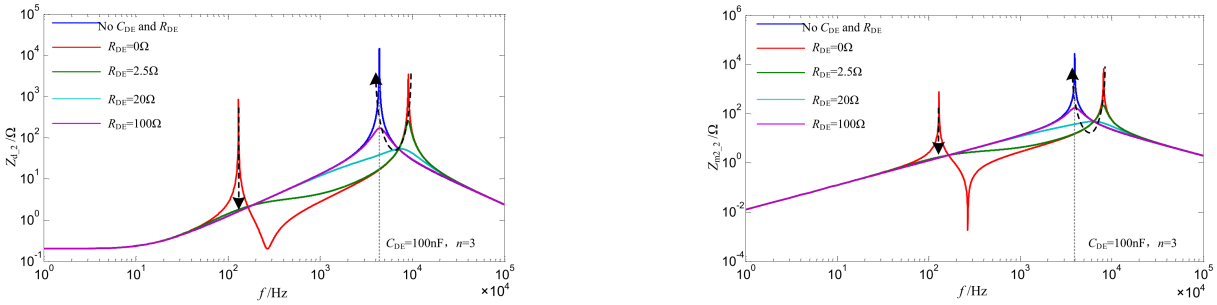
Figure 7. Range of resistor R_{DE} with different n.

According to Figure 7, the terminal impedances, Z_{d_2} and Z_{m2_2}, of the SiC diode and SiC MOSFET can be calculated as Equations (25) and (26),

$$Z_{d\_2}(s) = \frac{N_{d\_2}(s)}{D_{d\_2}(s)}, \tag{25}$$

$$Z_{m2\_2}(s) = \frac{N_{m2\_2}(s)}{D_{m2\_2}(s)}. \tag{26}$$

where $N_{d\_2}(s)$, $D_{d\_2}(s)$, $N_{m2\_2}(s)$, and $D_{m2\_2}(s)$ are shown in Appendix A. The amplitude–frequency curves of Z_{d_2} and Z_{m2_2}, based on Table 1, are shown in Figure 8. From Figure 8, the low-frequency peak impedances of Z_{d_2} and Z_{m2_2} are eliminated, which indicates this DC-side snubber can effectively suppress the low-frequency oscillation on turn-off voltage. In addition, if resistor R_{DE} satisfies its range requirement, the high-resonance frequency of the terminal impedance, Z_{d_2} and Z_{m2_2}, is scarcely affected, and the high-frequency peak impedances are reduced. It is indicated that inductor L'_{bus} can be decoupled from the switching power loop, and resistor R_{DE} has suppressing effectiveness on the turn-off overvoltage.



(**a**) (**b**)

Figure 8. Amplitude–frequency curves of the terminal impedances, Z_{d_2} and Z_{m2_2}, with capacitor C_{DE} and resistor R_{DE} (**a**) at Stage 4 and (**b**) at Stage 7 and Stage 8.

4. Experimental Results

To verify the suppressing effectiveness of DC-side snubbers, experiments using the 1200V SiC MOSFET C2M0080120D and the SiC diode C4D20120A by Cree Inc. are marked based on the double-pulse-test circuit. Figure 9 presents the testing platform, and Table 2 shows the test equipment used in the platform.

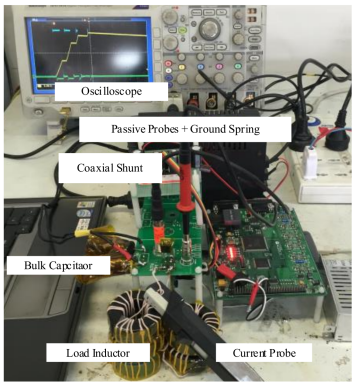


Figure 9. DC-side snubber testing platform.

Table 2. Test equipment used in the platform.

Model	Type	Bandwidth
Tektronix TCP0030A	Current probe	120 M
Tektronix DPO4054B	Oscilloscope	500 M
CP3308R	Passive probe	300 M
SSDN-10	Coaxial Shunt	2000 M

Figure 10 shows the experimental waveforms without and with capacitor C_{DE}, in which capacitor C_{DE} is the multilayer ceramic capacitor and C_{DE} = 100 nF. In Figure 10a,b, the turn-off voltage of the SiC diode is presented. In Figure 10c,d, the turn-off voltage of the SiC MOSFET is presented. Compared to results in Figure 10a,c, without capacitor C_{DE}, the turn-off overvoltage of the SiC diode and SiC MOSFET reduces obviously in Figure 10b,d. However, it is shown that the low-frequency oscillation overlays the high-frequency oscillation on the turn-off voltage of the SiC diode and SiC MOSFET.

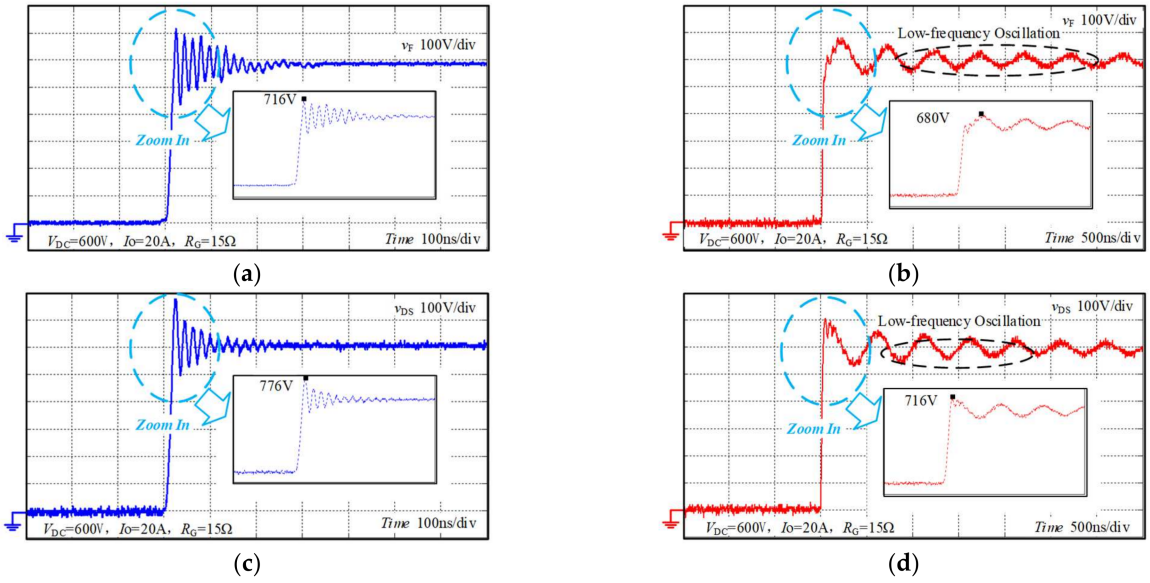


Figure 10. Tested waveforms without and with capacitor C_{DE}. (**a**) Turn-off voltage of the SiC diode without C_{DE}, (**b**) turn-off voltage of the SiC diode with C_{DE} = 100 nF, (**c**) turn-off voltage of the SiC MOSFET without C_{DE}, and (**d**) turn-off voltage of the SiC MOSFET with C_{DE} = 100 nF.

Figure 11 shows the experimental waveforms with capacitor C_{DE} and resistor R_{DE}, in which C_{DE} = 100 nF and R_{DE} = 2.5 Ω or R_{DE} = 5 Ω. In Figure 11a,b, the turn-off voltage of the SiC diode is presented. In Figure 11c,d, the turn-off voltage of the SiC MOSFET is presented. Compared to the results in Figure 10b,d, the low-frequency oscillations on the turn-off voltage of the SiC diode and SiC MOSFET are suppressed effectively. In addition, the turn-off overvoltage of the SiC diode and SiC MOSFET are reduced in Figure 11a,c, in which resistor R_{DE} = 2.5 Ω. Comparing Figure 11a,c with Figure 11b,d, the turn-off overvoltage of the SiC diode and SiC MOSFET were obviously increased when R_{DE} = 5 Ω.

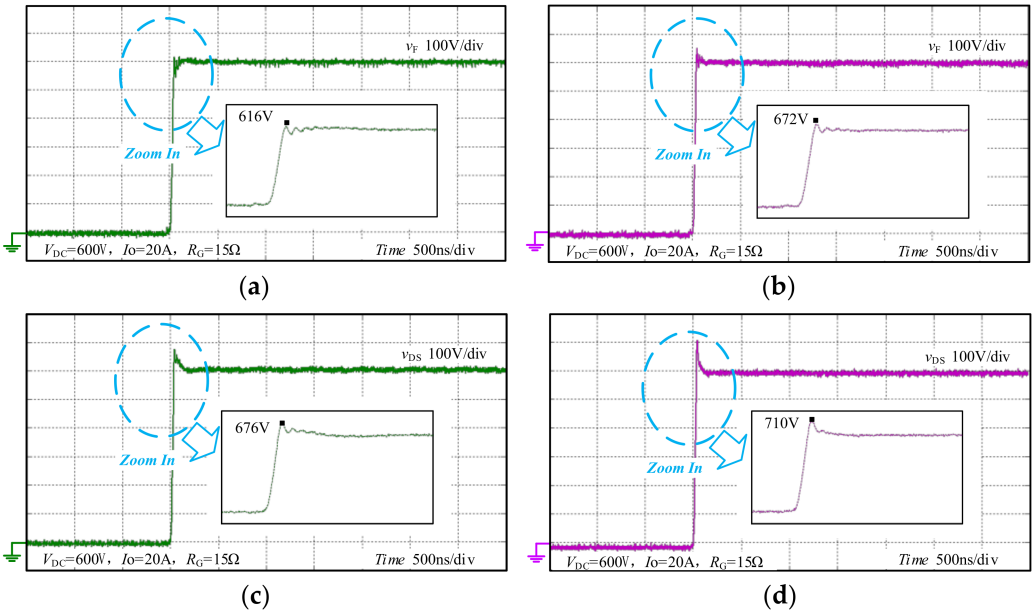


Figure 11. Tested waveforms with capacitor C_{DE} and resistor R_{DE}. (**a**) Turn-off voltage of the SiC diode at C_{DE} = 100 nF and R_{DE} = 2.5 Ω, (**b**) turn-off voltage of the SiC diode at C_{DE} = 100 nF and R_{DE} = 5 Ω, (**c**) turn-off voltage of the SiC MOSFET at C_{DE} = 100 nF and R_{DE} = 2.5 Ω, and (**d**) turn-off voltage of the SiC MOSFET at C_{DE} = 100 nF and R_{DE} = 5 Ω.

Figure 12 presents the turn-off overvoltage of the SiC diode and the SiC MOSFET at different I_o, V_{DC}, and R_G. From Figure 12, although the higher I_o, higher V_{DC}, and lower R_G make the turn-off overvoltage higher, DC-side snubbers have effective suppression on the turn-off overvoltage of the SiC diode and SiC MOSFET. Moreover, the DC-side snubber with the damping resistor C_{DE}-R_{DE} is the most effective. Figure 13 presents the effect of DC-side snubbers on the switching losses of the SiC MOSFET at different I_o and V_{DC}. Figure 13 employs the switching losses of the SiC MOSFET without the snubber as a reference quantity and transforms the switching losses with DC-side snubbers into per-unit. The turn-on loss of the SiC MOSFET with DC-side snubbers increases, and the turn-off loss of the SiC MOSFET decrease, because a portion of parasitic inductors is decoupled from the power switching loop. Figure 14 presents the efficiency of a 1.1kW buck converter with DC-side snubbers. The tested conditions of the buck converter are presented in Table 3, and the efficiency is tested under open-loop control. From Figure 14, it is observed that the efficiency of the buck converter with C_{DE} = 100 nF, R_{DE} = 2.5 Ω is a little lower than with C_{DE} = 100 nF, which is owning to the loss of R_{DE}.

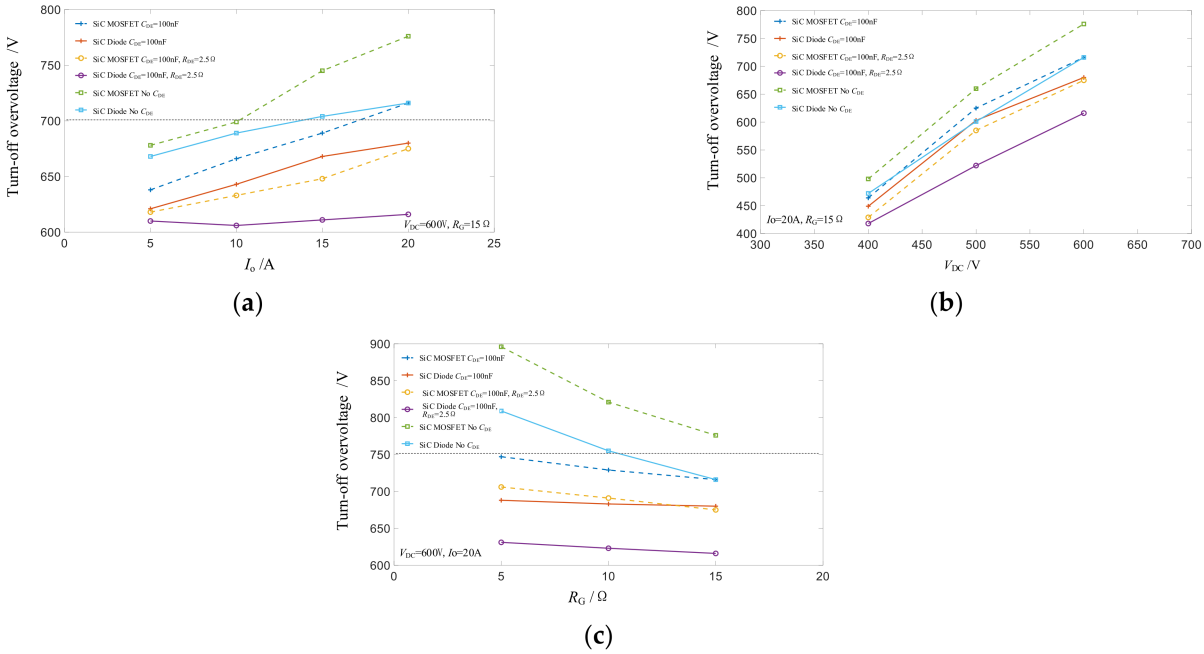


Figure 12. Turn-off overvoltage of the SiC diode and the SiC MOSFET with DC-side snubbers (**a**) at different I_o, (**b**) at different V_{DC}, and (**c**) at different R_G.

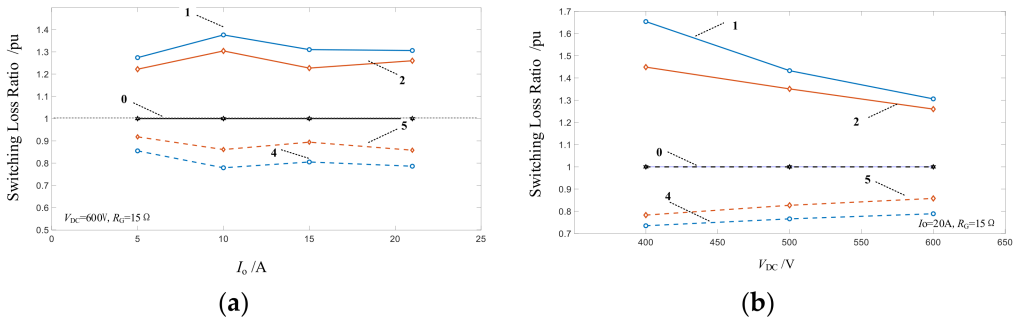


Figure 13. Switching losses of the SiC MOSFET with DC-side snubbers (**a**) at different I_o and (**b**) at different V_{DC}. (Note: 0: turn-on loss or turn-off loss with no C_{DE}, 1: turn-on loss with C_{DE} = 100 nF, 2: turn-on loss with C_{DE} = 100 nF and R_{DE} = 2.5 Ω, 4: turn-off loss with C_{DE} = 100 nF, 5: turn-off loss with C_{DE} = 100 nF and R_{DE} = 2.5 Ω).

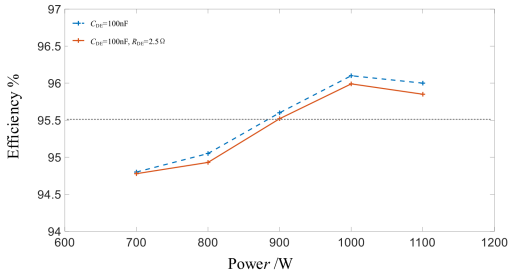


Figure 14. Efficiency of the buck converter with DC-side snubbers.

Table 3. Efficiency-tested conditions of the buck converter.

Parameter	Value	Parameter	Value
Input voltage	600 V	Switching frequency	50 kHz
Output voltage	150 V	Output inductor	100 μH
Output power	700 W~1100 W	Output capacitor	220 μF

5. Conclusions

This paper designs effective DC-side snubbers to suppress the turn-off overvoltage and oscillation for SiC devices application. By the turn-off terminal impedances of the SiC diode and SiC MOSFET, the suppressing mechanisms and design principles of DC-side snubbers are investigated. Based on the above analysis and experimental results, the following conclusions can be drawn:

(1) According to the guideline design for DC-side snubbers, the turn-off overvoltage and oscillation of the SiC diode and the SiC MOSFET can be suppressed effectively.
(2) Capacitor C_{DE} is closer to devices, which represents the parasitic inductors in the switching power loop are lower, which means the lower the peak impedance is and the lower the turn-off overvoltage is.
(3) The DC-side snubber with the damping resistor C_{DE}-R_{DE} can not only eliminate the low-frequency oscillation on the turn-off voltage but also can reduce the turn-off overvoltage.

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Appendix A

In Equation (1), $N_{d\_1}(s)$ and $D_{d\_1}(s)$ are as the following,

$$N_{d\_1}(s) = C_{DE}L\prime_{bus}L\prime_{P}s^3 + C_{DE}L\prime_{bus}R_{DS\_on}s^2 + L_{P}s + R_{DS\_on} \tag{A1}$$

$$D_{d\_1}(s) = C_{DE}C_{F}L\prime_{bus}L\prime_{P}s^4 + C_{DE}C_{F}L\prime_{bus}R_{DS\_on}s^3 + (C_{DE}L\prime_{bus} + C_{F}L_{P})s^2 + C_{F}R_{DS\_on}s + 1 \tag{A2}$$

In Equation (4), $N_{m2\_1}(s)$ and $D_{m2\_1}(s)$ are as the following,

$$N_{m2\_1}(s) = s\left(C_{DE}C_{GD}L\prime_{bus}L\prime_{P}R_{G}s^3 + C_{DE}L\prime_{bus}L\prime_{P}s^2 + C_{GD}R_{G}L_{P}s + L_{P}\right) \tag{A3}$$

$$D_{m2\_1}(s) = C_{DE}C_{DS}C_{GD}L\prime_{bus}L\prime_P R_G s^5 + C_{DE}C_{oss}L\prime_{bus}L\prime_P s^4 + C_{GD}R_G(C_{DE}L\prime_{bus} + C_{DS}L_P)s^3 + (C_{DE}L\prime_{bus} + C_{oss}L_P)s^2 + C_{GD}R_G s + 1 \quad \text{(A4)}$$

In Equation (25), $N_{\mathrm{d\_2}}(s)$ and $D_{\mathrm{d\_2}}(s)$ are as the following,

$$N_{d\_2}(s) = C_{DE}L\prime_{bus}L\prime_P s^3 + (C_{DE}L\prime_{bus}R_{DE} + C_{DE}L\prime_{bus}R_{DS\_on} + C_{DE}L\prime_P R_{DE})s^2 + (L_P + C_{DE}R_{DE}R_{DS\_on})s + R_{DS\_on} \quad \text{(A5)}$$

$$D_{d\_2}(s) = C_{DE}C_F L\prime_{bus}L\prime_P s^4 + (C_{DE}C_F L\prime_{bus}R_{DS\_on} + C_{DE}C_F L_P R_{DE})s^3 + (C_{DE}L\prime_{bus} + C_F L_P + C_{DE}C_F R_{DE}R_{DS\_on})s^2 + (C_{DE}R_{DE} + C_F R_{DS\_on})s + 1 \quad \text{(A6)}$$

In Equation (26), $N_{\mathrm{m2\_2}}(s)$ and $D_{\mathrm{m2\_2}}(s)$ are as the following,

$$N_{m2\_2}(s) = C_{DE}C_{GD}L\prime_{bus}L\prime_P R_G s^4 + (C_{DE}L\prime_{bus}L\prime_P + C_{DE}C_{GD}L_P R_{DE}R_G)s^3 + (C_{DE}L\prime_{bus}R_{DE} + C_{GD}L\prime_{bus}R_G + C_{DE}L\prime_P R_{DE} + C_{GD}L\prime_P R_G)s^2 + L_P s \quad \text{(A7)}$$

$$D_{m2\_2}(s) = C_{DE}C_{DS}C_{GD}L\prime_{bus}L\prime_P R_G s^5 + (C_{DE}C_{oss}L\prime_{bus}L\prime_P + C_{DE}C_{DS}C_{GD}L_P R_{DE}R_G)s^4 + (C_{GD}C_{oss}L\prime_{bus}R_G + C_{DE}C_{oss}L_P R_{DE} + C_{DS}C_{GD}L\prime_P R_G)s^3 + (C_{DE}L\prime_{bus} + C_{oss}L_P + C_{DE}C_{GD}R_{DE}R_G)s^2 + (C_{DE}R_{DE} + C_{GD}R_G)s + 1 \quad \text{(A8)}$$

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