

Article

Methodology for Improving High-Power Harmonic Measurement Accuracy and Stability

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Abstract: With continued dimension scaling of the semiconductor devices, the parasitic parameters become increasingly obvious and it affects the device performance directly. The harmonic distortion is one of the key factors to limit the RF system bandwidth resource and channel capability. Therefore, it is crucial to precisely extract the nonlinear index of the device and system. High-precision harmonic distortion extraction on a device's intrinsic characteristics could be beneficial not only to device modeling but also to circuit design. However, the harmonic distortion measurement is highly sensitive to the peripheral circuit and instrumentations, especially in high power stimulus; its repeatability and stability are also hard to control. This paper aims to contribute to the subject by extending the measurement methodology, combining isolation compensation with a dual trace phase tuning (DTPT) technique to obtain the optimal harmonic value. As shown by the experiment results, the optimized approach could achieve high measurements of both accuracy and stability. The proposed methodology is validated with measurement data and compared with conventional measurement architecture. The assessment results prove that the proposed methodology could improve 30.66% and 28.84% measurement accuracy both on second and third harmonics. Simultaneously, the proposed methodology decreases gauge repeatability and reproducibility (GRR) from 56.49% to 7.13%.

Keywords: harmonic; dual trace phase tuning (DTPT); phase compensation; isolation

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1. Introduction

The market explosion of big data [1], automatable cars [2], and artificial intelligence internet of things (AIoT) [3–5] boosts the global demands of the multi-mode and multi-frequency. Facing the upcoming information era, frequency channel spacing is close to achieving spectral efficiency as indicated in Figure 1. In narrow-band and wide-band communication systems, the distortion products might be unwanted in-channel, in-band, or out-of-band spectral signals. It would seriously restrict the bandwidth resource. The major impact is harmonic distortion. Harmonic distortion is defined as the amplitude-transferring characteristics of the device which prevent it from precisely tracking the input signal. It generates integer multiples of the input signal frequencies. Harmonic distortion not only degrades the performance of the transmitter but also the sensitivity of receivers.

In order to improve spectrum efficiency and restrain the non-linear distortion, most studies focus on protocol algorithms, material processes, and circuit design architecture. The spectrum allocation technique is essential for the protocol algorithm [6]. Some researchers investigate joint user association and spectrum allocation to further improve spectral efficiency for massive multiple-input multiple-output (MIMO) enabled heterogeneous networks with full-duplex wireless backhaul [7]. Some researchers study the device

structure and process to optimize the harmonic distortion suppression such as silicon on insulator (SOI). SOI CMOS process plays a pivotal role in material process control. It is selected to fabricate the chip to restrain the harmonic distortion brought from the silicon substrate. Both standard high resistivity HR-SOI and two types of trap-rich high resistivity HR-SOI substrates named enhanced signal integrity high resistivity silicon-on-insulator (eSI HR-SOI) provided by SOITEC are thoroughly studied and compared to eliminate distortion coming from the parasitical effect of the substrate structure [8–11]. Meanwhile, both symmetry shunt/series stacked topology and asymmetry with double floating techniques [12,13] are for high linear design architecture. The design with integrated filtering performance is to linearize the high-power antenna and power amplifiers' distortion performance [14,15]. The dual coupled-line sections embedded in the conventional quarter-wavelength transmission lines are designed for wideband filtering power divider with ultra-wideband harmonic rejection and isolation [16].

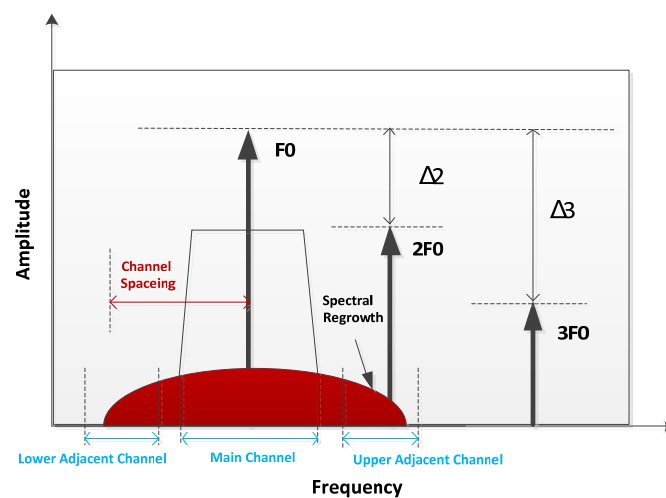


Figure 1. Harmonic spectral and spectral regrowth.

However, the phase angles' effects of harmonic measurement are simply ignored and they have not been investigated thoroughly. The existing methodologies and protocols for harmonics characterizing are only confined to the measurement of the amplitudes of these quantities [17–19]. It is critical to detect undesirable and nonlinear spectral distortions. The accurate optimal harmonic rejection and measurement are becoming new hotspots in the communication and semiconductor domains. The conventional method based on the standard 50-ohm terminator for harmonic contribution assessment highly depends on instrument accuracy and testing environment [20]. What's more, the repeatability and reproducibility challenge of harmonic measurement is also unprecedented. The SOI monolithic RF switch is realized as the carrier in the following paper. The high linear performance of the RF switch is already optimized by both eSI HR-SOI process control and symmetry stacked design topology. This work focuses on measurement methodology for deep further harmonic accuracy and stability improvement. DTPT with isolation compensation methodology is proposed to improve harmonics measurement accuracy and stability. The intrinsic device harmonic characteristic measured precisely could be the basis of reference for design optimization.

2. Mechanism on Harmonic Measurement Architecture

The harmonic distortion is generally emitted by nonlinear loads of the nonlinear system. It adds overtones that are whole number multiples of a wave's frequencies. Nonlinearities that give rise to amplitude distortion in the systems are most often measured in

terms of the harmonics added to a pure sine wave fed to the system. Harmonic distortion may be expressed in terms of the relative strength of individual components as below:

$$y(t) = a_1x(t) + a_2x^2(t) + a_3x^3(t) + \dots \quad (1)$$

$$x(t) = A\cos(\omega t + \phi) \quad (2)$$

$$y(t) = a_1A\cos(\omega t + \phi) + a_2A^2(\cos(\omega t + \phi))^2 + a_3A^3(\cos(\omega t + \phi))^3 + \dots \quad (3)$$

$$= \frac{a_2A^2}{2} + \left(a_1A + \frac{3a_3A^3}{4}\right)\cos(\omega t + \phi) + \frac{a_2A^2}{2}\cos 2(\omega t + \phi) + \frac{a_3A^3}{2}\cos 3(\omega t + \phi) + \dots \quad (4)$$

where, $y(t)$ is the nonlinear system function expression and $x(t)$ is the single-tone wave input. The second term of a polynomial represents the fundamental of the frequency. The third and fourth terms of polynomials stand for the second and the third harmonics. ϕ is expressed [21] as follows:

$$\phi = \arg \frac{S_{21}(1 - \Gamma_S\Gamma_L)}{(1 - S_{11}\Gamma_S)(1 - S_{22}\Gamma_L) - S_{21}S_{12}\Gamma_S\Gamma_L} \quad (5)$$

where S_{ij} are the scattering coefficients of the device under test (DUT). Γ_S and Γ_L are the source and load reflection coefficients looking from different test ports, respectively.

The straightforward harmonic distortion measurement method is using a continuous wave tone. Figure 2 shows the conventional high-power harmonic measurement architecture diagram. A signal generator (SG) provides the fundamental wave. In order to effectively release the methodology to volume multi-test verification, a V93K tester with a PSRF instrument card is selected as the signal generator whose power capability is 12 dBm. While doing the high-power harmonic measurement, the stimulus test signal requires over 36 dBm generally. Due to the fact that the basic instruments can't provide such a high input power, the external power amplifier (PA) is involved to provide certain and effective gain. In this paper, the gain of PA is 50 dB and the power handling capability is 45 dBm. Due to the introduction of the PA, the system has a high universality even though the SG is changed. Considering the PA's nonlinear characteristic, the multiple harmonics introduced by the amplifier itself can't be ignored. In order to eliminate the harmonic distortion caused by the amplifier, the additional low pass filter (LPF) is introduced into the test system to isolate the harmonic caused by the nonlinear factors of the power amplifier. The pass-band of LPF is DC-1000 MHz and the out-band rejection is 52 dB.

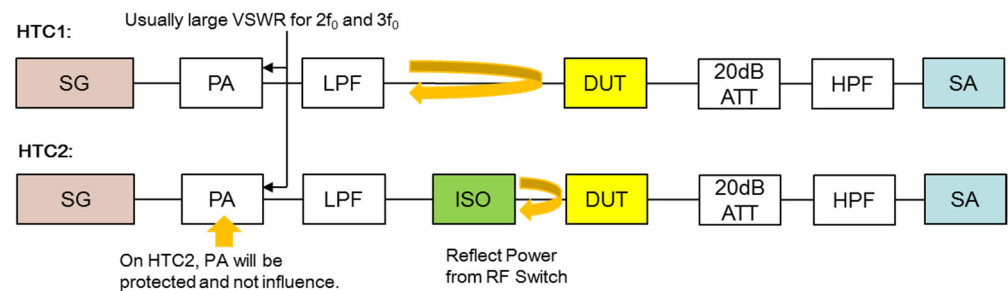


Figure 2. Conventional Harmonic Measurement Architecture.

The interface plane between LPF and DUT will cause the phase shift and impedance mismatch that lead to the generation of undesired nonlinear terms. Sometimes the distortion will be seriously amplified, specifically in such a high-power condition evaluation. In order to obtain the pure stimulus signal which doesn't mask the DUT's actual performance, one more Isolator (ISO) is in the loop to improve the source's effective harmonic distortion. In the back-end loop of the test chain, a cascaded attenuator and high pass filter

(HPF) are used to avoid such high-power fundamentals in the spectrum analyzer (SA). The pass-band of HPF is 1650–5000 MHz and the out-band rejection is 51 dB. Characterizing the harmonic distortion performance of the switch requires a low-distortion stimulus test signal and accurate measurement instruments and methods. The sensitivity of the harmonic measurement is restricted by the source's intrinsic harmonic and the SA dynamic range.

In order to demonstrate the above model, two different performance ISOs are used for the bench analysis. As a result, the difference gap of harmonic distortion almost reaches 10 dB while it works at high power transmission. The second harmonic is seriously affected without an isolator in the measurement system. For further study, we measure the smith chart and S parameter as Figure 3 shown. It is found that the harmonic impedance termination has a great influence on the distortion performance of the switch.

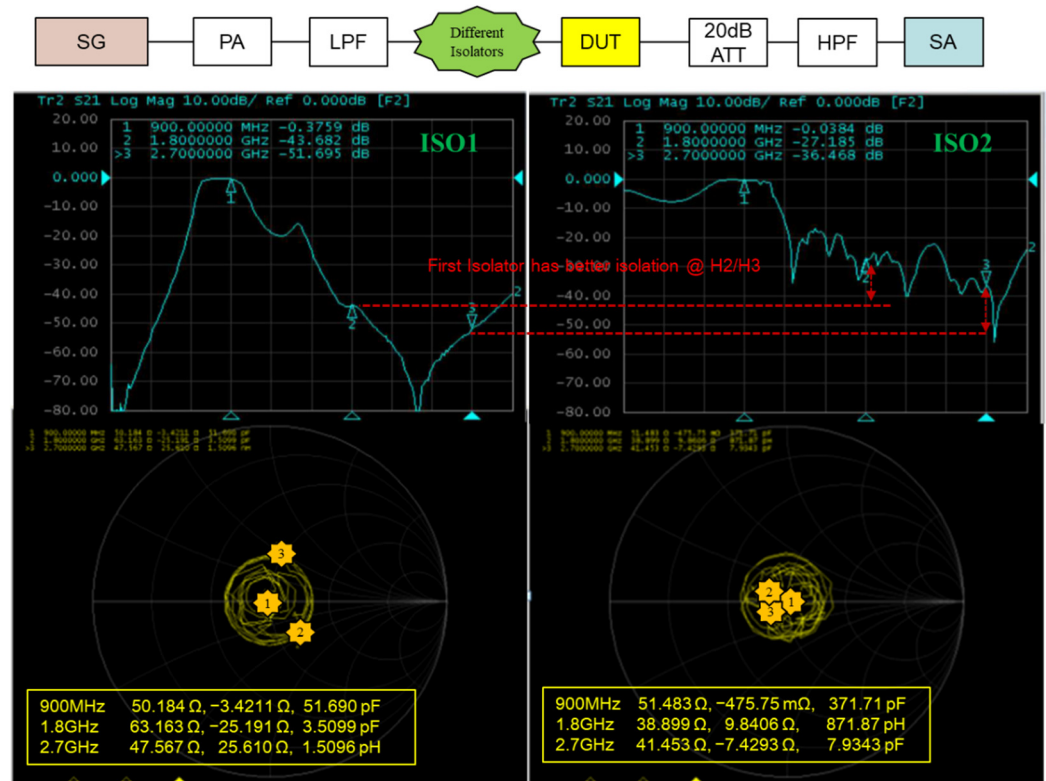


Figure 3. Performance Comparisons with Different Isolator.

3. DTPT for High Accuracy Harmonic Measurement

The above description of the analytical model demonstrates that the front-end and back-end harmonic impedance termination seriously affects the RF devices' distortion. Meanwhile, the best condition of the port match needs to be found out. Figure 4 illustrates the verification bench system diagram. Both stimulus and measurement are executed by the V93K tester with a PSRF instrument card. Harmonic verification is carried out by front-end phase tuning in half period and isolation compensation. While variable components are connected to the verification port, the phase $\Delta\phi$ is changed so that front superscripts i and f denote the initial and final settings, respectively; $\Delta\phi$ may be similarly expressed [22] as follows:

$$\Delta\phi = \arg \frac{{}^f S_{21} (1 - {}^i S_{11} \Gamma_S) (1 - {}^i S_{22} \Gamma_L) - {}^i S_{21} {}^i S_{12} \Gamma_S \Gamma_L}{{}^i S_{21} (1 - {}^f S_{11} \Gamma_S) (1 - {}^f S_{22} \Gamma_L) - {}^f S_{21} {}^f S_{12} \Gamma_S \Gamma_L} \quad (6)$$

$$\Delta\phi|_{\Gamma_S=\Gamma_L=0} = \arg \frac{f S_{21}}{i S_{21}} = \Delta\phi_{21} \quad (7)$$

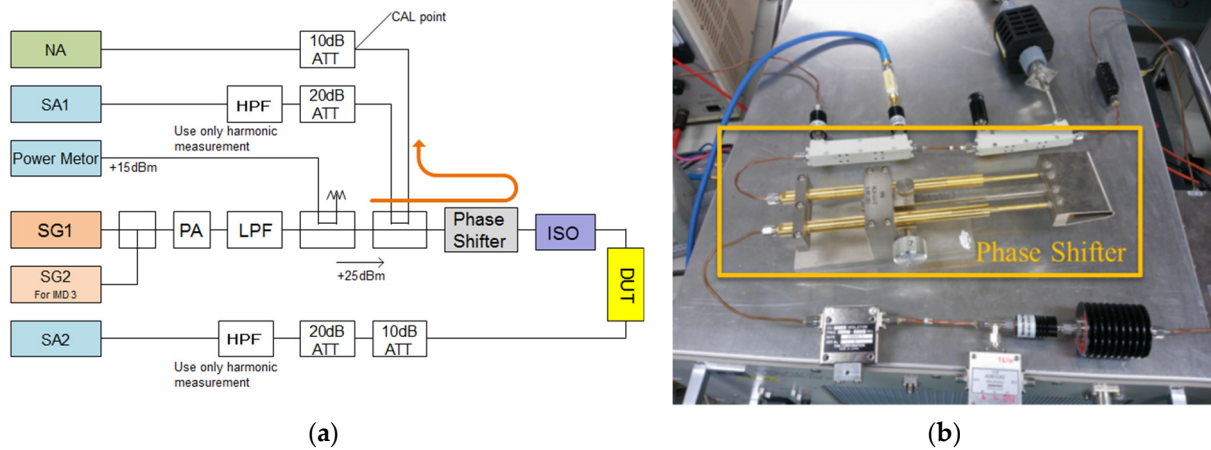


Figure 4. Verification circuit with phase shifter (a) Simple diagram of the system (b) Actual setup environment.

When both the front-end and the back-end load of DUT haven't a reflection, Γ_S and Γ_L are defined as zero and $\Delta\phi$ could be expressed as the above in the ideal condition. From the bench test results as Table 1 shows, for achieving a better and more stable distortion effect, it is necessary to offer lower harmonic impedance at the high-power port. A good performance isolator at high power is indispensable as well or the harmonics will be widely distributed. The isolation compensation could improve the harmonics convergence from 13.7 dB to 2.1 dB, while input is 25 dBm.

Table 1. Harmonic distortion in different isolation compensation.

Condition	Phase Shifter	Smith Chart @900 MHz	SA1		SA2	
			H2 [dBm]	H3 [dBm]	H2 [dBm]	H3 [dBm]
No isolation compensation	0 deg	56.062-j0.927	-93.67	-66.74	-60.28	-84.34
	45 deg	54.587-j4.652	-88.59	-63.84	-65.06	-86.01
	90 deg	55.553-j1.628	-88.57	-59.20	-51.43	-80.32
With isolation compensation	0 deg	53.511-j3.900	-90.77	-107.92	-58.92	-80.84
	45 deg	53.324-j3.000	-81.88	-97.46	-57.63	-80.34
	90 deg	52.103-j4.111	-89.48	-105.09	-56.77	-80.37

By the same token, dual trace phase tuning (DTPT) is proposed. Dual trace phase tuning sets out to track and tune the arbitrary phase at front-end and back-end ports. Figure 5 shows the actual verification circuit with both isolation compensation and DTPT. To eliminate the possibility of the auxiliary loop's measurement instability, the isolator is repositioned before LPF and a -3 dB attenuator is added to DUT's interface. Both the second harmonic (H2) and third harmonic (H3) impedance will be more concentrated on the central location of the smith chart. The positive effect is caused to the weakening of the different components' influences.

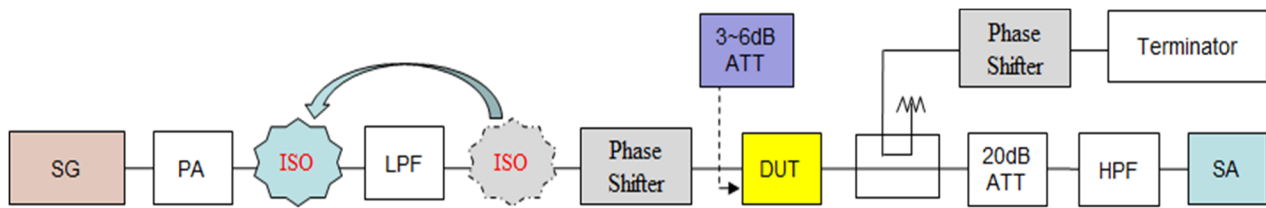


Figure 5. Verification circuit with isolation compensation and DTPT.

The 50-ohm terminator is conventionally based on the standard 50-ohm terminator without phase tuning. The H2-optimized and H3-optimized curves are pre-tuning the H2 and H3 harmonics impedance to optimize the optimal phase condition. From the results as Table 2 shown, H2 and H3 distortion could be restrained in different phase conditions. After the front-end harmonic impedance optimization with the DTPT approach, the H2 and H3 accuracy improvements achieve almost 15 dB and 10 dB, respectively, as Figures 6 and 7 shown. From the overall phases' tuning, the second and third harmonic measurement accuracy is optimized to 30.66% and 28.84% efficiently. Assessment results prove that the proposed methodology can restrain the influence of measurement error and it improves the accuracy of harmonic contribution assessment. Therefore, the remaining action is to choose the tradeoff on both second and third harmonic performances for final design consideration.

Table 2. Harmonic measurement with the DTPT method.

Harmonics	Methods	Phase Degree(°)								
		−180	−135	−90	−45	0	45	90	135	180
H2 (dBm)	50 Ω Terminator	−56.23	−52.75	−46.12	−45.27	−47.54	−49.32	−52.67	−55.98	−54.15
	H2 Optimized	−57.14	−53.69	−54.33	−59.15	−58.12	−56.32	−54.67	−55.68	−57.35
	H3 Optimized	−58.23	−55.71	−45.12	−44.26	−48.54	−48.32	−53.67	−55.98	−54.15
H3 (dBm)	50 Ω Terminator	−51.99	−53.24	−50.47	−48.56	−46.54	−43.37	−41.56	−44.78	−49.64
	H2 Optimized	−56.13	−51.57	−52.29	−48.58	−50.47	−49.89	−52.76	−54.32	−52.00
	H3 Optimized	−56.08	−53.76	−51.65	−53.21	−52.00	−51.64	−53.96	−52.35	−53.00

Note: The fundamental frequency (F0) is 900 MHz and input power is 36 dBm.

2nd Harmonic Result with Dual Trace Phase Tuning

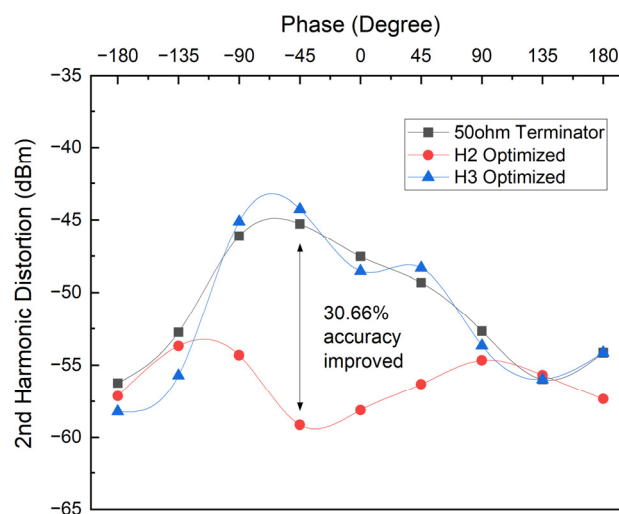


Figure 6. Second Harmonic Result with Dual Trace Phase Tuning.

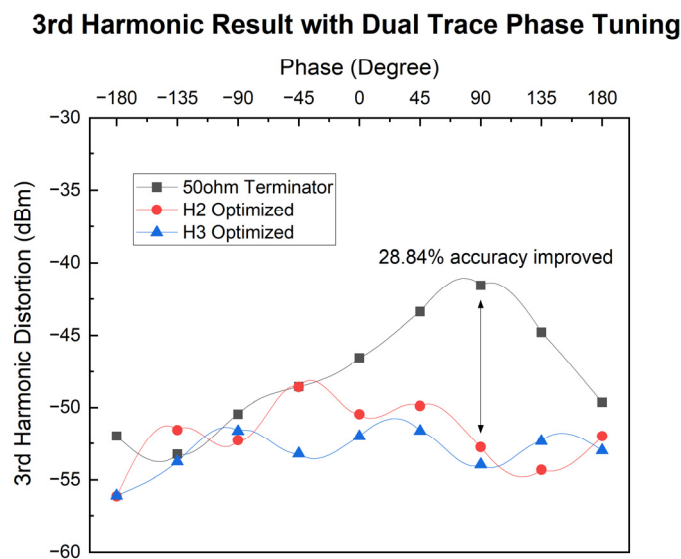


Figure 7. Third Harmonic Result with Dual Trace Phase Tuning.

4. DTPT on Measurement Stability Verification

Stability is the fundamental property to evaluate the DTPT tactic with isolation compensation, and GRR (Gauge Repeatability and Reproducibility) is involved in assessing the uncertainty and the stability verification. GRR is a particular technique in an industry that is utilized to determine the adequacy of a measurement system architecture [23,24]. Repeatability defines that variation in measurements obtained with the same instruments when used several times by an appraiser while measuring the identical characteristic on the same device. It's short-term and within EV (Equipment Variation). It indicates the gauge or potential capability. Reproducibility defines the variation in the average of the measurements made by different appraisers using the same gauge when measuring the identical characteristic on the same device. The AV (Appraiser Variation) error may be the appraiser, environment, or method. The methodology requires adequate discrimination and sensitivity. Instrument discrimination should divide the tolerance into ten parts or more and it ought to be in statistical control. In the following formula, nr expresses trials multiplied by samples. Pp is a constant value of 1.67. TV represents total variation. PV stands for part-to-part variation. NDC means the number of distinct categories:

$$EV = \bar{R} \times K_1 \quad (8)$$

$$AV = \sqrt{(X_{diff} \times K_2)^2 - \left(\frac{EV^2}{nr}\right)} \quad (9)$$

$$GRR = \sqrt{EV^2 \times AV^2} \quad (10)$$

$$TV_{tolerance} = \frac{(USL - LSL)}{6P_p} \quad (11)$$

$$PV_{tolerance} = \sqrt{TV^2 \times GRR^2} \quad (12)$$

$$NDC = 1.41 \times \left(\frac{PV}{GRR}\right) \quad (13)$$

Figure 8 sketches the compared relationships between two measurement methodologies and the Gauge R&R results as Table 3 shows, indicating that DTPT with isolation compensation achieves perfect repeatability and reproducibility versus conventional measurement architecture. The Gauge R&R of DTPT methodology could be kept around

7% and reach the acceptance criteria. Nevertheless, conventional architecture is seriously affected by device process variation, different setup environment, and measurement method.

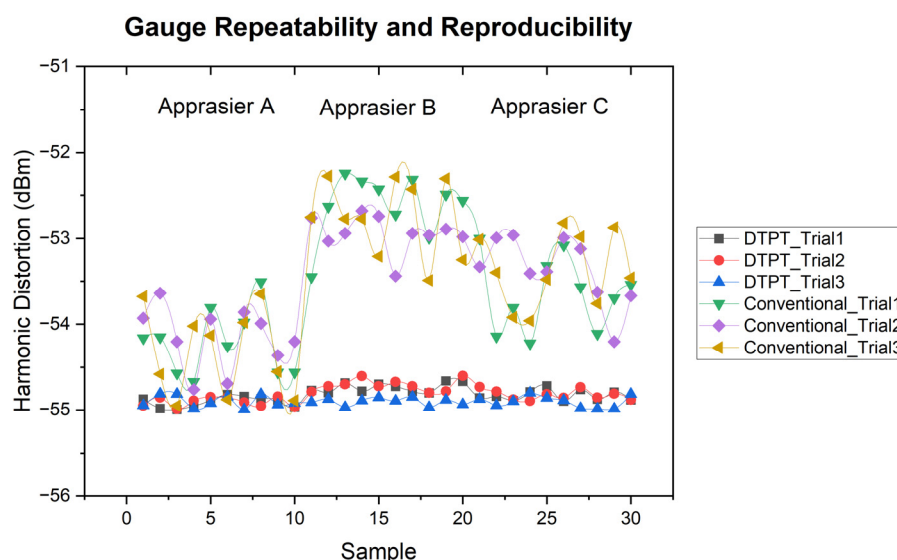


Figure 8. GRR comparisons between DTPT and Conventional Architecture.

Table 3. Gauge R&R Statistical Analysis Result.

	Conventional Architecture		DTPT with Isolation Compensation	
	SD	% Tolerance	SD	% Tolerance
EV	0.365	24.352%	0.087	5.829%
AV	0.764	50.973%	0.062	4.107%
GRR	0.847	56.489%	0.107	7.131%
PV	1.238	82.517%	1.496	99.745%

5. Conclusions

Harmonic measurement is sensitive to both front-end and back-end impedance match and the harmonic impedances of the RF device also have great influences on the performance. Isolation compensation can provide good isolation at fundamental power, second harmonic, and third harmonic. To avoid the worst phase case at the switch's antenna port, the properly chosen matching circuit is recommended. The overall harmonic performance could be improved by good selection of the critical phase angle. The precise and optimal harmonic distortion could be also measured through DTPT with an isolation compensation methodology implanted. Compared to conventional 50-ohm, terminator measurement architecture without phase tuning, the assessment results prove the proposed methodology could improve 30.66% and 28.84% measurement accuracy both on second and third harmonics and keep the gauge repeatability and reproducibility (GRR) reduced to around 7.13%.

Moreover, to achieve the best harmonic distortion performance, low impedance harmonic termination has to be determined at the high-power front-end port. The matching network can transform the VSWR circle to the perfect back-end port impedance condition to avoid the worst harmonic case performance phase by the DTPT approach. All in all, the isolation compensation and dual trace phase tuning are combined efficiently to seek out the optimal harmonic performance condition, especially at the back-end port's VSWR mismatch. Last but not least, the core hybrid methodology on dual trace phase tuning with

isolation compensation could be not only extended to ultra-low distortion FEM circuit design but also practical in application.

6. Patents

Chinese Patent License No: 201510560849.9.

Author Contributions: Conceptualization, methodology, L.W. and J.Z.; software, validation, investigation L.W.; data curation, writing—original draft preparation, L.W.; writing—review and editing, L.W. and J.Z.; visualization, L.W. and J.Z.; supervision, J.Z. All authors have read and agreed to the published version of the manuscript.

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Conflicts of Interest: The authors declare no conflicts of interest.

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