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An Ultra-Low Power Fast Transient LDO with Dynamic Bias

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Abstract: A low-dropout linear regulator (LDO) without external capacitors is designed, combining ultra-low power consumption and ultra-fast transient response. The common support voltage of the LDO is 2.5 V to 3.6 V with a stable output voltage of 1.2 V and an output current dynamic range of 10 µA to 20 mA to supply power to other circuit modules. A Rail-to-Rail Input-Output (RRIO) Class AB push-pull output amplifier and a dynamic bias circuit are also designed. Meanwhile, a dynamic bias circuit which can regulate the operating current of error amplifier is proposed by monitoring output voltage variation in order to provide a larger compensation current to the operational amplifier when the load current changes are at high frequency and maintain ultra-low operating current at low clock frequency. The LDO is designed without resistors, and the deep well NMOS is applied in the output stage in order to reduce the difficulty of loop compensation. Designed in a 180 nm CMOS process, the post-simulation results show that under the condition of 40 °C and 3 V input voltage, the static power consumption is 31.7 nA with a settling time (±5%) of less than 35 ns.

Keywords: capacitor-less LDO; dynamic bias; fast transient response; low power

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1. Introduction

System on chip (SoC) and very large-scale integrated (VLSI) circuits need fully integrated power management units with high power efficiency and low design cost. Such power units are required to provide high-quality power supplies to integrated circuits with minimal power losses. Various topologies are able to satisfy different applications, such as linear regulator, dc-dc converters, etc. For analog circuits, a high power-supply-reject regulator is needed, while an ultra-fast transient response regulator is required in digital circuits [1,2]. Previous LDO have mainly focused on current efficiency by optimizing quiescent current. However, for low-voltage, high-performance digital circuits, the regulator needs to have both high power-supply-reject and fast transient response. To achieve fast transient response, many techniques have been proposed. A flipped voltage follower (FVF) is used to achieve a fast transient and low power consumption [3]. RC feed-back circuits, switching capacitor filters, and negative capacitor networks are used in [4–6] to obtain high power supply rejection at higher frequency. The design introduced in [7] can achieve high performance by sensing the load current and adding dynamic bias, a buffer stage, and differential detection of the input ripple. However, the structure is complicated, and additional structures are needed to ensure system stability.

Plenty of methods have been presented to achieve lower quiescent current. The LDO proposed in [8] uses bulk transconductance, g_{mb}, to achieve a quiescent current of 7 nA. Adaptive biasing and two cross-summed transconductance cells are described in [9], consuming only 25 nA with no load current. Based on a super source follower, an adaptive biasing scheme is used to measure the absolute voltage difference between the two inputs of the error amplifier and to modify the biasing current [10]. In this manuscript, a LDO that can measure changes in output ripple differentially with less current is proposed. Only when the output impedance changes at high operating speed is the dynamic bias required to provide a large current to meet the requirements of bandwidth and slew rate.

The rest of this manuscript is organized as follows. Section 2 shows the architecture of the proposed LDO. Section 3 introduces the circuit implementation and analyzes the small signal mode, system stability, and the system closed-loop bandwidth. The simulation results are given in Section 4. Finally, Section 5 presents the conclusions.

2. Proposed LDO Architecture

The basic structure of the LDO is shown in Figure 1. It consists of the dynamic current bias, the error amplifier, and the power transistor (as the power stage). A detailed description of the dynamic current bias and amplifier are presented in next section. The output stage, of which the substrate is directly connected to the source and used to provide the load current with its leakage, is composed of a deep-trench NMOS transistor. The gate of the power transistor is directly controlled by the operational amplifier to reduce the overshoot of the V_{out} by discharging quickly.

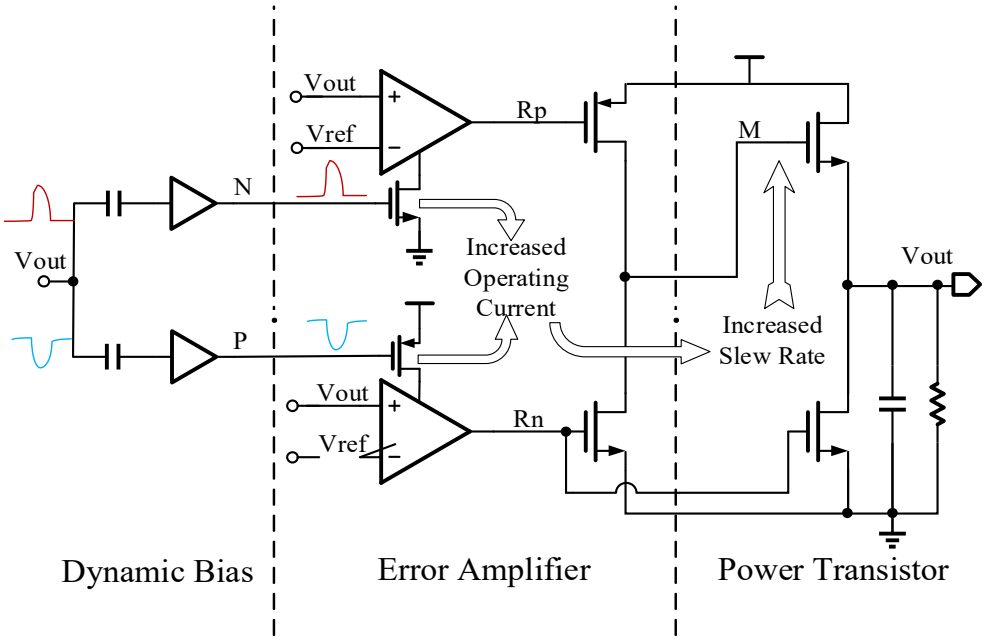


Figure 1. Basic Structure of the proposed LDO.

Generally, the best method to trade low power consumption for fast transient response is to sample the gate capacitance at the output pole and add current limiting resistance to ensure that the sampling current is kept within a small range. However, the static power consumption still increases with the load current. Based on the FVF structure, when the load is switched, the LDO uses the loop from the output end to the gate of the power transistor for feedback regulation. By dynamically adjusting the working current of the operational amplifier, this structure can greatly improve the bandwidth and gain to meet the requirement of a high transient response. The static power consumption will be irrelevant to the load current.

The LDO is fully integrated on-chip using MOS transistors for loop compensation instead of off-chip capacitors. Most transistors are designed in the same finger width to reduce process mismatches. The structure shows high reliability, since the overall process deviation is small, according to the corner simulation

3. Circuits Implementation of the Proposed Scheme

Figure 2 shows a detailed schematic of the LDO, including the differential dynamic current bias, the class AB complementary push-pull error amplifier, and the power stage.

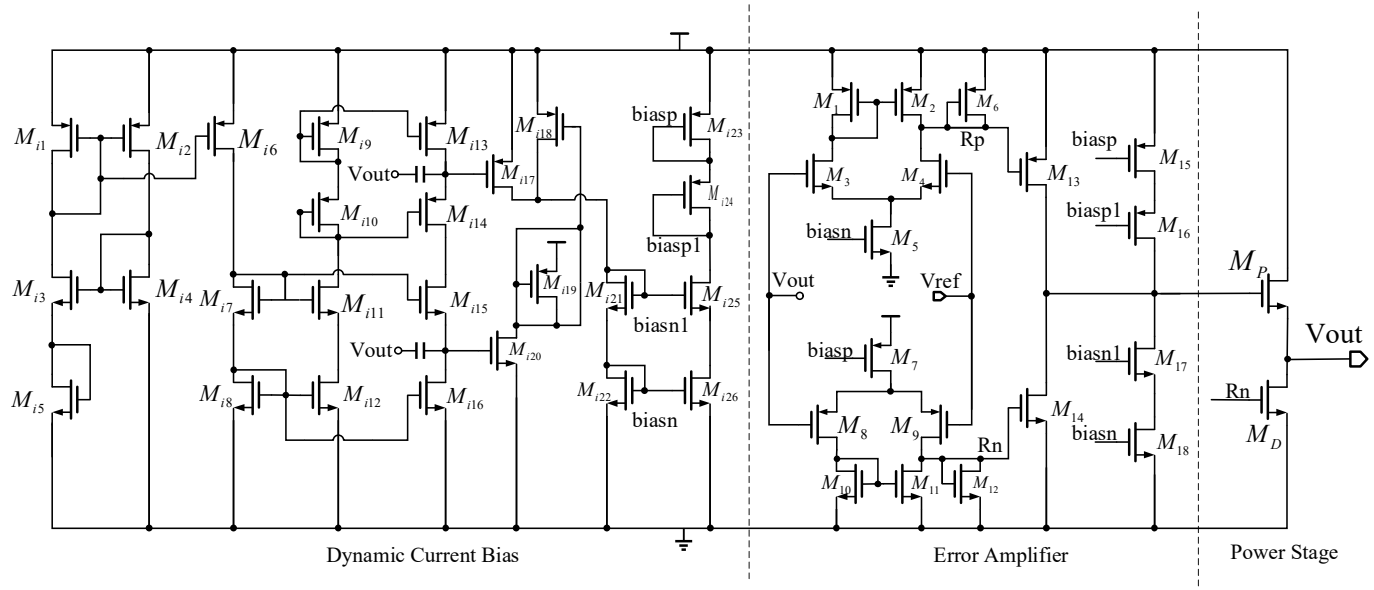


Figure 2. Schematic of the proposed LDO.

3.1. Stability Analysis of RRIO Amplifier

The amplifier is composed of an N-P complementary error amplifier, as shown in Figure 2. The second stage is composed of common source amplifier. Because of the complementary design, rail-to-rail input and output can be achieved. By introducing the internal mismatch of a differential pair, the common source amplifier has low power consumption. Compared with other RRIO amplifiers, its input stage structure is simpler. The internal poles of the amplifier are pushed to high frequencies through dynamic pole compensation with high stability in the loop.

Figure 3 shows the small signal model of the LDO structure. Taking the input and output impedance at all levels into account, an open-loop transfer function is given as Equation (1).

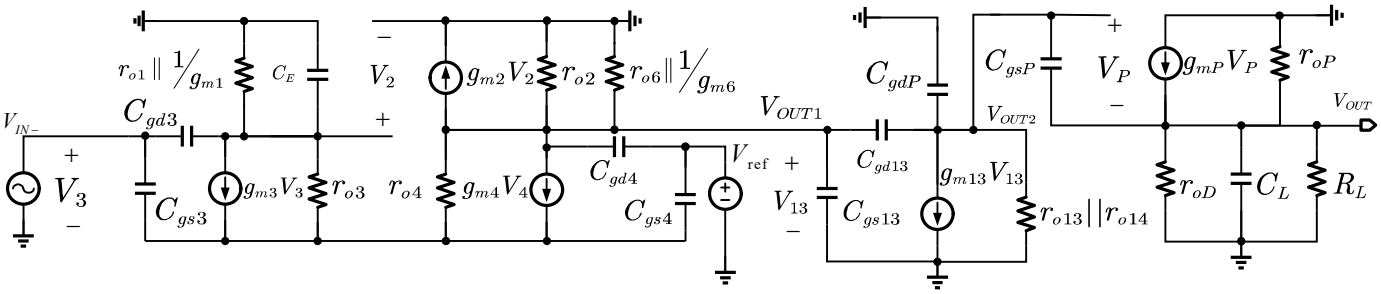


Figure 3. Small signal model.

$$\frac{V_{OUT}}{V_{IN-}} = \frac{g_{m2}(sC_{gd3}-g_{m3})}{[s(C_E+C_{gd3})+{}^{1}\!/_{r_{o3}}+{}^{1}\!/_{g_{m1}^{-1}\,\|\,r_{o1}}]\cdot[s(C_{gd2}+C_{gs13})+{}^{1}\!/_{r_{o4}}+{}^{1}\!/_{g_{m6}^{-1}\,\|\,r_{o6}}]} \cdot \frac{sC_{gd13}-g_{m13}}{s(C_{gdP}+C_{gd13})+{}^{1}\!/_{r_{o3}\,\|\,r_{o4}}} \cdot \frac{g_{mP}+sC_{gsP}}{s(C_{gsP}+C_L)+g_{mP}+{}^{1}\!/_{R_L\,\|\,r_{oP}\,\|\,r_{oD}}} \quad (1)$$

It is worth noting that in the first stage small signal model, a mismatch of M_1 and M_2 of about 3:4 to improve the static voltage of M_{out1} is introduced so that the second-stage amplifier works in a sub-threshold state in order to reduce current consumption. C_E is the ground capacitance of the gate of M_1 and M_2. Dynamic pole compensation is used at the output node of the first stage. M_6, connected in the form of diode, can dynamically reduce the output resistance of this stage with a change of output current for dynamic frequency

compensation. On this basis, the bandwidth of the operational amplifier is dynamically compensated for, according to the variation of the switching load of the proposed LDO, which is quite different from a conventional static compensation structure. As a result, the compensated operational amplifier has no low-frequency poles except in the power transistor grid and output stage. Therefore, it can be equivalent to a single-stage operational amplifier. The two poles of LDO are given in Equations (2) and (3).

$$P_1 \approx \frac{1}{2\pi C_{gdP} \cdot (r_{o13} \parallel r_{o14})} \tag{2}$$

$$P_2 \approx \frac{g_{mP} + \frac{1}{R_L \| r_{oP} \| r_{oD}}}{C_{gsP} + C_L} \tag{3}$$

In short, our new structure adopts mismatched transistors to compensate for the frequency response of the operational amplifier by reducing the output resistance, while the power stage uses the deep-trench NMOS transistor of the source follower structure as the output pole. The number of poles is reduced to the greatest extent. Regarding the stability of the loop, capacitance compensation is not required, which reduces the chip size.

3.2. Dynamic Bias

As the subthreshold bias part, M_{i1} to M_{i5} provide the basic current bias for the whole LDO to ensure that the circuit works in the subthreshold state when the output load remains unchanged. The gates of M_{i17} and M_{i20} sense changes in V_{OUT} through capacitance and provide a large compensation current when necessary. M_{i13} to M_{i16} have two functions: to provide the subthreshold gate voltage for M_{i17} and M_{i20} in steady state and to adjust the voltage across the detection capacitor in order to restore the bias voltage when V_{OUT} changes rapidly. If V_{OUT} overshoots due to load switching, the gate voltage of M_{i17} and M_{i20} also increases, because the voltage at both ends of the capacitor cannot change suddenly. V_{gs14} of M_{i14} increases while V_{gs15} of M_{i15} decreases, which can safeguard large resistance on this branch to reduce power consumption. The complementary structure of M_{i17} and M_{i20} can ensure the provision of a large compensation current, regardless of V_{OUT} overshoot or undervoltage.

3.3. Compensation Current

When V_{OUT} changes suddenly, a high-frequency current inflows from the detection capacitor, which can be given as (4):

$$i = C\frac{dVout}{dt} \tag{4}$$

If V_{OUT} undervoltage, the current inflows from the detection capacitor with an increase of current flowing through M_{i15} and a decrease of current flowing through M_{i14}, as shown in Figure 4, resulting in the generation of a large compensation current in M_{i17}, as shown in Figure 5a, which can increase the bandwidth of the operational amplifier. In another case, the compensation current generated by the M_{i20} is shown in Figure 5b when the load current drops.

I_{i20} is the subthreshold current when the system is in a static state. When V_{OUT} no longer changes, the gate voltage of M_{i17} and M_{i20} will slowly reset to the static working point. If the output changes frequently and V_{OUT} changes again before the gate voltage is completely reset, the bias will remain at a high static current level. This can strengthen the transient performance of LDO so as to realize adaptive adjustments to frequency of different loads, as shown in Figure 6.

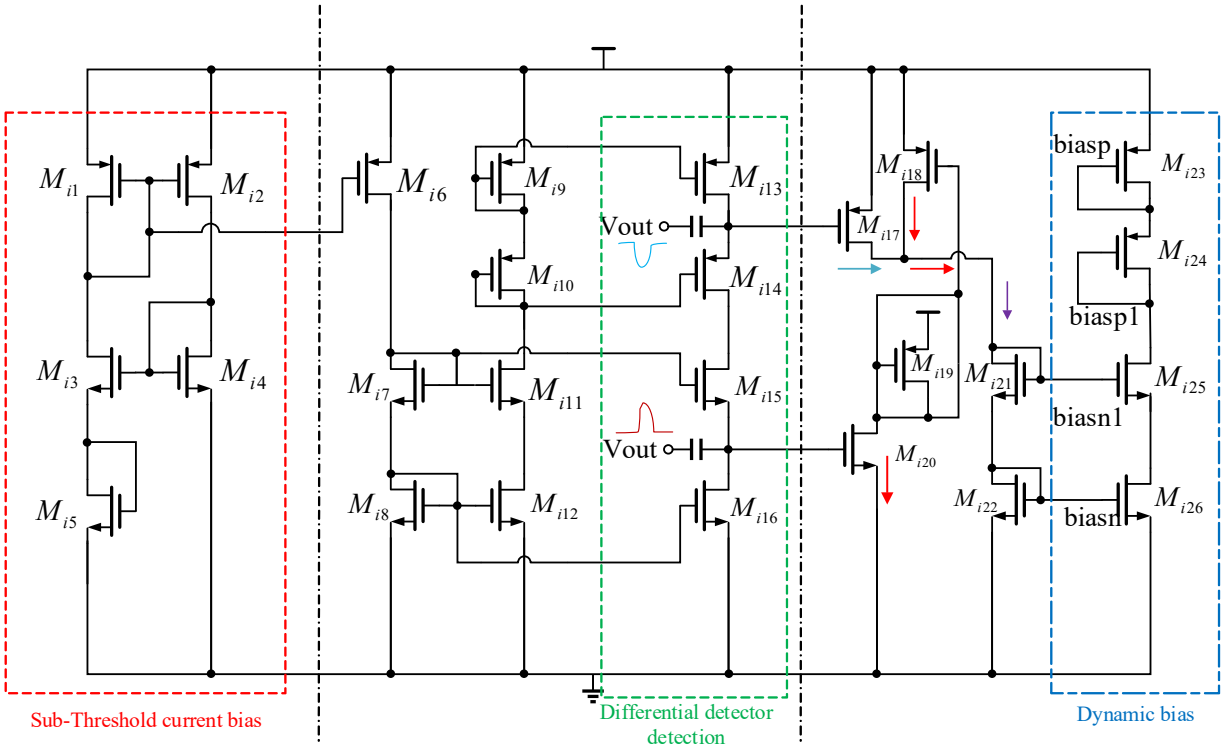


Figure 4. Bias structure.

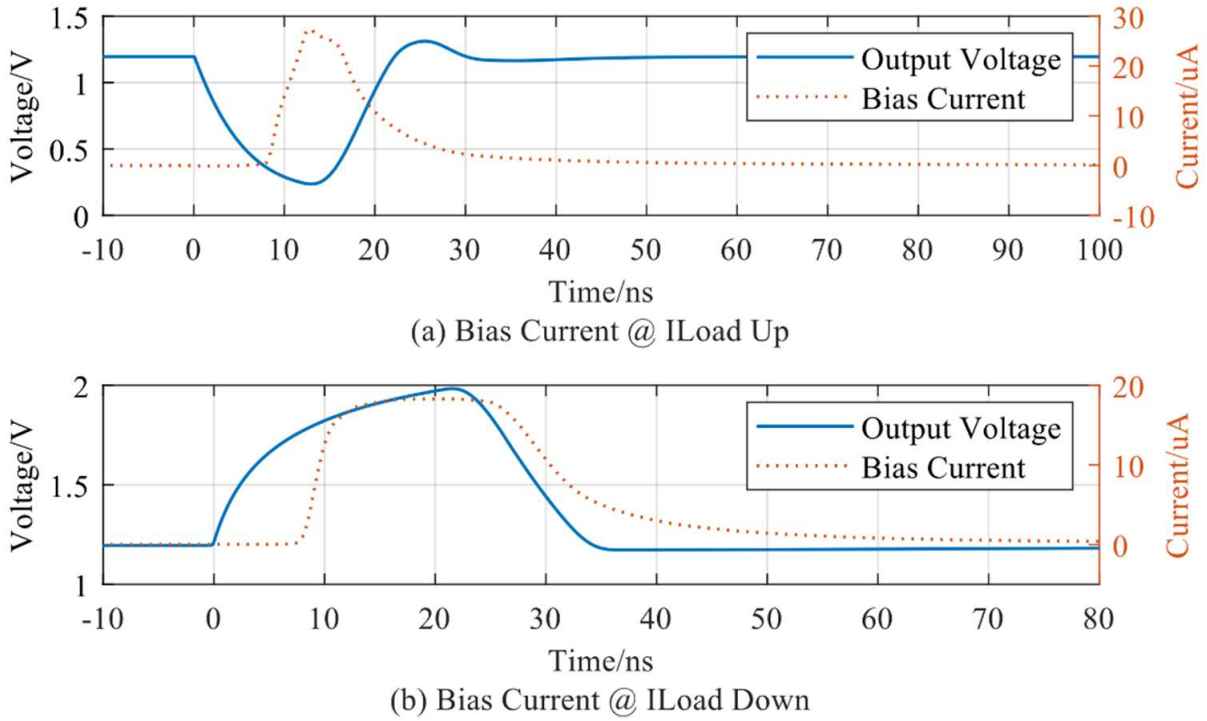


Figure 5. Transient bias response.

$$\Delta V_{GSi20} = \frac{C}{C + C_{GSi20}} \cdot \Delta V_{OUT} \approx \Delta V_{OUT} \qquad (C \gg C_{GSi20}) \tag{5}$$

$$\Delta I_{i20} = \frac{1}{2}\frac{W}{L}\mu C_{OX}(V_{GSi20} + \Delta V_{GSi20} - V_{TH})^2 - I_{i20} \tag{6}$$

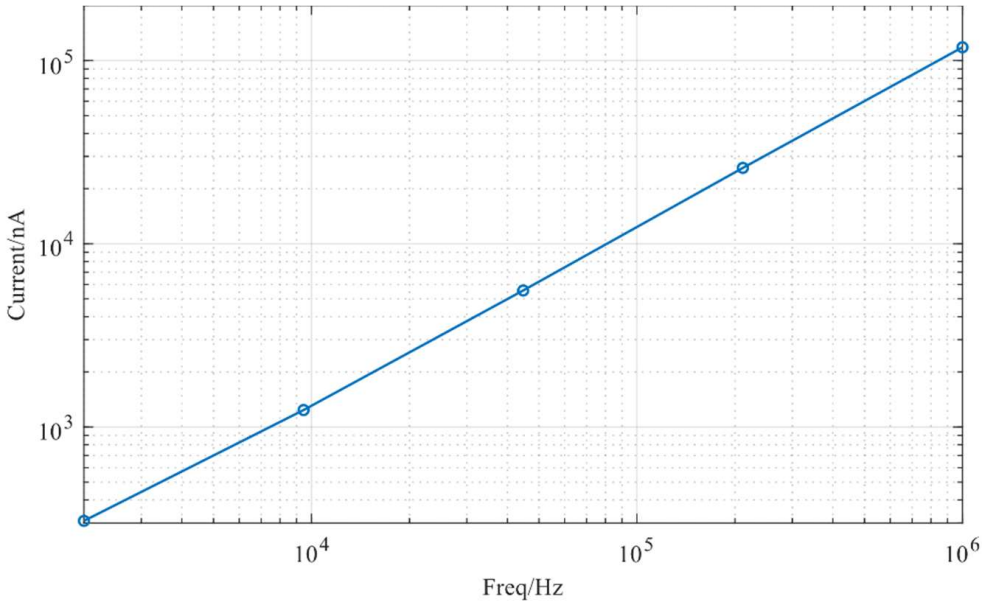


Figure 6. Current consumption vs. load switching frequency.

3.4. Transient Analysis

The maximum offset of undervoltage V_{dip} and the adjustment time of the system Δt_{dip} are determined by (7) and (8). The adjustment time mainly consists of large and small signal responses.

$$\begin{aligned} V_{dip} &= \left({}^{\Delta I_{OUT}}/_{2\pi C_L}\right) \cdot \Delta t_{dip} \\ \Delta t_{dip} &\approx {}^{1}/_{BW} + {}^{2\pi C_P \cdot \Delta V_P}/_{I_{SR+}} \end{aligned} \tag{7}$$

where C_P is the grid capacitance of power regulator, ΔI_{OUT} is the variation of load current, ΔV_P is the variation of the gate voltage that should be adjusted as required, I_{SR+} is the charging current, and BW is the closed loop bandwidth of the system.

In contrast, the maximum offset and adjustment time during system overshoot are as follows:

$$V_{peak} = \left({}^{\Delta I_{OUT}}/_{2\pi C_L}\right) \cdot \Delta t_{peak} \tag{8}$$

$$\Delta t_{peak} \approx {}^{1}/_{BW} + {}^{2\pi C_P \cdot \Delta V_P}/_{I_{SR-}} \tag{9}$$

Because there is no load capacitance of several μF outside the chip, the LDO module integrated inside the chip has a large degree of overshoot. To increase the transient response performance of the LDO, the closed-loop bandwidth and I_{SR} are often improved. The proposed dynamic bias structure can rapidly increase the closed-loop bandwidth and I_{SR} by detecting the change of output voltage in order to reduce the response time of the loop.

As is shown in Figure 7, when the dynamic compensation current increases the system instantaneous power of LDO to 10 μA, the closed-loop system has a unit gain bandwidth of nearly 86.89 MHz.

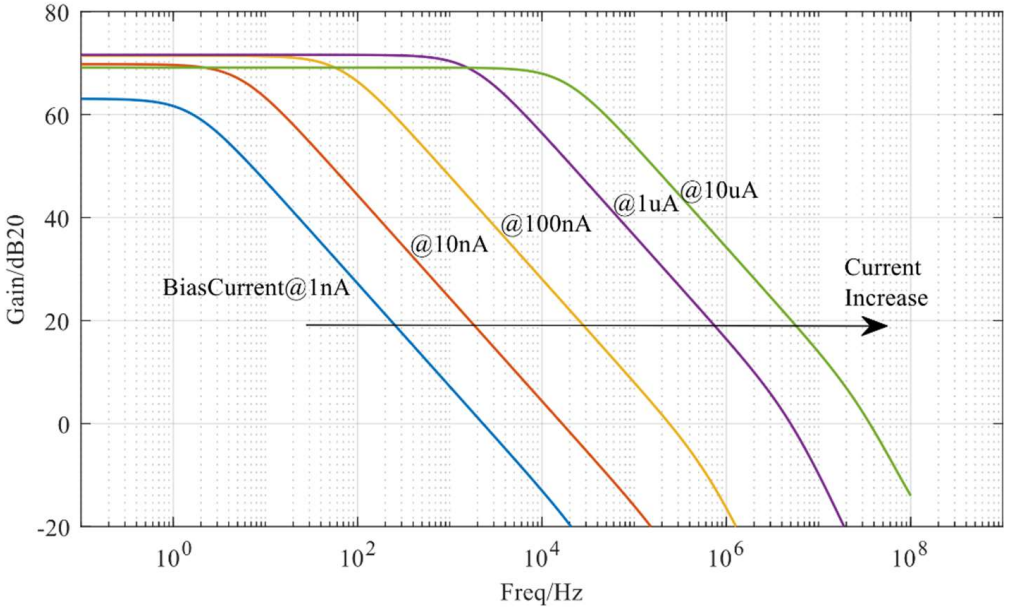


Figure 7. Dynamically increasing the closed-loop bandwidth.

When the load current is switched, the charging and discharging current of the power transistor will also increase with static power consumption. Figure 8 shows that the dynamic bias can gradually increase the Slew Rate from 1 V/µs to 100 V/µs in the transient response. The dynamic bias will slide the LDO system bandwidth and charging current in these curve clusters. The actual transient response results will be shown in the next section.

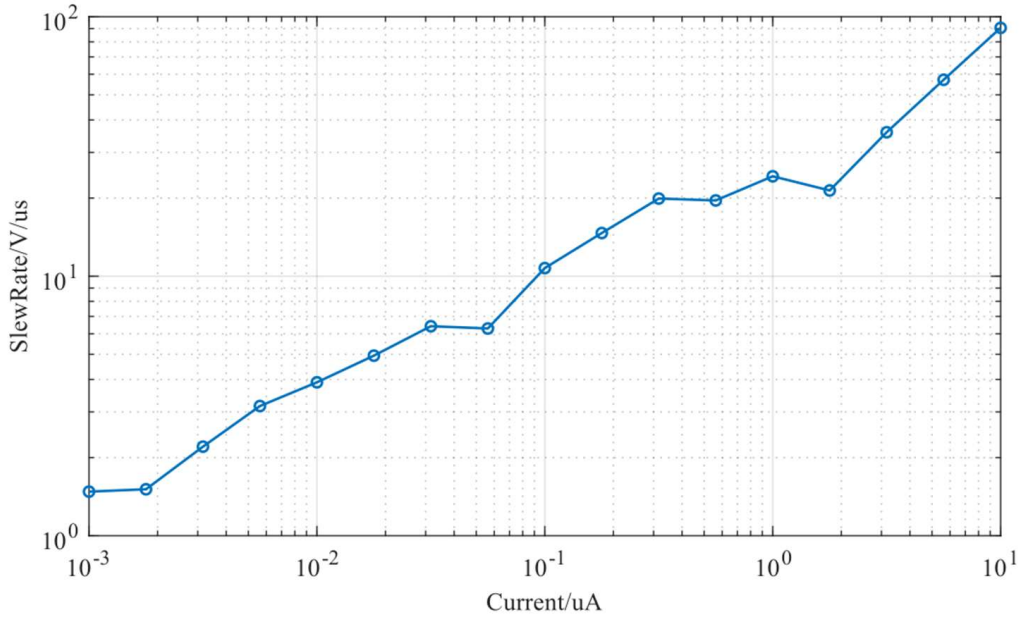


Figure 8. Dynamically increase the Slew Rate.

4. Simulation Results

The LDO is designed in a 180 nm CMOS process. The input voltage ranges from 2.5 V to 3.6 V while the output voltage is set to 1.2 V. Figure 9 shows that in the standard state (TT, 3.0 V, 40 °C), the static current is 32 nA. Considering the process corner deviation, the maximum current is 128 nA (FF, 3.6 V, 125 °C).

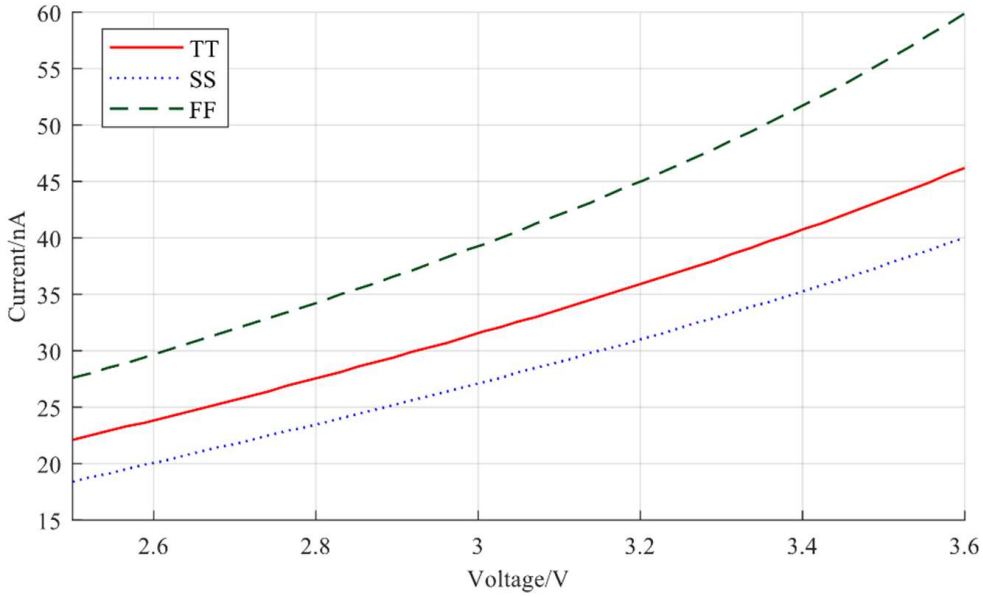


Figure 9. Quiescent current vs. Input Voltage.

With a 100 pF load capacitance, it takes 32.769 ns for the output voltage to reach 1.2 V (±5%) when the load current drops, as is shown in Figure 10a. When the load current rises, it takes 28.389 ns for the output voltage to reach 1.2 V (±5%), as is shown in Figure 10b.

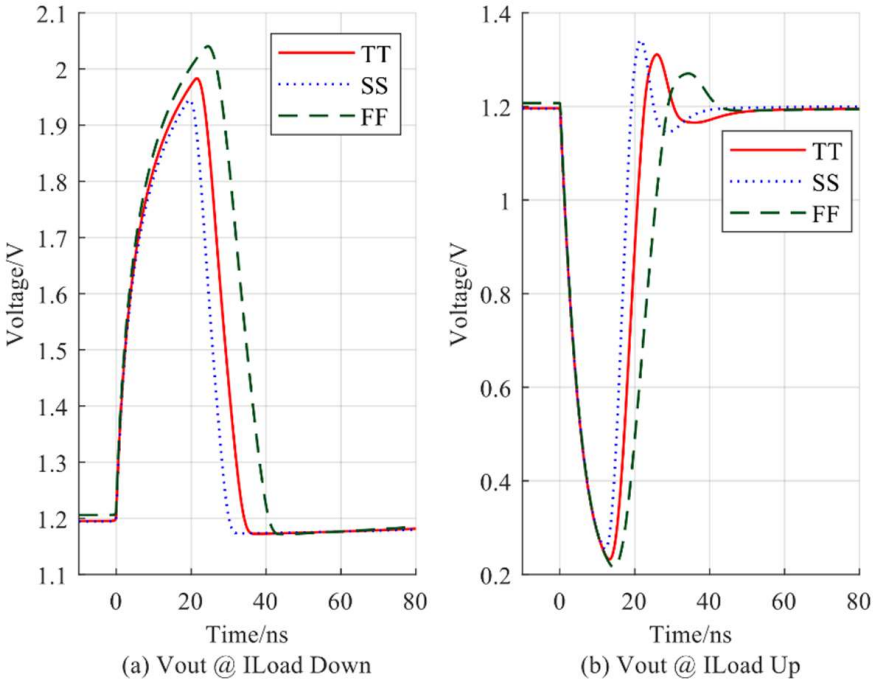


Figure 10. Transient Response.

Supply voltage regulation and load regulation are shown in Figure 11a and Figure 11b, respectively. The worst power supply voltage adjustment rate under the standard state is 0.61 mV/V, while the load regulation rate is less than ±0.4%.

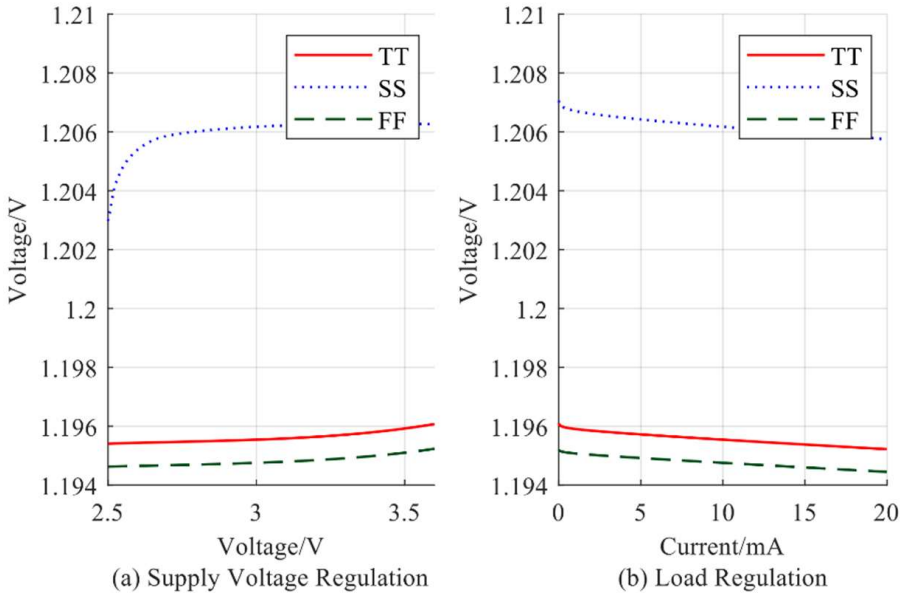


Figure 11. Supply voltage regulation and load regulation.

The simulated power supply rejection ratio and phase margin versus current are shown in Figure 12a and Figure 12b, respectively. The minimum phase margin is 73° at all corners. In the case of TT, it generally has power ripple suppression of more than 60 dB. However, in the case of SS, the current of the class AB complementary operational amplifier is reduced, which leads to an increase of offset voltage of the differential pair.

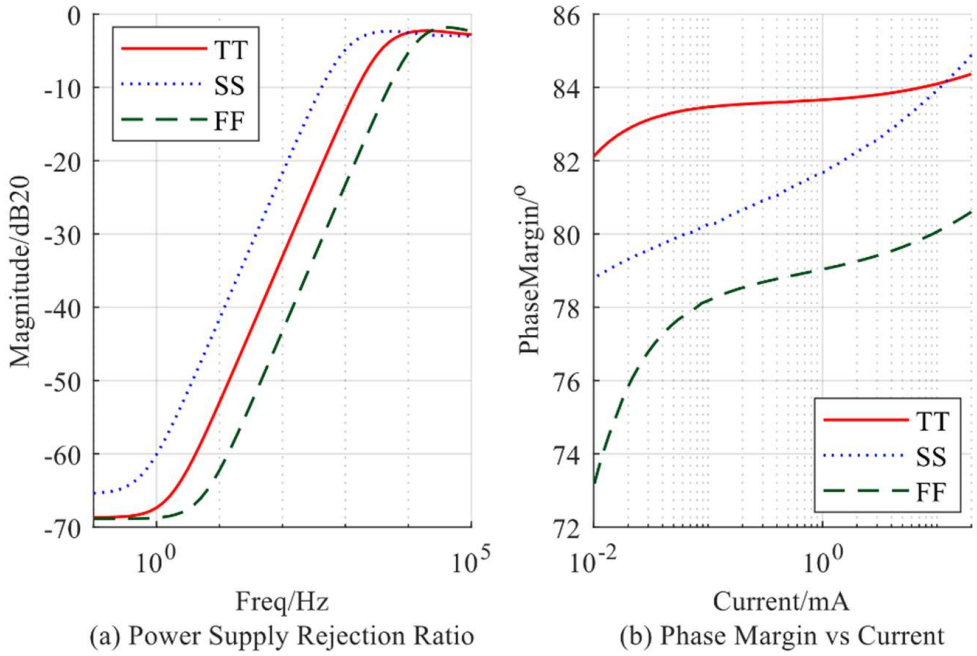


Figure 12. Power Supply Rejection Ratio and Phase Margin vs. Current.

Table 1 shows a performance comparison with other simulated LDOs. Two figures of merit (FOM) have been applied for comparison. The proposed design obtained an FOM of 7.79 fs, as calculated by Equation (10). Considering the relationships between the transient

response and the current utilization, FOMt is defined using Equation (11). This work achieved a better compromise between these two FOM than the other listed designs.

$$FOM = \frac{C_{TOTAL} \times \Delta V_{OUT} \times I_Q}{\Delta {I_{LOAD}}^2} \tag{10}$$

$$FOMt = \frac{T_{edge} \times \Delta V_{OUT} \times I_Q}{\Delta I_{LOAD}} \tag{11}$$

Table 1. Comparison of state-of-the-art low-power LDOs.

Reference	[9]	[11]	[12]	[13]	[14]	This Work
Year	2021	2021	2021	2020	2016	2022
Technology (nm)	65 nm	55 nm	130 nm	40 nm	40 nm	180 nm
IL (mA)	0.2–20	0–10	1–20	0–100	0.01–0.4	0.01–20
T_{edge} (ns)	10	100	1000	300	1	1
CL_{max} (pF)	100	20	100	100	80	100
I_Q (nA)	25	1000	7200	220	25,000	31.7
VIN (V)	1.4–4.2	0.9–1.3	2.5–3.6	1.1	1.5–2	2.5–3.6
VOUT (V)	1.2–3.0	0.8–1.2	1.2	0.9	1.18	1.2
△VOUT (mV)	240	438	97	292	15	960
DC Load Reg	31 mV/mA	-	11.05 µV/mA	37 µV/mA	25 mV/mA	50 µV/mA
DC Line Reg (mV/V)	0.01@Vout = 2.5	-	-	4.8	1	0.6096
PSRR (dB)	-	-	-	32.12@1 MHz	43@10 MHz	53@10 Hz
FOM	0.35 fs	53.6 fs	174 fs	0.6424 fs	187.5 ps	7.79 fs
FOMt	84 fs·V	2385.2 fs·V	52.38 ps·V	192.72 fs·V	0.9375 ps·V	49.86 fs·V

5. Conclusions

This paper proposes an ultra-low power LDO with a 100 pF loading capacitance and a 20 mA output current in a CMOS 180 nm process. The dynamic bias achieved a quiescent current of only 32 nA in standby mode and increased the operating current adaptively when the frequency of load changes increased. In addition, this paper tested the power supply voltage regulation and load regulation rates at process corners and temperatures under extremely low power consumption; the error range was less than 1%. Further, the transient response of the regulator can be improved without considering power consumption. The proposed LDO with low quiescent current can also be widely used as a power supply for the Internet of Things (IoT) and wearable or implantable devices for biomedical applications.

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Conflicts of Interest: The authors declare no conflict of interest.

References

1. Cheah, M.; Mandal, D.; Bakkaloglu, B.; Kiaei, S. A 100-mA, 99.11% Current Efficiency, 2-mV_{pp} Ripple Digitally Controlled LDO with Active Ripple Suppression. *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.* **2017**, *25*, 696–704. [CrossRef]
2. Huang, M.; Lu, Y.; Seng-Pan, U.; Martins, R.P. An Analog-Assisted Tri-Loop Digital Low-Dropout Regulator. *IEEE J. Solid-State Circuits* **2018**, *53*, 20–34. [CrossRef]
3. Ma, X.; Lu, Y.; Li, Q. A Fully Integrated LDO With 50-mV Dropout for Power Efficiency Optimization. *IEEE Trans. Circuits Syst. II Express Briefs* **2020**, *67*, 725–729. [CrossRef]
4. Lavalle-Aviles, F.; Torres, J.; Sanchez-Sinencio, E. A High Power Supply Rejection and Fast Settling Time Capacitor-Less LDO. *IEEE Trans. Power Electron.* **2019**, *34*, 474–484. [CrossRef]
5. Magod, R.; Suda, N.; Ivanov, V.; Balasingam, R.; Bakkaloglu, B. A Low-Noise Output Capacitorless Low-Dropout Regulator With a Switched-RC Bandgap Reference. *IEEE Trans. Power Electron.* **2017**, *32*, 2856–2864. [CrossRef]
6. Yun, S.J.; Yun, J.S.; Kim, Y.S. Capless LDO Regulator Achieving −76 dB PSR and 96.3 fs FOM. *IEEE Trans. Circuits Syst. II Express Briefs* **2017**, *64*, 1147–1151. [CrossRef]
7. Duong, Q.-H.; Nguyen, H.-H.; Kong, J.-W.; Shin, H.-S.; Ko, Y.-S.; Yu, H.-Y.; Lee, Y.-H.; Bea, C.-H.; Park, H.-J. Multiple-Loop Design Technique for High-Performance Low-Dropout Regulator. *IEEE J. Solid-State Circuits* **2017**, *52*, 2533–2549. [CrossRef]
8. Pereira-Rial, O.; Lopez, P.; Carrillo, J.M. 0.6-V-V_{IN} 7.0-nA-I_Q 0.75-mA-I_L CMOS Capacitor-Less LDO for Low-Voltage Micro-Energy-Harvested Supplies. *IEEE Trans. Circuits Syst. I Regul. Pap.* **2022**, *69*, 599–608. [CrossRef]
9. Liu, N.; Guo, J. A 25nA I_Q, 20mA I_{LOAD} OCL-LDO for Battery-Powered IoT Devices. In Proceedings of the 2021 IEEE International Conference on Integrated Circuits, Technologies and Applications (ICTA), Zhuhai, China, 24–26 November 2021; pp. 187–188. [CrossRef]
10. Pereira-Rial, O.; Lopez, P.; Carrillo, J.M.; Brea, V.M.; Cabello, D. An 11 mA Capacitor-Less LDO With 3.08 nA Quiescent Current and SSF-Based Adaptive Biasing. *IEEE Trans. Circuits Syst. II Express Briefs* **2021**, *69*, 844–848. [CrossRef]
11. Chen, W.; Chen, M.; Hao, Y.; Qi, L.; Zhao, J. A 1-µA-Quiescent-Current Capacitor-Less LDO Regulator with Adaptive Embedded Slew-Rate Enhancement Circuit. In Proceedings of the 2021 IEEE International Symposium on Circuits and Systems (ISCAS), Daegu, Korea, 22–28 May 2021; pp. 1–5. [CrossRef]
12. Tang, J.; Ouyang, L.; Dai, C.; Wang, Y.; Zou, W. A Low-Power Fast-Transient Output-Capacitorless LDO. In Proceedings of the 2021 9th International Symposium on Next Generation Electronics (ISNE), Changsha, China, 9–11 July 2021; pp. 1–4. [CrossRef]
13. Sudan, R.B.; Karsilayan, A.I. A 220-nA Quiescent Current Capacitor-Less Low-Dropout Regulator with Improved Recovery Time. In Proceedings of the 2020 IEEE 63rd International Midwest Symposium on Circuits and Systems (MWSCAS), Springfield, MA, USA, 9–12 August 2020; pp. 994–997. [CrossRef]
14. Wang, L.; Mao, W.; Wu, C.; Chang, A.; Lian, Y. A fast transient LDO based on dual loop FVF with high PSRR. In Proceedings of the 2016 IEEE Asia Pacific Conference on Circuits and Systems (APCCAS), Jeju, Korea, 25–28 October 2016; pp. 99–102. [CrossRef]