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Research on Bidirectional Isolated Charging System Based on Resonant Converter

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Abstract: This paper proposes a two-stage bidirectional isolated charging system, which can realize the bidirectional flow of electric energy, not only making the electric energy flow from the grid side to the battery side but also converting the battery's energy into single-phase alternating current to supply other electric equipment. The charging system also has the function of power factor correction and wide-range voltage output. The front stage of the charging system is a bidirectional totem pole structure power factor correction converter with a voltage and current double closed-loop control strategy to ensure the stability of the DC bus voltage, and the rear stage is a bidirectional CLLLC resonant converter, which adopts a high-frequency soft start strategy to reduce the inrush current during start-up and ensure the safe operation of the converter. Moreover, the frequency control strategy is used to make it have a wide range of DC output characteristics. In this paper, the principle analysis and parameter calculation of the charging system is carried out, the simulation platform and hardware circuit design are built, and a test prototype is piloted to verify the bidirectional operating characteristics of the charging system. The simulation and experimental results demonstrate the correctness of the theoretical analysis and topology design.

Keywords: bidirectional charging system; totem pole converter; bidirectional CLLLC resonant converter; double closed-loop control

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1. Introduction

With the development of the economy and the increase of social demand, new energy electric vehicles are one of the important means to alleviate the shortage of oil energy, environmental pollution, and the development trend to replace fuel cars [1,2]. While electric vehicles are attracting attention, on-board charging technology is also developing rapidly and is generally divided into unidirectional vehicle chargers and bidirectional vehicle chargers. Compared with the single function of unidirectional vehicle charger, which can only transfer energy from the grid to the vehicle battery, the bidirectional vehicle charger also allows the vehicle battery to provide energy to the outside, and it is the core equipment in V2X technology. The bidirectional vehicle charger can also be used as an emergency power source for the family during power outages, and the research into this device is beneficial to the development of a variety of disciplines.

A bidirectional charging system is a device that uses conduction to convert AC power to DC power to charge a battery. Its commonly used two-stage power architecture is shown in Figure 1. The bidirectional charger is capable of the bidirectional flow of energy between the grid and the battery, with a bidirectional AC/DC converter in the front stage, which can achieve power factor correction, reduce harmonic content, and output a stable bus voltage; and a bidirectional isolated DC/DC converter in the backstage, which can output a wide range of DC voltages with low pulsation ripple [3,4].

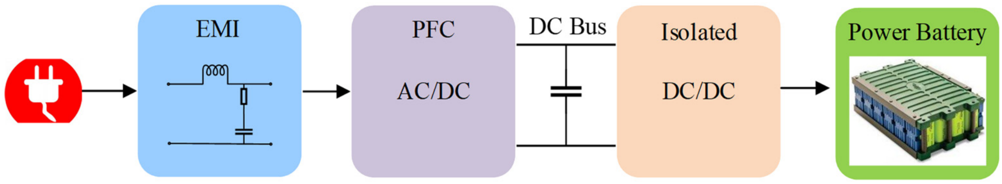

Figure 1. The two-stage architecture of a vehicle charger.

Bidirectional AC/DC converters are often used as system pre-stages with either a half-bridge structure or a full-bridge structure. The half-bridge structure requires fewer devices and is easy to control, but the switching transistor voltage and current stress are high, and the efficiency is low. An improved single-cycle controlled bidirectional half-bridge AC/DC converter is proposed in [5], capable of stable operation in rectifier and inverter modes with a high power factor, but it has high reactive power losses and low efficiency. The full-bridge AC/DC converter is more widely used than the half-bridge structure. In [6], a full-bridge AC/DC converter considering inductor resistance and conduction voltage is proposed with a single-loop bidirectional current sensor-free control strategy, which reduces the number of sensors and can regulate the voltage of the household DC grid. An interleaved parallel structure has also been derived from the bridge structure. [7] proposes a bidirectional interleaved parallel AC/DC converter with no auxiliary circuit and a TCM mode soft-switching strategy. This topology can effectively reduce losses and improve the overall system efficiency, but it adds difficulty to the control system design. To improve the efficiency and reduce the switching losses, a segmented synchronous control strategy based on zero-vector embedding is proposed in [8] to ensure good input-output performance. Ref. [9] proposes an improved space vector pulse width modulation strategy to enhance the system's reliability, but its main circuit structure and control circuit are complex, with more switching elements and higher stress on the switching transistors. Ref. [10] proposes a control strategy that can govern AC bus harmonic currents to ensure that the microgrid has good power quality, but still cannot solve the problem of large turn-off losses. Ref. [11] proposes a diode-clamped three-level AC/DC converter with a composite control strategy combining PI control based on a rotating coordinate system and T/2 period repetition control to ensure dynamic performance and improve steady-state accuracy. However, the structure requires more power switching transistors, and the midpoint potential of the DC bus is prone to imbalance. Ref. [12] proposes a bidirectional isolated AC/DC matrix converter that can be suitable for bidirectional power flow with minimal high harmonics; however, the large number of power devices makes it require more circuit cost and makes it difficult to control. Combining the advantages of fewer switching devices, high power density, and significant common-mode interference capability, the bidirectional totem pole converter is widely used.

Bidirectional isolated DC/DC converters as systems backstage are usually classified into non-resonant or resonant topologies. The typical non-resonant topology is a dual active bridge converter (DAB) [13,14], which is easy to control and can achieve zero voltage switching (ZVS). When the switch transistor is turned off, however, the current flowing through is larger, the converter shutdown loss is larger, and the current harmonics flowing through the high frequency transformer are larger, which also increases transformer losses and reduces efficiency [15]. To achieve soft switching and improve efficiency, resonant converters are widely used and have been gradually developed from LC series-parallel structures to LLC [16,17], CLLC [18,19], and CLLLC [20,21] structures. The bidirectional LLC resonant converter can achieve ZVS and Zero Current Switching (ZCS) in forward operation, i.e., battery charging. The voltage gain, however, is less than 1 in the reverse operation, i.e., battery discharging, and soft switching cannot be achieved. Refs. [22,23] propose an inverter-phase shift control method to meet the gain requirement for reverse operation and achieve full-range soft switching under such control. Ref. [24] proposes a half-bridge three-level bidirectional LLC resonant converter with a three-stage hybrid control strategy combining "frequency, phase shift, and frequency burst" control methods to achieve high efficiency and wide-range voltage output. However, it is prone to inrush current and long commutation time during switching control. The bidirectional CLLC resonant converter is composed by adding a resonant capacitor to the secondary side of the resonant network and has similar characteristics to the LLC resonant converter in forward and reverse operation. A fixed-bus scheme is proposed in [25] for parameter design optimization, but the asymmetric resonant cavity structure and high coupling degree of the bidirectional CLLC resonant converter make the difference between forward and reverse operating characteristics relatively large and difficult to control. Compared with the bidirectional CLLC resonant converter, the bidirectional CLLLC resonant converter is a set of LC series resonant structures added on the secondary side, with symmetrical structure, consistent forward and reverse characteristics, low coupling degree, and easy control.

For the requirements of high efficiency and wide range, this paper proposes a two-stage isolated vehicle charger with a bidirectional totem pole structure in the front stage, which can realize power factor correction and provide stable bus voltage for the rear stage, and a bidirectional CLLLC resonant converter in the rear stage, which inherits the characteristics of the traditional LLC resonant converter such as wide range, soft switching, and high power density. The resonant network is symmetrical with identical forward and reverse operation characteristics to realize bidirectional boost conversion. Through the parameter design and characteristic analysis, the power components can realize full-range soft switching under full load and improve the system efficiency.

2. Bidirectional Isolation Type Charging System and Characterization

The main circuit topology of the two-stage bidirectional charging system designed in this paper is shown in Figure 2. The front stage is a bidirectional totem pole converter with a full bridge structure, and the rear stage is a bidirectional CLLLC resonant converter. This converter has a symmetrical structure with the same operating characteristics in forward and reverse operation, which has high efficiency.

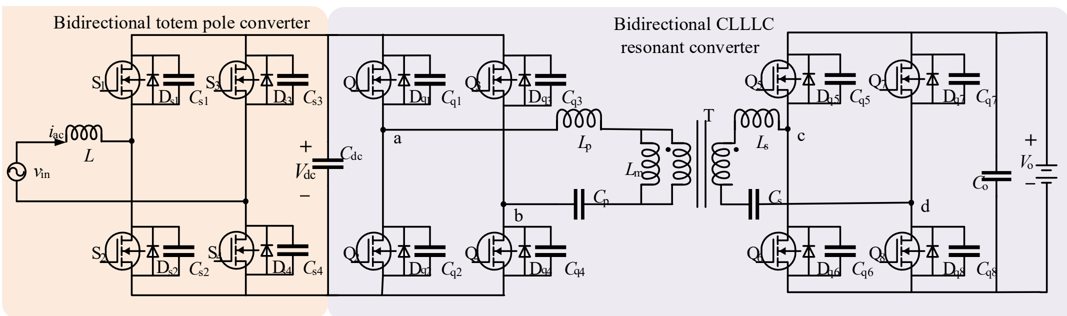

Figure 2. Main topology of the charging system.

During forward charging, the bidirectional totem pole converter achieves power factor correction and outputs a stable DC bus voltage V_{dc}. Power switches Q_1~Q_4 obtain drive signals to invert the DC voltage V_{dc}, Q_5~Q_8 pulse blocking, and body diodes D_{q5}~D_{q8} conduct work to rectify the high-frequency signal on the secondary side of the transformer.

During reverse discharging, the power switch Q_5~Q_8 inverts the DC power into a high-frequency AC signal, Q_1~Q_4 pulse blocking, and the body diode D_{q1}~D_{q4} completes the rectification function. Then the bidirectional totem pole converter achieves the inverter supply AC load power.

2.1. Modeling Analysis of Bidirectional Totem Pole Converter

For example, a bidirectional totem pole converter operating in forward charging mode and the grid voltage in the positive half cycle can be divided into two modes according to the on and off of the switching transistors. Its equivalent circuit is shown in Figure 3.

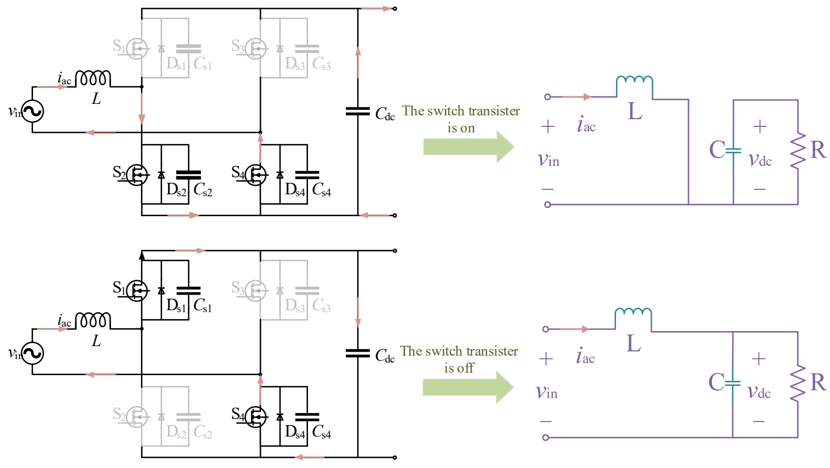

Figure 3. Forward equivalent circuit of bidirectional totem pole.

The matrix form of the equation of state when the switching transistor is on is:

$$\begin{bmatrix} \dot{i}_{ac}(t) \\ \dot{v}_{dc}(t) \end{bmatrix} = \begin{bmatrix} 0 & 0 \\ 0 & -\frac{1}{RC_{dc}} \end{bmatrix} \begin{bmatrix} i_{ac}(t) \\ v_{dc}(t) \end{bmatrix} + \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} [v_{in}(t)] \tag{1}$$

where i_{ac}(t) is the AC current; v_{dc}(t) is the DC bus voltage; R is the equivalent resistance of the rear stage converter; C_{dc} is the DC bus capacitance; L is the AC inductance; v_{in}(t) is the grid voltage.

The coefficient matrix can be obtained as:

$$\boldsymbol{A_0} = \begin{bmatrix} 0 & 0 \\ 0 & -\frac{1}{RC_{dc}} \end{bmatrix}, \boldsymbol{B_0} = \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} \tag{2}$$

The matrix form of the equation of state when the switching transistor is turned off is:

$$\begin{bmatrix} \dot{i}_{ac}(t) \\ \dot{v}_{dc}(t) \end{bmatrix} = \begin{bmatrix} 0 & \frac{1}{L} \\ \frac{1}{C_{dc}} & -\frac{1}{RC_{dc}} \end{bmatrix} \begin{bmatrix} i_{ac}(t) \\ v_{dc}(t) \end{bmatrix} + \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} [v_{in}(t)] \tag{3}$$

The coefficient matrix can be obtained as:

$$\boldsymbol{A_1} = \begin{bmatrix} 0 & -\frac{1}{L} \\ \frac{1}{C_{dc}} & -\frac{1}{RC_{dc}} \end{bmatrix}, \boldsymbol{B_1} = \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} \tag{4}$$

where $\boldsymbol{A_0}$, $\boldsymbol{B_0}$, $\boldsymbol{A_1}$, $\boldsymbol{B_1}$ are state coefficients.

Let the state vector x(t) = [i_{ac}(t) v_{dc}(t)]^T and the input vector u(t) = [v_{in}(t)], the steady-state expressions of the state vector and the input vector for the whole switching period T can be obtained by combining Equations (1)–(4) as follows:

$$\dot{\boldsymbol{x}} = [d\boldsymbol{A_0} + (1-d)\boldsymbol{A_1}]\boldsymbol{x} + [d\boldsymbol{B_0} + (1-d)\boldsymbol{B_1}]\boldsymbol{u} \quad 0 \le t \le T \tag{5}$$

where d is the duty cycle.

The equation of state coefficients are:

$$\begin{cases} \boldsymbol{A} = d\boldsymbol{A_0} + (1-d)\boldsymbol{A_1} = \begin{bmatrix} 0 & -\frac{1-d}{L} \\ \frac{1-d}{C_{\text{dc}}} & -\frac{1}{RC_{\text{dc}}} \end{bmatrix} \\ \boldsymbol{B} = d\boldsymbol{B_0} + (1-d)\boldsymbol{B_1} = \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} \end{cases} \tag{6}$$

Add a perturbation to the steady-state Equation (5) such that:

$$\begin{cases} \boldsymbol{x} = \boldsymbol{X} + \hat{\boldsymbol{x}} \\ \boldsymbol{u} = \boldsymbol{U} + \hat{\boldsymbol{u}} \\ d = D + \hat{d} \end{cases} \tag{7}$$

where $\boldsymbol{X}$, $\boldsymbol{U}$, and $\boldsymbol{D}$ are the steady-state values of the state vector, input vector, and duty cycle, respectively.

Substituting Equation (7) into Equation (5), we get:

$$\begin{aligned} \dot{\boldsymbol{X}} + \dot{\hat{\boldsymbol{x}}} = \; & [(D+\hat{d})\boldsymbol{A_0} + (1-D-\hat{d})\boldsymbol{A_1}](\boldsymbol{X}+\hat{\boldsymbol{x}}) + \\ & [(D+\hat{d})\boldsymbol{B_0} + (1-D-\hat{d})\boldsymbol{B_1}](\boldsymbol{U}+\hat{\boldsymbol{u}}) \end{aligned} \tag{8}$$

Neglecting the higher-order terms, Equation (8) can be decomposed into the steady state equation and the perturbation equation as Equations (9) and (10), respectively:

$$\dot{\boldsymbol{X}} = [D\boldsymbol{A_0} + (1-D)\boldsymbol{A_1}]\boldsymbol{X} + [D\boldsymbol{B_0} + (1-D)\boldsymbol{B_1}]\boldsymbol{U} \tag{9}$$

$$\begin{aligned} \dot{\hat{\boldsymbol{x}}} = \; & [D\boldsymbol{A_0} + (1-D)\boldsymbol{A_1}]\hat{\boldsymbol{x}} + [D\boldsymbol{B_0} + (1-D)\boldsymbol{B_1}]\hat{\boldsymbol{u}} + \\ & [\boldsymbol{X}(\boldsymbol{A_0}-\boldsymbol{A_1}) + \boldsymbol{U}(\boldsymbol{B_0}-\boldsymbol{B_1})]\hat{d} + \\ & (\boldsymbol{A_0}-\boldsymbol{A_1})\hat{d}\hat{\boldsymbol{x}} + (\boldsymbol{B_0}-\boldsymbol{B_1})\hat{d}\hat{\boldsymbol{u}} \end{aligned} \tag{10}$$

Assume that the quadratic term of the small signal is much smaller than the remaining terms, i.e.,:

$$\begin{aligned} & \left|(\boldsymbol{A_0}-\boldsymbol{A_1})\hat{d}\hat{\boldsymbol{x}} + (\boldsymbol{B_0}-\boldsymbol{B_1})\hat{d}\hat{\boldsymbol{u}}\right| \ll \Big|[D\boldsymbol{A_0} + (1-D)\boldsymbol{A_1}]\hat{\boldsymbol{x}} + \\ & [D\boldsymbol{B_0} + (1-D)\boldsymbol{B_1}]\hat{\boldsymbol{u}} + [\boldsymbol{X}(\boldsymbol{A_0}-\boldsymbol{A_1}) + \boldsymbol{U}(\boldsymbol{B_0}-\boldsymbol{B_1})]\hat{d}\Big| \end{aligned} \tag{11}$$

From this, neglecting the AC small signal product term in Equation (10), it is obtained that:

$$\dot{\hat{\boldsymbol{x}}} = \boldsymbol{A}\hat{\boldsymbol{x}} + \boldsymbol{B}\hat{\boldsymbol{u}} + [\boldsymbol{X}(\boldsymbol{A_0}-\boldsymbol{A_1}) + \boldsymbol{U}(\boldsymbol{B_0}-\boldsymbol{B_1})]\hat{d} \tag{12}$$

Converting the time domain Equation (12) to the frequency domain equation yields:

$$s\hat{\boldsymbol{x}}(s) = \boldsymbol{A}\hat{\boldsymbol{x}}(s) + \boldsymbol{B}\hat{\boldsymbol{u}}(s) + [\boldsymbol{X}(\boldsymbol{A_0}-\boldsymbol{A_1}) + \boldsymbol{U}(\boldsymbol{B_0}-\boldsymbol{B_1})]\hat{d}(s) \tag{13}$$

And then we can get:

$$\hat{\boldsymbol{x}}(s) = (s\boldsymbol{I}-\boldsymbol{A})^{-1}\boldsymbol{B}\hat{\boldsymbol{u}}(s) + (s\boldsymbol{I}-\boldsymbol{A})^{-1} \cdot [\boldsymbol{X}(\boldsymbol{A_0}-\boldsymbol{A_1}) + \boldsymbol{U}(\boldsymbol{B_0}-\boldsymbol{B_1})]\hat{d}(s) \tag{14}$$

where $\boldsymbol{I}$ is the unit matrix.

Substituting Equations (2), (4) and (6) into Equation (14), we get:

$$\begin{bmatrix} \hat{i}_{\mathrm{ac}}(s) \\ \hat{v}_{\mathrm{dc}}(s) \end{bmatrix} = \begin{bmatrix} s & \frac{1-D}{L} \\ -\frac{1-D}{C_{\mathrm{dc}}} & s+\frac{1}{RC_{\mathrm{dc}}} \end{bmatrix}^{-1} \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} \left[\hat{v}_{\mathrm{in}}(s)\right] + \begin{bmatrix} s & \frac{1-D}{L} \\ -\frac{1-D}{C_{\mathrm{dc}}} & s+\frac{1}{RC_{\mathrm{dc}}} \end{bmatrix}^{-1} \begin{bmatrix} 0 & \frac{1}{L} \\ -\frac{1}{C_{\mathrm{dc}}} & 0 \end{bmatrix} \begin{bmatrix} I_{\mathrm{ac}} \\ V_{\mathrm{dc}} \end{bmatrix} \left[\hat{d}(s)\right] \tag{15}$$

From the above equation, we get:

$$\hat{i}_{\mathrm{ac}}(s) = \frac{sC_{\mathrm{dc}}+\frac{1}{R}}{s^2LC_{\mathrm{dc}}+s\frac{L}{R}+(1-D)^2}\hat{v}_{\mathrm{in}}(s) + \frac{(1-D)I_{\mathrm{ac}}+(sC_{\mathrm{dc}}+\frac{1}{R})V_{\mathrm{dc}}}{s^2LC_{\mathrm{dc}}+s\frac{L}{R}+(1-D)^2}\hat{d}(s) \tag{16}$$

$$\hat{v}_{\mathrm{dc}}(s) = \frac{1-D}{s^2LC_{\mathrm{dc}}+s\frac{L}{R}+(1-D)^2}\hat{v}_{\mathrm{in}}(s) + \frac{(1-D)V_{\mathrm{dc}}-sLI_L}{s^2LC_{\mathrm{dc}}+s\frac{L}{R}+(1-D)^2}\hat{d}(s) \tag{17}$$

From Equations (16) and (17), the transfer functions G_{id}(s) for input current versus duty cycle and G_{vd}(s) for bus voltage versus duty cycle are:

$$G_{\mathrm{id}}(s) = \frac{\hat{i}_{\mathrm{ac}}(s)}{\hat{d}(s)} = \frac{(sC_{\mathrm{dc}}+\frac{1}{R})V_{\mathrm{dc}}}{s^2LC_{\mathrm{dc}}+s\frac{L}{R}+(1-D)^2} \tag{18}$$

$$G_{vd}(s) = \frac{\hat{v}_{\mathrm{dc}}(s)}{\hat{d}(s)} = \frac{(1-D)V_{\mathrm{dc}}}{s^2LC_{\mathrm{dc}}+s\frac{L}{R}+(1-D)^2} \tag{19}$$

In the bidirectional totem pole converter circuit, there is the following relationship:

$$D = 1 - \frac{v_{\mathrm{in}}}{v_{\mathrm{dc}}} \tag{20}$$

In the analysis and design of the control circuit, G_{id}(s) is the commonly used control object, where R, L, and C_{dc} are constants in the transfer function. At the same time, duty cycle D, AC input current I_{ac}, and output voltage V_{o} are the quantities that keep changing with normal operation. According to Equation (20), the factors affecting the duty cycle are the input voltage and the output voltage; when the input power is specific, the factor affecting the size of the AC input current is also the input voltage. There is a large filter capacitor at the output of the bidirectional totem pole converter circuit, so the output voltage does not vary much and can be neglected [26]. Therefore, the factor affecting G_{id}(s) is the magnitude of the input voltage. To analyze the effect of the input voltage on the transfer function, the Byrd diagram is drawn for different input voltage levels, as shown in Figure 4.

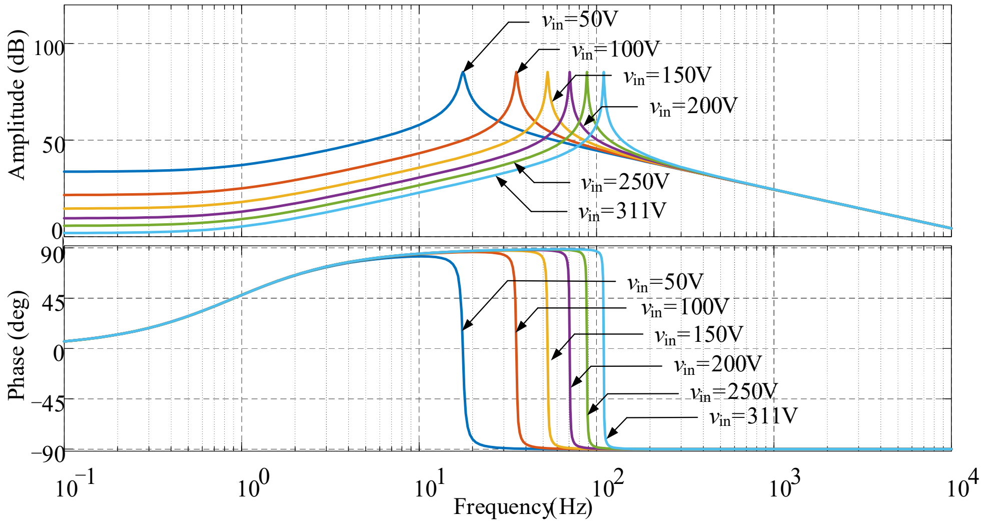

Figure 4. Bode plot of G_{id}(s) at different input voltages.

As seen in Figure 4, the low-frequency characteristics of G_{id}(s) are different for different input voltages, whereas the high-frequency characteristics are the same. The current loop deals with the high-frequency signal, so the influence of the low-frequency band can be ignored in the analysis, and then the control system can be designed.

2.2. Bidirectional CLLLC Resonant Converter Modeling

The fundamental wave analysis method is used to model the bidirectional CLLLC resonant converter. Then its equivalent circuit model is obtained to analyze the characteristics of the bidirectional CLLLC resonant converter.

2.2.1. Equivalent Circuit Model

Taking forward operation as an example, the alternating conduction of power switches Q_1 to Q_4 makes the input voltage v_{ab} of the resonant network a square wave signal with amplitude varying from $-V_{dc}$ to V_{dc}, for which the Fourier expansion is carried out to obtain the following expression:

$$v_{ab}(t) = \frac{4V_{dc}}{\pi} \sum_{m=1,3,5\cdots}^{\infty} \frac{1}{m} \sin(2\pi m f_s t) \tag{21}$$

where m is an integer parameter; f_s is the switching frequency.

From Equation (21), the fundamental components of v_{ab} and their RMS values are:

$$v_{ab\_FHA} = \frac{4V_{dc}}{\pi} \sin(2\pi f_s t) \tag{22}$$

$$V_{ab\_FHA} = \frac{2\sqrt{2}V_{dc}}{\pi} \tag{23}$$

Similarly, the output voltage v_{cd}, the fundamental component of the output voltage v_{cd_FHA}, and its RMS value V_{cd_FHA} are obtained as follows:

$$v_{cd}(t) = \frac{4V_o}{\pi} \sum_{m=1,3,5\cdots}^{\infty} \frac{1}{m} \sin(2\pi m f_s t - \theta) \tag{24}$$

$$v_{cd\_FHA} = \frac{4V_o}{\pi} \sin(2\pi f_s t - \theta) \tag{25}$$

$$V_{\text{cd\_FHA}} = \frac{2\sqrt{2}V_{\text{o}}}{\pi} \tag{26}$$

where θ is the phase difference between v_{ab} and v_{cd}.

Equating the load at the output to the resistance R_{o}, the expression of the output current of the resonant network is:

$$i_{\text{Ls}}(t) = \sqrt{2}I_{\text{Ls}}\sin(2\pi f_{\text{s}}t - \theta) \tag{27}$$

where I_{Ls} is the RMS value of the output current of the resonant network.

From Equation (27), the average value of the output current is:

$$I_{\text{o}} = \frac{2}{T_{\text{s}}}\int_0^{\frac{T_{\text{s}}}{2}} |i_{\text{Ls}}(t)|dt = \frac{2\sqrt{2}}{\pi}I_{\text{Ls}} \tag{28}$$

And because $v_{\text{cd\_FHA}}$ is in phase with i_{Ls}, the rectifier network, as well as the output load, can be equated to a purely resistive load, i.e.,

$$V_{\text{cd\_FHA}} = \frac{2\sqrt{2}V_{\text{o}}}{\pi} \tag{29}$$

Converting the secondary components of the transformer to the primary side, we get:

$$\begin{aligned} R_{\text{eq}} &= n^2 R_{\text{o.eq}} = \tfrac{8n^2}{\pi^2} R_{\text{o}} \\ C_{\text{s}} &= \tfrac{C_{\text{s}}}{n^2} \\ L_{\text{s}} &= n^2 L_{\text{s}} \end{aligned} \tag{30}$$

where R_{eq} is the resistance converted to the primary side; $C_{\text{s}}{}'$ is the capacitance converted to the primary side; $L_{\text{s}}{}'$ is the inductance converted to the primary side; n is the transformer ratio.

In summary, the voltages at points a and b on the primary side of the transformer are $v_{\text{ab\_FHA}}(t)$, and the voltages between points c and d on the secondary side are converted to $nv_{\text{cd\_FHA}}(t)$ on the primary side, while the capacitance inductance on the secondary side is converted to the primary side, resulting in the equivalent circuit model of the rear stage converter, as shown in Figure 5.

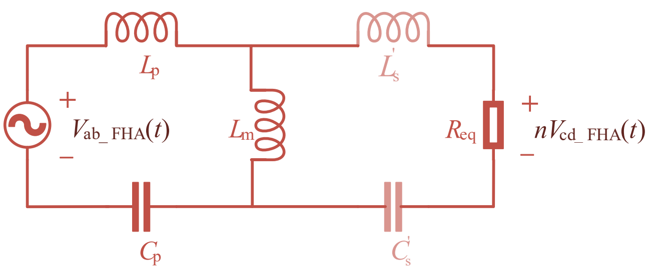

Figure 5. Forward equivalent circuit model of bidirectional CLLLC resonant converter.

2.2.2. Characteristic Analysis

The following is a characterization of the bidirectional CLLLC resonant converter, including voltage gain characteristics, impedance characteristics, inductance coefficient, and quality factor.

1. Voltage Gain Characteristics

M is the DC voltage gain characteristic of the CLLLC resonant converter, whose expression is:

$$M(f_{\rm n}) = \frac{1}{\sqrt{(1+\frac{1}{k}-\frac{1}{kf_{\rm n}^2})^2 + [Qf_{\rm n}(2+\frac{1}{k}) - \frac{Q}{f_{\rm n}}(2+\frac{2}{k}) + \frac{Q}{kf_{\rm n}^3}]^2}} \quad (31)$$

where $f_{\rm n}$ is the normalized frequency, k is the inductance factor, and Q is the quality factor. The expressions are:

$$f_n = \frac{f_s}{f_{r1}}$$
$$k = \frac{L_m}{L_p} \quad (32)$$
$$Q = \frac{\sqrt{L_p/C_p}}{R_{eq}}$$

where $f_{\rm r1}$ is the resonant frequency of the resonant inductor and resonant capacitor of the transformer, i.e., the resonant frequency of $L_{\rm p}$, $C_{\rm p}$, or $L_{\rm s}$, $C_{\rm s}$; $f_{\rm s}$ is the switching frequency.

As seen from Equation (32), the main parameters affecting the voltage gain are k and Q. If the quality factor Q = 0.5, the change law of voltage gain with normalized frequency for different k values is shown in Figure 6.

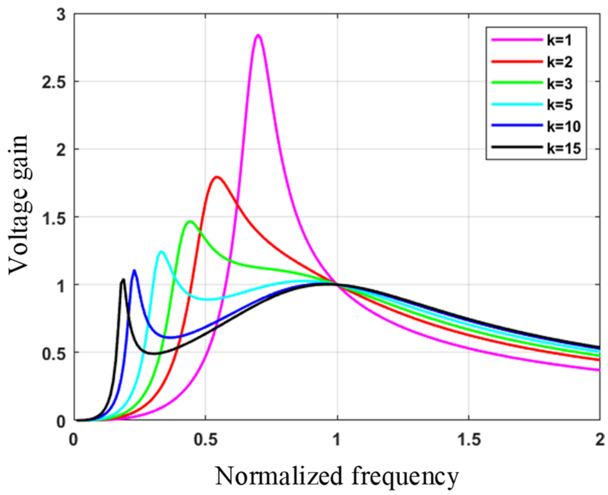

Figure 6. Voltage gain at different k values (Q = 0.5).

When the Q value is specific, the maximum voltage gain value of the resonant converter gradually decreases with the increase of the k value, the corresponding normalized frequency gradually decreases, and the curve has a trough after the highest point. On the right side of the resonance point, the smaller the k value is, the faster the voltage gain changes with the normalized frequency, which benefits the voltage gain regulation [27].

When the inductance coefficient k = 2, the curves of voltage gain with $f_{\rm n}$ change at different Q values are shown in Figure 7.

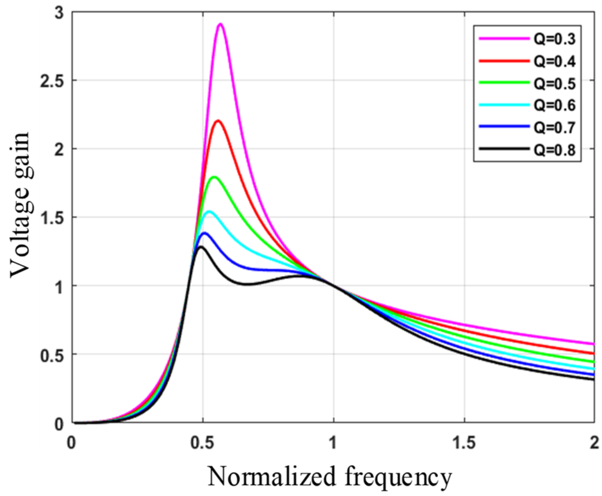

Figure 7. Voltage gain at different Q values (k = 2).

When the value of k is specific, and the normalized frequency is less than 1, the Q value is small, the voltage gain of the converter is wide, and the voltage regulation rate is fast. In contrast, when the normalized frequency is greater than 1, the voltage gain of the converter is narrow, and the voltage regulation rate is relatively flat, which will not meet the requirements of the system. When the Q value is too large, the voltage gain curve has two peak points when the switching frequency is less than the resonant frequency, which is unsuitable for the converter's stability and the control system's design. At more significant values than the resonant frequency, the gain curve of the converter gradually becomes steeper, but the peak gain may not meet the system requirements for voltage gain. Therefore, the Q value is too large or too small to meet the design requirements, and a compromise should be made in the specific selection process.

2. Impedance Characteristics Analysis

According to Figure 5, the following impedances are defined:

$$\begin{cases} Z_1 = j\omega_s L_p + 1/(j\omega_s C_p) \\ Z_2 = j\omega_s L_s + 1/(j\omega_s C_s') \\ Z_m = j\omega_s L_m \end{cases} \tag{33}$$

where Z_1 is the primary series resonant impedance; Z_2 is the equivalent secondary series resonant impedance; Z_m is the excitation inductance impedance; $\omega_s = 2\pi f_s$ is the switching angle frequency.

The input impedance is:

$$Z_{in} = Z_1 + Z_m // (Z_2 + R_{eq}) \tag{34}$$

The imaginary part:

$$\mathrm{Im}(Z_{in}) = \frac{R_{eq}Q((k+1)f_n^3 - f_n)[Q^2((2k+1)f_n^2 - 1)(f_n^2 - 1) + f_n^2]}{f_n^4 + Q^2(f_n - (k+1)f_n^3)^2} \tag{35}$$

Let Equation (35) be 0, then:

$$\begin{cases} Q = \frac{f_n}{\sqrt{(1-f_n^2)[(2k+1)f_n^2-1]}} \\ f_{n1} = \frac{1}{\sqrt{k+1}} \end{cases} \tag{36}$$

Substituting Equation (36) into Equation (31), we get M = 1, and then according to Im(Z_{in})> 0 when f_n > 1, we can get the resistive divider of the bidirectional CLLLC resonant converter as shown in Figure 8.

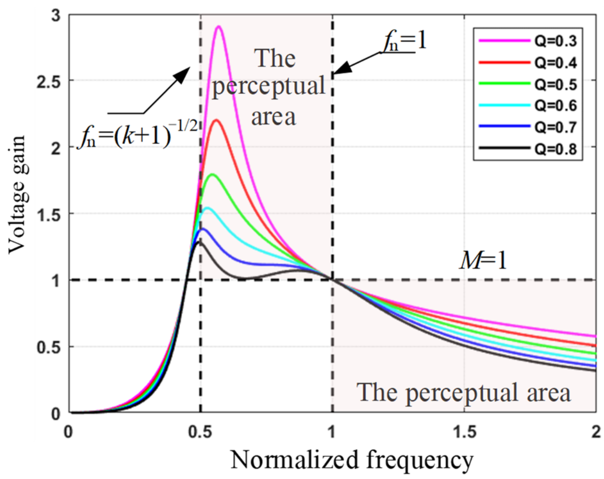

Figure 8. Resistive divider for bidirectional CLLLC resonant converter (k = 2).

As seen from Figure 8, the overlap area on the upper side of the line M = 1 and the right side of f_n = $(k + 1)^{-1/2}$ is the inductive region. The inductive region in the region where f_n > 1 can realize the ZVS of the switching transistor, and in the process of designing k and Q it is essential to ensure that the curve falls within these two regions.

3. Design Conditions for the Inductance Factor K and Quality Factor Q

The bidirectional CLLLC resonant converter needs to meet the voltage gain requirement. At no-load Q = 0, the voltage gain is:

$$M(f_{\text{n\_max}})|_{Q=0} = \frac{1}{1+\frac{1}{k}-\frac{1}{kf_{\text{n\_max}}^2}} \tag{37}$$

The minimum voltage gain $M_{\min}$ satisfies:

$$M_{\min} > M(f_{\text{n\_max}})|_{Q=0} \tag{38}$$

This leads to the design condition of the inductance coefficient k:

$$k < \frac{M_{\min}(f_{\text{n\_max}}^2-1)}{(1-M_{\min})f_{\text{n\_max}}^2} \tag{39}$$

As can be seen from Figure 8, in f_n > 1, the voltage gain curve is located in the inductive region and monotonically decreasing; in the area of $1/(k + 1)^{1/2}$ < f_n < 1, the voltage gain curve may be located outside the inductive area and may not appear monotonically, to meet the requirements, Q needs to meet certain conditions, thus the following focus on this operating frequency range. To meet the ZVS condition of the switching transistor, Im(Z_{in}) > 0 should be satisfied. Then:

$$Q_{\max 1} < F_1(f_n) = \frac{f_n}{\sqrt{(1-f_n^2)[(2k+1)f_n^2-1]}} \tag{40}$$

Let $F_1{}'(f_\mathrm{n}) = 0$; then there is a unique solution in the range of $1/(k+1)^{1/2} < f_\mathrm{n} < 1$; that is, $f_{\mathrm{n}1} = 1/(2k+1)^{1/4}$, which is a minimal value, and which is substituted into the equation $F_1(f_\mathrm{n})$ to get:

$$Q_{\max 1} < \frac{1}{\sqrt{2k+1}-1} \tag{41}$$

To make the voltage gain curve monotonically decreasing, we have:

$$M(f_\mathrm{n}) = \frac{-\frac{2}{k} f_\mathrm{n}^4 A(f_\mathrm{n}) - Q^2 f_\mathrm{n}^2 B(f_\mathrm{n}) C(f_\mathrm{n})}{[f_\mathrm{n}^2 A^2(f_\mathrm{n}) + Q^2 B^2(f_\mathrm{n})]^{\frac{3}{2}}} < 0 \tag{42}$$

$$\begin{cases} A(f_\mathrm{n}) = f_\mathrm{n}^2(1+\frac{1}{k}) - \frac{1}{k} \\ B(f_\mathrm{n}) = f_\mathrm{n}^4(2+\frac{1}{k}) - f_\mathrm{n}^2(2+\frac{2}{k}) + \frac{1}{k} \\ C(f_\mathrm{n}) = f_\mathrm{n}^4(2+\frac{1}{k}) + f_\mathrm{n}^2(2+\frac{2}{k}) - \frac{3}{k} \end{cases} \tag{43}$$

In the range of $1/(k+1)^{1/2} < f_\mathrm{n} < 1$, $A(f_\mathrm{n}) > 0$, $B(f_\mathrm{n}) < 0$, and $C(f_\mathrm{n})$ there exists a zero point for:

$$f_{\mathrm{n}2} = \sqrt{\frac{-(k+1)+\sqrt{4+8k+k^2}}{2k+1}} \tag{44}$$

It is known that $f_{\mathrm{n}2} < f_{\mathrm{n}1}$ and $C(f_\mathrm{n}) > 0$ in the range $f_{\mathrm{n}1} < f_\mathrm{n} < 1$. To make $M'(f_\mathrm{n})$ less than 0, it follows that:

$$Q_{\max 2} < F_2(f_\mathrm{n}) = \sqrt{\frac{-\frac{2}{k} f_\mathrm{n}^2 A(f_\mathrm{n})}{B(f_\mathrm{n}) C(f_\mathrm{n})}} \tag{45}$$

In summary, two constraints on the quality factor Q are obtained.

3. Control Strategy of the Charging System

The block diagram of the bidirectional charging system control strategy is shown in Figure 9. The front-stage bidirectional totem pole converter adopts a voltage and current double closed-loop control, and the dc bus voltage v_dc is compared with the reference voltage $v_\mathrm{dc\_ref}$ to obtain the error v_err; the error v_err is first passed through the transfer function $G_\mathrm{v}(s)$ of the voltage loop PI controller, and then multiplied by the v_shape obtained through the phase-locked loop PLL to get further the current reference which is consistent with the phase of the ac input voltage $i_\mathrm{ac\_ref}$, and then make a difference with the sampled input current i_ac, the result i_err after the current loop PI controller transfer function $G_\mathrm{i}(s)$ for Sinusoidal Pulse Width Modulation (SPWM), the output signal through the drive circuit to control the switching transistor on and off.

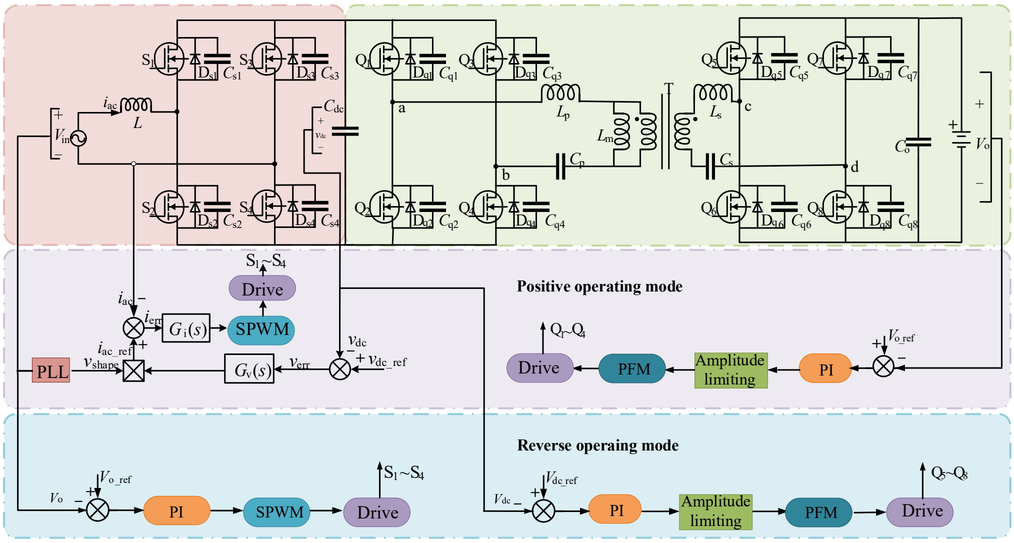

Figure 9. Control strategy of the charging system.

The back-stage bidirectional CLLLC resonant converter adopts frequency conversion control; when working in the forward operation, the actual output voltage V_o and the given voltage V_{o_ref} make a difference through the PI regulator and for limiting, and then through the pulse frequency modulation (PFM) and the driver module to control the switch transistor Q_1~Q_4 on and off; at this time the secondary side switch transistor is only renewed by the body diode. The control in the reverse operation is similar to that in the forward movement and will not be described in detail here.

To improve the power factor, the input current of the bidirectional totem pole converter should accurately track the input voltage, thus requiring the current inner loop for regulation; the normal operation of the backstage CLLLC resonant converter requires a stable DC voltage output from the front stage, thus requiring the voltage outer loop for regulation. The voltage and current double closed-loop controller design will be carried out below.

3.1. Current Internal Loop Controller Design

The current in-loop controller is shown in Figure 10, where G_{id}(s) is the transfer function of the input current versus the duty cycle.

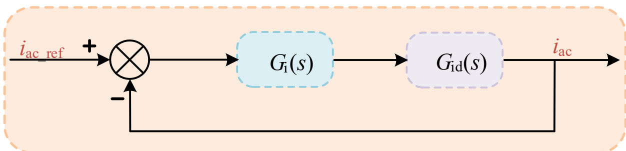

Figure 10. Structure of current inner loop controller.

The expression for the PI controller $G_i(s)$ is:

$$G_i(s) = k_{ip} + \frac{k_{ii}}{s} \tag{46}$$

where k_{ip} is the proportionality factor; k_{ii} is the integration factor.

From Figure 10, the current loop open-loop transfer function is:

$$G_{io}(s) = G_i(s)G_{id}(s) = \frac{(k_{ip}s + k_{ii})V_{dc}}{s^2 L} \tag{47}$$

Let s = jω be substituted in the above equation to get:

$$G_{\mathrm{io}}(\mathrm{j}\omega) = \frac{(\mathrm{j}k_{\mathrm{ip}}\omega + k_{\mathrm{ii}})V_{\mathrm{dc}}}{-\omega^2 L} \tag{48}$$

The corresponding amplitude-frequency characteristics and phase frequency characteristics are:

$$\begin{cases} L_{\mathrm{io}}(\omega) = 20\log|G_{\mathrm{io}}(\mathrm{j}\omega)| = 20\log\left(\frac{V_{\mathrm{dc}}\sqrt{\omega^2 k_{\mathrm{ip}}^2 + k_{\mathrm{ii}}^2}}{\omega^2 L}\right) \\ \varphi_{\mathrm{io}(\omega) = \arctan(\frac{k_{\mathrm{ip}}\omega}{k_{\mathrm{ii}}}) - 180^\circ} \end{cases} \tag{49}$$

To ensure the stability of the system, in general, the Bode diagram crossing frequency of the corrected open-loop transfer function is lower than 1/10 of the switching frequency. The switching frequency of the bidirectional totem pole converter in this design is 50 kHz, so the cutoff frequency is selected as 5 kHz, i.e., $\omega_{\mathrm{c}} = 2\pi f_{\mathrm{s}} = 3.14 \times 10^4$ rad/s, while keeping the phase margin as $\gamma_{\mathrm{i}} = 45°$. Substituting the design conditions to Equation (49) to obtain:

$$\begin{cases} \frac{V_{\mathrm{dc}}\sqrt{\omega_{\mathrm{ic}}^2 k_{\mathrm{ip}}^2 + k_{\mathrm{ii}}^2}}{\omega_{\mathrm{ic}}^2 L} = 1 \\ 180^\circ + \arctan(\frac{k_{\mathrm{ip}}\omega_{\mathrm{ic}}}{k_{\mathrm{ii}}}) - 180^\circ = \gamma_{\mathrm{i}} \end{cases} \tag{50}$$

From Equation (50), we obtain k_{ip} = 0.2137 and k_{ii} = 6710. The open-loop Bode diagram of the current loop before and after correction of the system is shown in Figure 11; the cut-off frequency of the system after modification is 5 kHz, and the phase margin is 45°, so the system can reach the steady state to meet the design requirements.

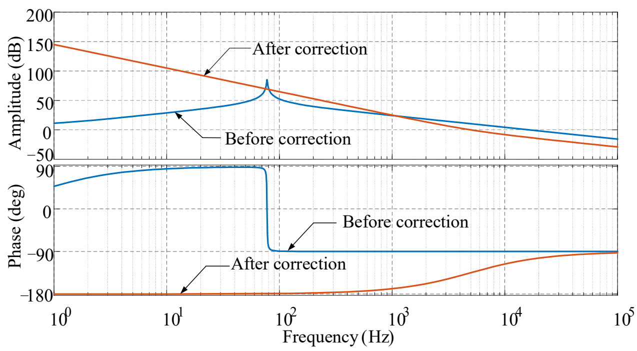

Figure 11. Open-loop Bode diagram of the current loop before and after correction.

3.2. Voltage Outer Loop Controller Design

A simplified controller can be obtained by putting the current loop regulation link as a whole into the block diagram of the voltage outer loop, as shown in Figure 12.

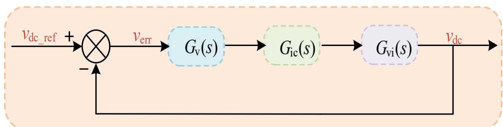

Figure 12. Voltage outer loop controller structure.

The transfer function of the voltage loop PI compensator is:

$$G_{\mathrm{v}}(s) = k_{\mathrm{vp}} + \frac{k_{\mathrm{vi}}}{s} \tag{51}$$

where k_{vp} is the proportionality factor; k_{vi} is the integration factor.

The current closed-loop transfer function is:

$$G_{\text{ic}}(s) = \frac{G_{\text{io}}(s)}{1 + G_{\text{io}}(s)} = \frac{(k_{\text{ip}}s + k_{\text{ii}})V_{\text{dc}}}{s^2L + (k_{\text{ip}}s + k_{\text{ii}})V_{\text{dc}}} \tag{52}$$

$G_{\text{iv}}(s)$ is the transfer function that represents the relationship between input current and output voltage, which can be obtained from Equations (18) and (19):

$$G_{\text{vi}}(s) = \frac{G_{\text{vd}}(s)}{G_{\text{id}}(s)} = \frac{(1 - D)R}{sCR + 1} \tag{53}$$

From Equations (51)–(53), the open-loop transmission of the voltage loop before correction is as follows:

$$\begin{aligned} G_{\text{vob}}(s) &= G_{\text{ic}}(s) \times G_{\text{vi}}(s) = \frac{(k_{\text{ip}}s+k_{\text{ii}})V_{\text{dc}}}{s^2L+(k_{\text{ip}}s+k_{\text{ii}})V_{\text{dc}}} \times \frac{(1-D)R}{sCR+1} \\ &= \frac{(0.2137s+6710)\times 400}{s^2\times 3.85\times 10^{-3}+(0.2137s+6710)\times 400} \times \frac{0.55\times 533}{s\times 330\times 10^{-6}\times 533+1} \\ &\approx \frac{25060s+7868\times 10^5}{6.772\times 10^{-4}s^3+15.04s^2+4722\times 10^2 s+2684\times 10^3} \end{aligned} \tag{54}$$

The open-loop transfer function of the corrected voltage loop is:

$$G_{\text{vo}}(s) = G_{\text{v}}(s)G_{\text{vob}}(s) = \frac{(k_{\text{vp}}s + k_{\text{vi}})(k_{\text{ip}}s + k_{\text{ii}})V_{\text{dc}}(1 - D)R}{s[s^2L + (k_{\text{ip}}s + k_{\text{ii}})V_{\text{dc}}](sCR + 1)} \tag{55}$$

To reduce the output voltage ripple, the cutoff frequency of the voltage loop is set to 10 Hz, i.e., ω_{vc} = 62.8 rad/s, and the phase margin is set to 45°. Substitute s = jω into Equation (55) to obtain the corresponding amplitude and phase frequency characteristics as:

$$\begin{cases} L_{\text{v}}(\omega_{\text{vc}}) = 1 \\ 180^\circ + \varphi_{\text{v}(\omega_{\text{vc}})=45^\circ} \end{cases} \tag{56}$$

From the above equation, k_{vp} = 0.0242 and k_{vi} = 1.822. The open-loop Bode diagram of the voltage loop before and after correction of the system is shown in Figure 13. The cutoff frequency of the system before correction is 290 Hz, which becomes 10.1 Hz after correction, and the phase margin also becomes 46°, which shows that the PI controller meets the expected design requirements.

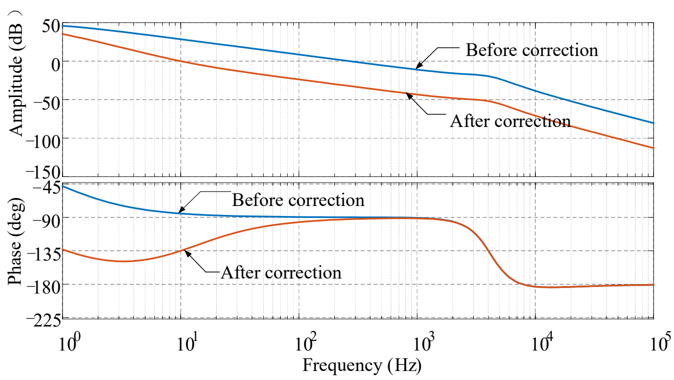

Figure 13. Open-loop Bode diagram of the voltage loop before and after correction.

3.3. Control of Soft Start

After the optimization of the relevant coefficients, in order to ensure that the system can achieve the desired control objectives, realize safe and reliable operation, significantly improve the system operating efficiency and reduce the occurrence of faults, it is necessary to propose a highly efficient control method of frequency conversion for the current operating characteristics of the system, so as to achieve the rationalization of resource utilization. In addition, the use of a high-efficiency control strategy can also improve the shock resistance, form a favorable protection for capacitors, and further optimize the system to ensure that the CLLLC resonant converter has a soft-start function and can smoothly complete the continuous output of voltage, so it can be seen that the application of a control strategy is extremely important. At the same time, the resonant converter uses PFM control during the operation phase, and this control system has certain special features that need to be adjusted to the maximum value when the load is light, combined with the relevant switching frequency theory, in order to ensure the actual efficacy [28]. Therefore, in order to improve the utilization of the inverter controller, relevant research in the CLLLC resonant converter, in which soft-start control is more effective, is carried out.

The application of soft-start control to the inverter system can complete the improvement of the system performance and make the system performance more smoother. For the CLLLC resonant converter the role for the application range expansion gradually presents itself. When in normal start, usually, it will be in a default state, allowing the primary side capacitor to complete charging, when the output voltage is 0 [29]. Based on such a premise, the signal based on PFM control can be used directly to complete the drive to control the primary side switch, as can be seen from the equivalent circuit in Figure 5; the output voltage of the bridge arm has all been added to the CLLLC resonance, and on this basis it can complete the charging of the output capacitor is on the secondary side; it is worth noting that in this process there will be a large current surge. Based on such a situation, the probability of breakdown of the switching transistor will increase, over-voltage problems will occur, resulting in damage to the resonant capacitor, and the safety of the output capacitor cannot be guaranteed. In a word, simple high-frequency starting cannot be equated with an ideal starting effect, and a soft start must be invoked on the basis of the original control strategy to ensure that the CLLLC functionality is brought into play and its safe starting operation is ensured.

The soft start of the CLLLC resonant converter is a dynamic response process. In the process of soft start, the frequency change is very large. First, in the initial stage of the soft start, the frequency must be increased to a relatively high level, thus reducing the voltage and current stress in the resonant cavity. Then the frequency is slowly reduced, gradually dropping to the resonant frequency point and gradually building up the output voltage.

Commonly used frequency reduction methods are shown in Figure 14, Frequency reduction method 1 for uniform frequency reduction; that is, in the start-up process of the switching frequency proportional to time, from the maximum start the frequency $f_{\max}$ began to decline at a uniform rate, and the end of the start-up the frequency is equal to the circuit operating frequency. Frequency reduction method 2 is improved on the basis of the former circuit to establish the initial stage of resonant network energy with a faster rate of frequency reduction, to complete and then to reduce the relatively slower switching frequency to complete the process of establishing the output voltage until the start-up is completed. Frequency reduction method 3 uses the exponential function to calculate the switching frequency at each moment, but its decreasing speed is faster than the linear downscaling speed, which generates a larger current overshoot when the CLLLC resonant converter does not reach the steady state [30]. Therefore, the first frequency reduction method is used in this paper.

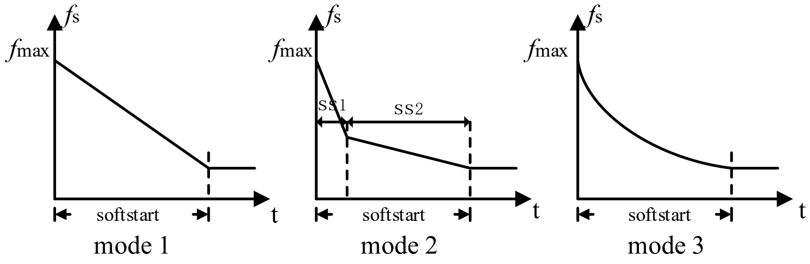

Figure 14. Soft start frequency reduction method.

In this paper, the soft start of the resonant converter is completed by a high-frequency soft-start strategy under a PI regulator. The switching frequency is increased to 150 kHz at start-up, and then the switching frequency is slowly reduced to 100 kHz, and the voltage gain is gradually increased to complete the soft start. The comparison graph of resonant current with and without a soft start in forward operating mode is shown in Figure 15. From the figure, it can be seen that, in both cases, the bidirectional CLLLC resonant converter is started from 0.004 s, and the resonant current to the device is much smaller when a soft start is adopted compared with when no soft start is taken. Comparison of the secondary side output current is shown in Figure 16. In the circuit without a soft start, the inrush current can reach 180 A, which is very dangerous for the circuit, while in a soft-start circuit the inrush current does not exceed 50 A and quickly falls to less than 15 A, indicating that a soft start for the circuit as well as the power switching transistor has a better protection effect.

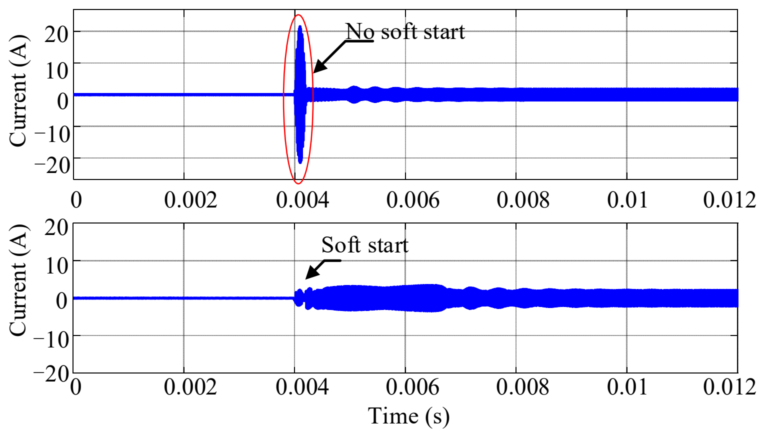

Figure 15. Comparison of resonant current with and without soft start.

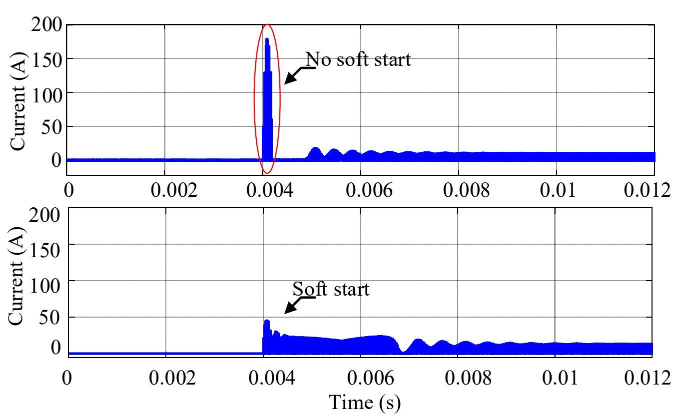

Figure 16. Comparison of secondary side output current with and without soft start.

4. Parameter Design of Charging System

The whole parameters of the charging system are designed as shown in Table 1.

Table 1. Design of the charging system.

Symbol	Description	Value
V_{in}	AC input voltage range	176–264 V
$V_{\text{in\_rated}}$	Rated AC side input voltage	220 V
V_{dc}	DC bus voltage range	380–420 V
$V_{\text{dc\_rated}}$	Rated DC bus voltage	400 V
V_{o}	DC output voltage range	44–56 V
$V_{\text{o\_rated}}$	Rated DC output voltage	48 V
P_{o}	Rated power	300 W
f_{s}	Switching frequency	50–150 kHz
f_{r1}	Resonant frequency	100 kHz
η	Efficiency	95%

4.1. Parameter Design of Bidirectional Totem Pole Changer

The inductor-capacitor is particularly important when performing the bidirectional totem pole parameter design. The design of the inductor-capacitor is carried out according to the design index of the whole charging system. At the same time, the powerswitching transistor is determined by the voltage, current, and other related parameters [31].

1. AC Inductance

The inductor stores and releases electrical energy during circuit operation and is generally designed to operate at the lowest input voltage.

Since the efficiency of the whole machine is 95%, the maximum input power of the circuit at rated condition P_{in} is:

$$P_{\text{in}} = \frac{P_{\text{o}}}{\eta} = \frac{300}{95\%} \approx 316(\text{W}) \tag{57}$$

where P_{o} is the output power; η is the efficiency.

Assuming a maximum grid voltage fluctuation of 20%, when the input voltage minimum RMS value is $V_{\text{in(min)\_rms}}$ = 176 V, the input current maximum RMS value $I_{\text{rms(max)}}$ is:

$$I_{\text{rms(max)}} = \frac{P_{\text{in}}}{V_{\text{in(min)\_rms}}} = \frac{316}{176} \approx 1.80(\text{A}) \tag{58}$$

The peak input current I_{peak} is:

$$I_{\text{peak}} = \sqrt{2} I_{\text{rms(max)}} = 2.55(\text{A}) \tag{59}$$

The size of the inductor is related to the size of the ripple of the input current. Assuming that the ripple coefficient of the input current is 20%, the ripple current ΔI is:

$$\Delta I = 20\% I_{\text{peak}} = 20\% \times 2.55 = 0.51(\text{A}) \tag{60}$$

The duty cycle D at the time of the maximum peak of the input current is:

$$D = 1 - \frac{V_{\text{in(min)\_peak}}}{V_{\text{dc\_rated}}} = 1 - \frac{176\sqrt{2}}{400} \approx 0.3777 \tag{61}$$

Therefore, the AC inductance is:

$$L \geq \frac{V_{\text{in(min)\_peak}} D}{f_{\text{s}} \Delta I} = \frac{176\sqrt{2} \times 0.3777}{50 \times 10^3 \times 0.51} \approx 3.69(\text{mH}) \tag{62}$$

where $V_{\text{in(min)peak}}$ is the peak voltage of the minimum input voltage; f_s is the switching frequency.

2. DC Bus Capacitance

When designing a capacitor, if the maintenance time is used as a limiting condition, the difference between the energy on the capacitor before and after the energy cutoff at the input is equal to the energy consumed by the load during the maintenance time. Therefore:

$$C = \frac{2P_o \Delta t}{V_{\text{dc\_rated}}^2 - V_{\text{dc(min)}}^2} = \frac{2 \times 300 \times 0.02}{400^2 - (0.8 \times 400)^2} \approx 208(\mu\text{F}) \tag{63}$$

where Δt is the maintenance time; V_{dc} is the output voltage; $V_{\text{dc(min)}}$ is the minimum capacitance-voltage value allowed after the energy cutoff at the input.

If output voltage ripple is used as a limiting condition, a compromise must be made in designing the capacitor so that the capacitor size and cost are in the correct range.

Assuming a maximum output voltage ripple of 5% of the output voltage, then:

$$\frac{\Delta V_{\text{cpp}}}{V_{\text{dc}}} = \frac{I_o}{\omega C V_{\text{dc\_rated}}} \leq 5\% \tag{64}$$

where ΔV_{cpp} is the peak-to-peak value of the ripple.

Therefore:

$$C \geq \frac{I_o}{0.05\omega V_{\text{dc\_rated}}} \approx 119(\mu\text{F}) \tag{65}$$

To meet the requirements of voltage maintenance time and output voltage ripple, the DC bus capacitor should be selected as a more significant value and retain a certain margin. In this paper, a 450 V/330 μF electrolytic capacitor is selected.

3. Power Switching Transistor Selection

In general, if the withstand voltage of the switching transistor is 1.2–1.5 times the rated withstand voltage, and the withstand current can be considered as 1.5–2 times the margin, then:

$$\begin{cases} V_{\text{VEM}} > 1.5V_{\text{dc\_rated}} = 1.5 \times 400 = 600(V) \\ I_{\text{VEM}} > 2I_{\text{peak}} = 2 \times 2.55 = 5.1(A) \end{cases} \tag{66}$$

As can be seen from (66), the rated voltage of the power switching transistor should be not less than 600 V, the rated current should be not less than 600 V, and the rated current should be not less than 5.1 A. Therefore, the selected power switching transistor is IPD65R420CFDA, whose minimum drain breakdown voltage is 650 V and whose maximum continuous drain current at 25 °C is 8.7 A, all of which meet the circuit requirements.

4.2. Parameter Design of Bidirectional CLLLC Resonant Changer

The parameters of the bidirectional CLLLC resonant converter are designed according to the design index of the charging system, and mainly for the design of the transformer, resonant inductor-capacitor design, and power switch transistor selection.

1. Transformer Turns Ratio

At the rated operating point, the transformer turns ratio is:

$$n = \frac{V_{\text{dc\_rated}}}{V_o} = \frac{400}{48} \approx 8.333 \tag{67}$$

2. The Maximum and Minimum Voltage Gain of the Transformer

According to the voltage range of DC input and output, the maximum voltage gain and minimum voltage gain of the transformer can be obtained as:

$$\begin{aligned} M_{\max} &= \tfrac{nV_{\mathrm{o\_max}}}{V_{\mathrm{dc\_min}}} \approx 1.228 \\ M_{\min} &= \tfrac{nV_{\mathrm{o\_min}}}{V_{\mathrm{dc\_max}}} \approx 0.794 \end{aligned} \tag{68}$$

3. Inductance Factor K and Quality Factor Q

The maximum operating frequency is 150 kHz, and according to Equation (39), the inductance coefficient is:

$$k < \frac{M_{\min}(f_{\mathrm{n\_max}}^2 - 1)}{(1 - M_{\min})f_{\mathrm{n\_max}}^2} \approx 2.141 \tag{69}$$

Under the consideration of converter efficiency and limitation, the larger the choice of k, the better, so k is taken as 2. Substituting the value of k into Equation (41), we get:

$$Q_{\max1} < \frac{1}{\sqrt{2k+1} - 1} \approx 0.809 \tag{70}$$

Then, according to Equation (45), we can see that:

$$Q_{\max2} < F_2(f_{\mathrm{n}}) = \sqrt{\frac{-\frac{2}{k}f_{\mathrm{n}}^2 A(f_{\mathrm{n}})}{B(f_{\mathrm{n}})C(f_{\mathrm{n}})}} \approx 0.706 \tag{71}$$

Combined with Equations (70) and (71), and Figure 8, Q = 0.5 is selected. At this time, the voltage gain curve is located within the inductive region near the resonance point. The maximum and minimum gain requirements can be met by more minor frequency adjustments and remain monotonic.

4. Resonant Inductance and Capacitance

The equivalent impedance of the converter is:

$$R_{\mathrm{eq}} = \frac{8n^2}{\pi^2}R_{\mathrm{o}} = 432.3\Omega \tag{72}$$

Then the parameters of the original secondary resonant inductor and resonant capacitor are:

$$\begin{cases} L_{\mathrm{p}} = \frac{QR_{\mathrm{eq}}}{2\pi f_{\mathrm{r1}}} = 344.01\mu\mathrm{H} \\ C_{\mathrm{p}} = \frac{1}{(2\pi f_{\mathrm{r1}})^2 L_{\mathrm{p}}} = 7.36\mathrm{nF} \\ L_{\mathrm{s}} = \frac{L_{\mathrm{p}}}{n^2} = 4.95\mu\mathrm{H} \\ C_{\mathrm{s}} = n^2 C_{\mathrm{p}} = 0.51\mu\mathrm{F} \\ L_{\mathrm{m}} = kL_{\mathrm{p}} = 688.02\mu\mathrm{H} \end{cases} \tag{73}$$

5. The Selection of Power Switching

In forward operation, the effective value of the primary resonant current is:

$$I_{\mathrm{p\_rms1}} = \sqrt{\frac{V_{\mathrm{o\_rated}}^2}{8}[(\frac{n}{2f_{\mathrm{r1}}L_{\mathrm{m}}})^2 + (\frac{\pi}{nR_{\mathrm{o}}})^2]} \approx 1.323\mathrm{A} \tag{74}$$

The effective value of the secondary resonant current is:

$$I_{\mathrm{s\_rms1}} = \sqrt{\frac{(5\pi^2 - 48)}{192\pi^2}(\frac{nV_{\mathrm{o\_rated}}}{L_{\mathrm{m}}f_{\mathrm{r1}}})^2 + \frac{\pi^2 V_{\mathrm{o\_rated}}^2}{16R_{\mathrm{o}}^2}} = 4.91\mathrm{A} \tag{75}$$

In reverse operation, the corresponding resonant current is:

$$\begin{aligned} I_{\text{p\_rms2}} &= 0.589\text{A} \\ I_{\text{s\_rms2}} &= 11.02\text{A} \end{aligned} \tag{76}$$

The voltage stress of the primary power switch is the maximum value of the DC bus voltage, i.e., 420 V, and the current stress is the peak value of the primary resonant current, i.e., 1.871 A. Therefore, the primary switch is SMD7N65, whose drain-source withstand voltage is 650 V and continuous drain current is 7 A, and the secondary switch is SQJ402EP-T1_GE3, whose drain-source withstand voltage is 100 V and the continuous drain current is 32 A.

5. Simulation Analysis

The two-stage bidirectional charging system's simulation model includes the main circuit and the control circuit. The power circuit includes a grid, bidirectional totem pole converter, and bidirectional CLLLC resonant converter; the control circuit consists of a PI controller (current loop, voltage loop), SPWM modulation, and frequency control module. In the control of the post-stage CLLLC resonant converter, the PWM signal is obtained by comparing the output voltage with the given voltage through the PI regulator and pulse frequency modulation (PFM) to control the power switching transistor. The charging system simulation model is shown in Figure 17.

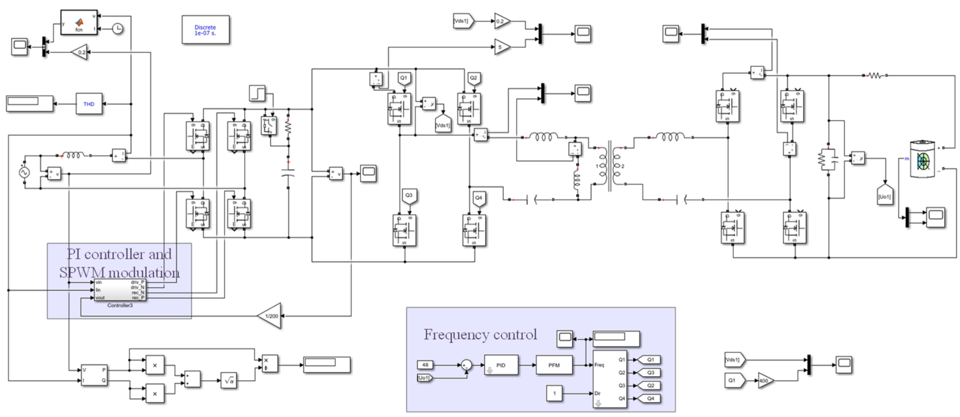

Figure 17. Charging system simulation model.

5.1. Simulation of the Forward Operating State

The bidirectional totem pole converter is cascaded with a bidirectional CLLLC resonant converter to obtain the waveform of the rated output of the charging system at full load. The simulated waveform of the front stage is shown in Figure 18. The figure shows that after 0.045 s, the front stage converter's input voltage and current phase can be kept consistent. The pre-stage output voltage fluctuates between 395 V and 405 V, and the voltage ripple is about 2.5%.

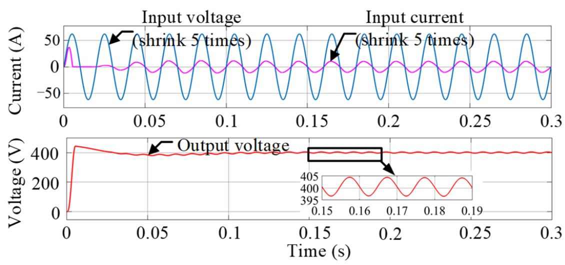

Figure 18. Simulation waveform of pre-stage.

The voltage and current of the switching transistor Q_1 are shown in Figure 19. Through the detection of the voltage at the terminal of the primary-side switching transistor Q_1 and the current flowing through Q_1, it can be seen that when the voltage at Q_1 drops from V_{dc} to zero, the current flows positively through the switching transistor Q_1 only from the anti-parallel body diode of Q_1, so the primary-side switching transistor in this state can realize ZVS. The waveforms of the resonant current and the excitation current are shown in Figure 20. When the excitation current is equal to the resonant current, the excitation current increases rapidly in the reverse operation, which shows that the operation is near the quasi-resonant point at this time. Due to the fluctuation of the DC bus voltage, the switching frequency of the resonant converter fluctuates between 95 kHz and 102 kHz.

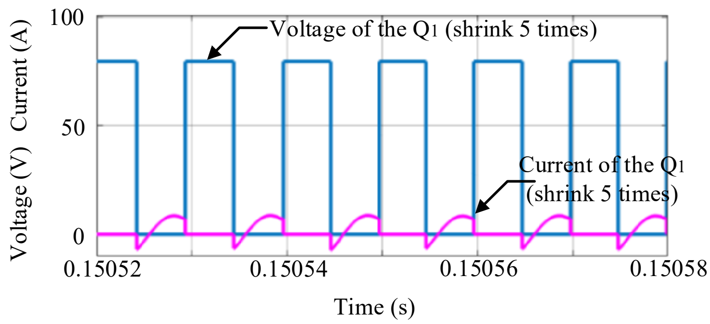

Figure 19. Voltage and current of Q_1.

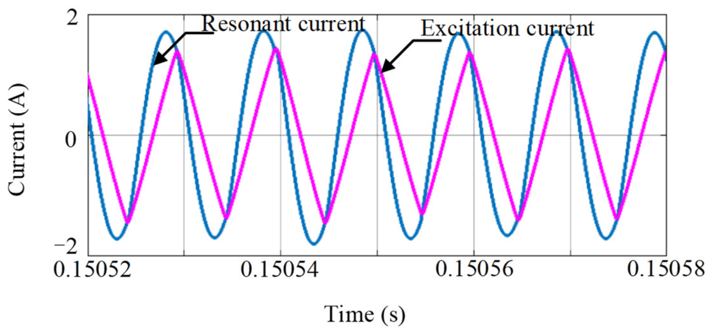

Figure 20. Resonant current and excitation current.

The currents of diodes D_{q5} and D_{q7} with the post-stage output voltages are shown in Figures 21 and 22. The detection of the secondary sidelobe diodes D_{q5} and D_{q7} shows that D_{q5} and D_{q7} just achieve ZCS, i.e., the secondary sidelobe diodes can achieve ZCS, the output voltage fluctuates between 47.9 V and 48.1 V when stable, and the output voltage ripple is about 0.4%

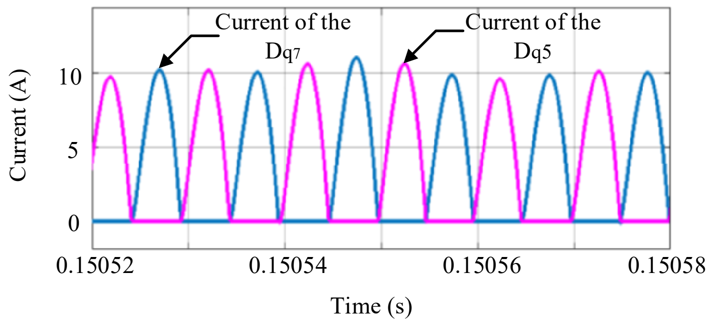

Figure 21. Current of D_{q5} and D_{q7}.

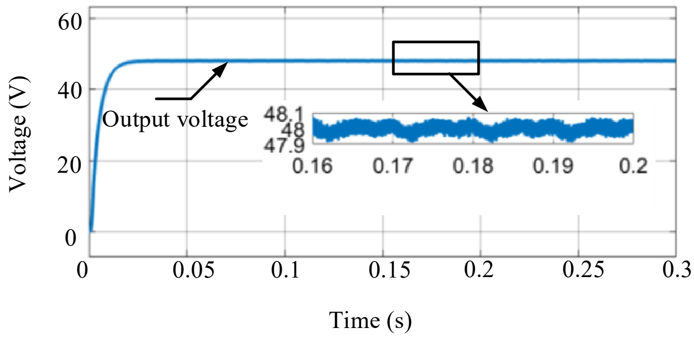

Figure 22. Output voltage of the rear stage.

5.2. Simulation of Reverse Operating State

The voltage and current waveforms of the switching transistor Q_5 are shown in Figure 23. The DC bus voltage fluctuation makes the resonant converter's switching frequency fluctuate between 110 kHz and 115 kHz. The Q_5 current flows positively to the switching transistor only after the voltage at Q_5 is zero, so the secondary side switching transistor can realize ZVS.

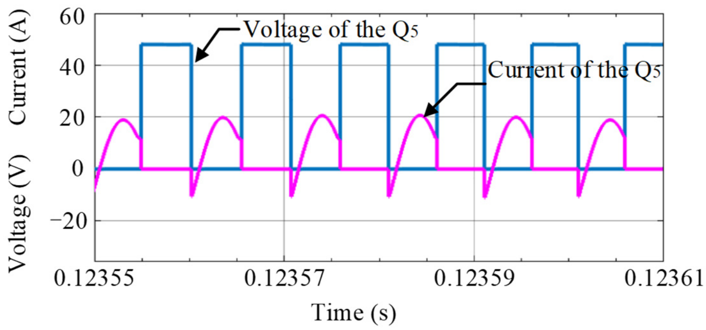

Figure 23. Voltage and current of Q_5.

The waveforms of the excitation current and the resonant current are shown in Figure 24, when the excitation current is equal to the resonant current. After the excitation current is equal to the resonant current, it rapidly increases in the reverse operation, and it is known that at this time the work is near the quasi-resonant point, and the voltage gain is about 1. In this process, the primary-side body diodes D_{q1} and D_{q3} can just achieve ZCS, and the waveform approximates a sinusoidal waveform. The current waveforms of diodes D_{q1} and D_{q3} are shown in Figure 25.

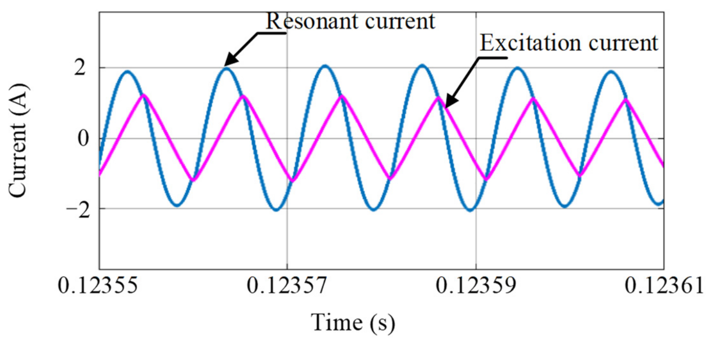

Figure 24. Resonant current and excitation current.

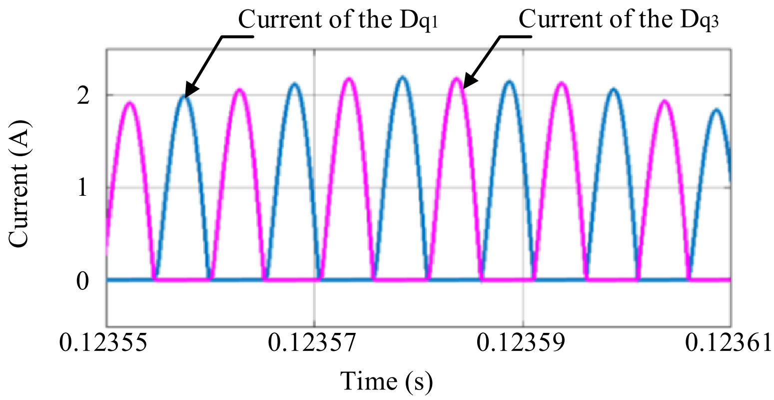

Figure 25. Current of D_{q1} and D_{q3}.

The output voltage of the rear stage converter and the output voltage of the front stage converter are shown in Figures 26 and 27. The output voltage of the rear stage bidirectional CLLLC resonant converter can be stabilized at 400 V left, and when the front stage converter works in reverse, the output voltage is output in the form of a sinusoidal waveform with a certain harmonic content. Basically, however, it can meet the output requirements.

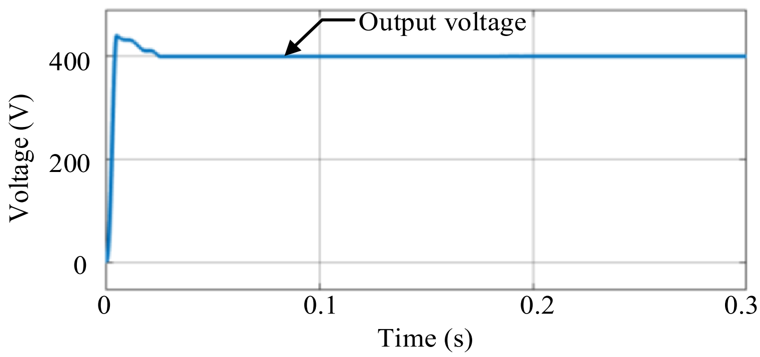

Figure 26. Output voltage of the rear stage.

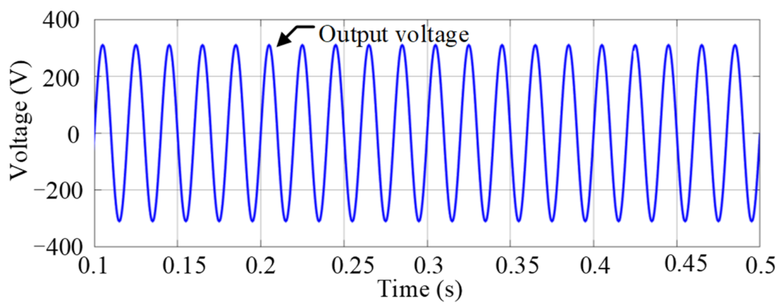

Figure 27. Pre-stage reverse output voltage waveform.

6. Experimental Verification

The hardware structure of the two-stage bidirectional isolated charging system is shown in Figure 28. The control chip TMS320F28335 is used to process the sampled input current, input voltage, and DC voltage signals to get the control signal. Then the isolated driver chip is used to drive the switch transistor to realize the forward and reverse operation of the system.

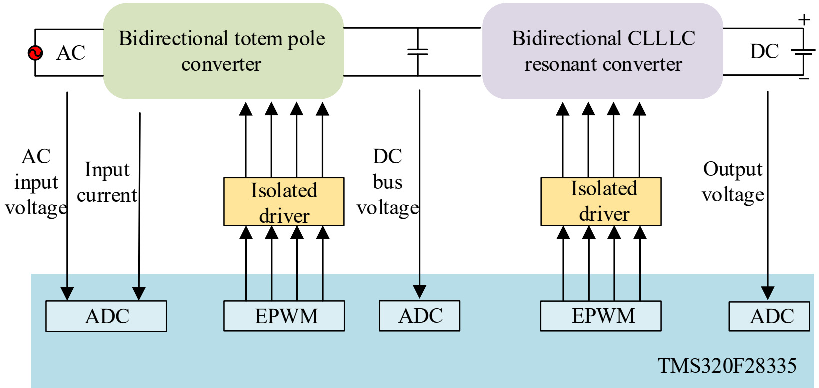

Figure 28. Block diagram of the two-stage bidirectional isolated charging system.

The experimental platform of the charging system is designed and built through the above analysis, as shown in Figure 29. It mainly includes a bidirectional isolated charging system, oscilloscope, PC, DC power supply, and electronic load, et al.

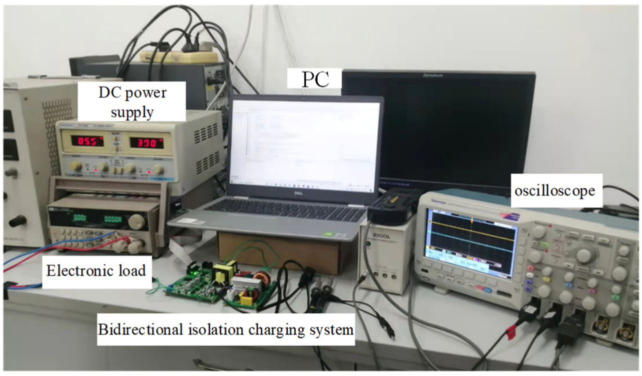

Figure 29. Experimental platform.

6.1. Forward Operation

When the charging system works in the forward operation, and at full load, the input current and voltage waveforms are shown in Figure 30. The peak value of the input current is about 2 A, which is in the same phase as the input voltage. The input current contains fewer harmonics, and the overall power factor of the charging system is high and meets the working requirements. The DC bus voltage and post-stage output voltage waveforms are shown in Figure 31. The amplitude of the DC bus voltage ranges from 392.3 V to 403.7 V, which meets the input voltage requirements of the post-stage.

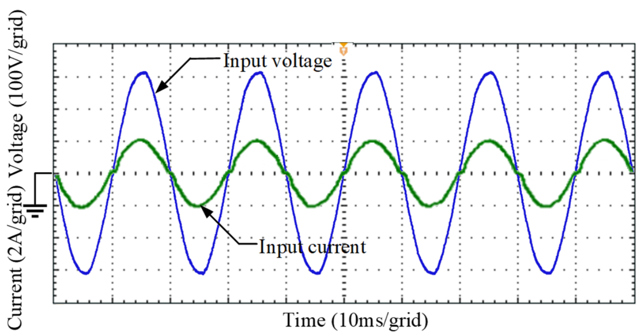

Figure 30. Input current and voltage waveforms.

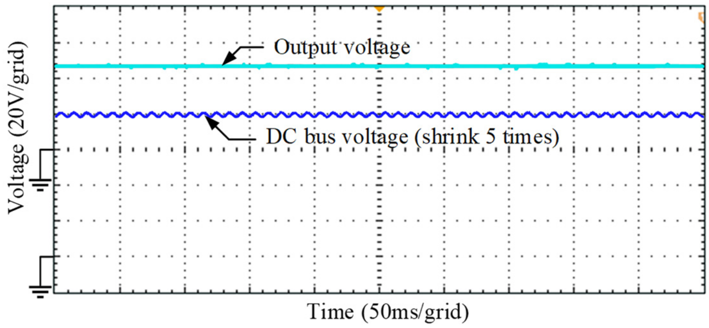

Figure 31. Front and rear stage output voltage.

The waveforms of the gate-source voltage V_{gs_2} and drain-source voltage V_{ds_2} of the primary-side switch transistor Q_2 in the forward operation of the rear stage CLLLC resonant converter are shown in Figure 32. When V_{ds_2} drops to zero potential, V_{gs_2} starts to increase, indicating that all switch transistors on the primary side in the forward operation mode can achieve ZVS, thus reducing the turn-on loss of the switch transistors.

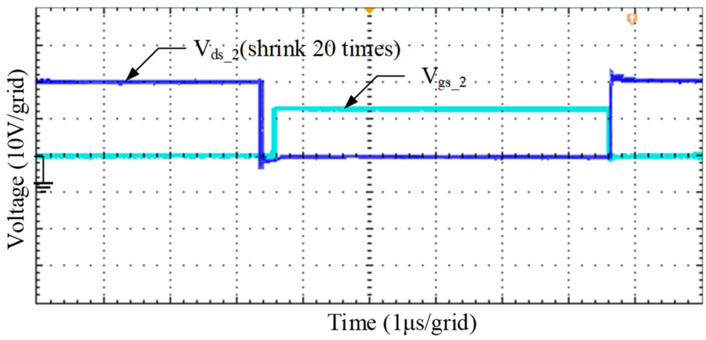

Figure 32. Switching transistor Q2 zero voltage turn-on waveform.

When starting the charging system, set the maximum dead time and the highest frequency so that the starting current is small, and then gradually reduce the operating frequency and dead time to ensure normal operation; taking the resonant current as an example, there is no current shock during the starting process, and you can choose equipment with a smaller value of voltage and current resistance to reduce costs. The soft-start process is shown in Figure 33.

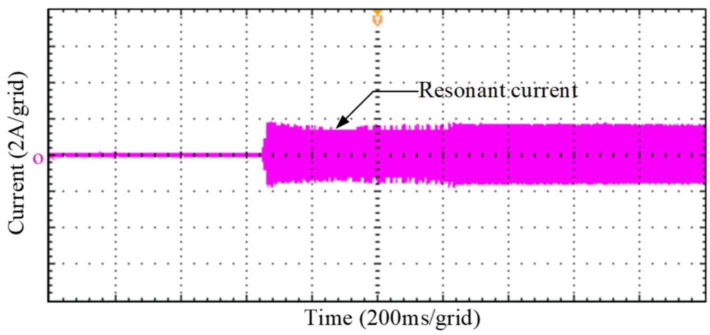

Figure 33. Soft-start process with resonant current.

6.2. Reverse Operation

When the charging system works in reverse and is fully loaded, the waveforms of output voltage and output current are shown in Figure 34. The output voltage and output current maintain a sinusoidal output, and the peak output voltage is about 311 V at this time. There is a certain harmonic content; however, it meets the requirements, which allows the power to be supplied to other devices in reverse.

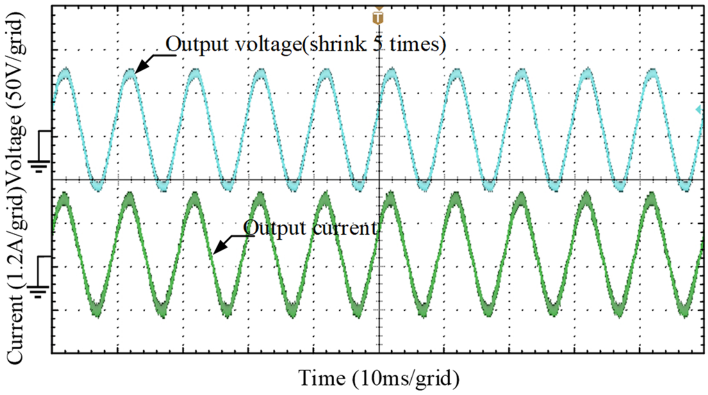

Figure 34. Output voltage and output current waveforms of reverse operation.

The waveforms of the gate-source voltage V_{gs_5} and drain-source voltage V_{ds_5} of the rear stage CLLLC resonant converter at the secondary side switch transistor Q_5 during reverse operation are shown in Figure 35, and V_{gs_5} starts to increase when V_{ds_5} drops to zero potential, thus realizing ZVS. The current waveforms of the body diodes D_{q1} and D_{q3} and the resonant current waveforms are shown in Figure 36. It can be seen that the body diodes can achieve zero-current shutdown and that the resonant current approximates a sinusoidal waveform, which is the highest efficiency.

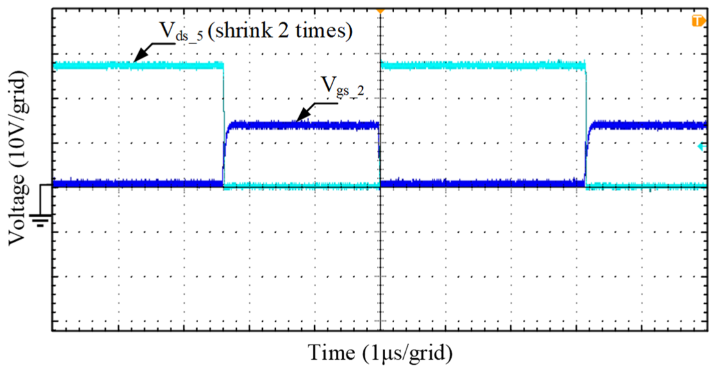

Figure 35. Switching transistor Q_5 zero voltage turn-on waveform.

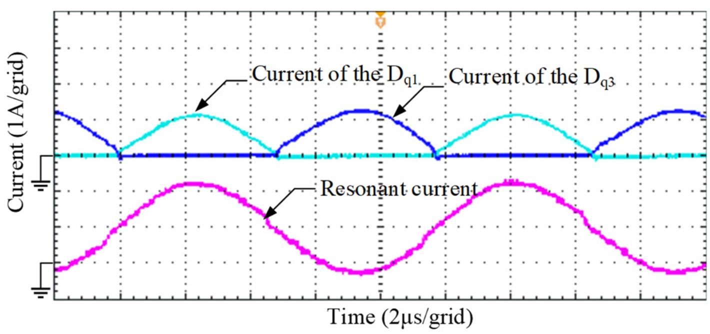

Figure 36. Output current.

A charging system with a bidirectional CLLC resonant converter in the rear stage was designed in [27] with an overall control strategy of up to 94.5% in efficiency. In this paper, the efficiency of the two-stage isolated charging system was tested and calculated at different loads, and the resulting efficiency graph is shown in Figure 37. From the graph, it can be seen that the maximum efficiency is 95.895% for forward operation and 95.504% for reverse operation. From the overall comparison, it can be seen that the charging system designed in this paper has a high efficiency.

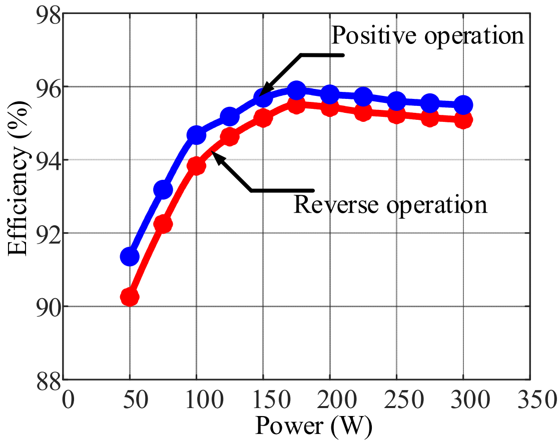

Figure 37. Efficiency curve.

7. Conclusions

In this paper, the theory, simulation, and experiment of two-stage isolated charging system topology based on resonant converter are studied, and the following conclusions are obtained:

1. Mathematical modeling of bidirectional totem pole converter using small signal analysis can obtain the transfer function of input current transformation with a duty cycle; an equivalent model of a bidirectional CLLLC resonant converter is obtained by fundamental wave analysis for characterization, and the parameters of the design are reasonable.
2. The front stage adopts voltage and current double closed-loop control to keep the DC bus voltage stable, and the rear stage adopts frequency conversion and a high-frequency soft start to control the constant output voltage. The simulation model results of the control system show that the control strategy designed in this paper is reasonable.
3. The experimental results prove that the bidirectional charging system can achieve power factor correction and has soft switching characteristics across the full load range.

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