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A High Performance and Low Power Triple-Node-Upset Self-Recoverable Latch Design

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Abstract: The charge sharing effect is becoming increasingly severe due to the continuous reduction of semiconductor process feature size. In the nanoscale digital circuit, the probability of triple-node upset (TNU) is increasing, which seriously affects the reliability of the circuit. To improve the reliability of the digital circuit, this paper presents an optimized TNU self-recoverable latch (HLTNURL). This latch consists of three dual-node-self-recoverable dual interlocked storage cells (DNSR-DICE) and one clock-gating C-element. Whenever any three nodes invert, the latch is able to self-recover to its correct logical values. The HSPICE simulation results indicate that this latch enables full self-recovery of TNU in all cases. In comparison with existing TNU self-recoverable latches, the proposed HLTNURL latch is able to reduce the power dissipation, delay, area overhead, and area-power-delay product (APDP) by 32.41%, 79.73%, 1.32%, and 88% on average. In addition, the HLTNURL latch proposed in this paper has high reliability and low sensitivity to process, voltage, and temperature (i.e., PVT) variations.

Keywords: soft error; latch hardening; c-element; triple-node-upset; self-recoverable

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1. Introduction

As the semiconductor feature size enters the nanoscale, the internal node capacitance of nanoscale integrated circuits (ICs) continues to decrease, which further results in a dramatic reduction in the number of stored charges. Moreover, the digital circuits (e.g., latches) have also become increasingly susceptible to the single event effects (SEE) as the size of semiconductor goes smaller [1]. After a node collects charges generated by high-energy particles bombardment, exceeding the critical charge on the node will result in the single-node upset (SNU) [2,3], which is called a soft error (SE). Although soft errors do not physically damage circuit components, they can seriously affect the reliability of digital circuits [4].

The continuous reduction of the feature size of the semiconductor process leads to decreasing the distance between two adjacent transistors in digital integrated circuits, which exacerbates the charge sharing effect. The nodes affected by the single event effect may increase from one to many, which will lead to multiple-node upset (MNU), e.g., double-node upset (DNU) and triple-node upset (TNU) [5]. In addition, in some special environments (e.g., space), high-energy particles have a high flux, which may bombard multiple circuit nodes simultaneously, and can also cause MNU. Research shows that MNU has become the main factor of soft errors in ICs [6,7]. Radiation hardening by design (RHBD) can effectively solve the circuit errors caused by MNU. Some studies have been conducted to reduce the probability of MNU occurrence by means of special layouts. Reference [8] proposed a new sequential element called LEAP-DICE, which adopts a special layout design. TCAD simulation results show it can reduce the probability of Ses greatly as compared to the traditional DICE structure. However, this LEAP-DICE structure cannot realize the self-recovery of TNU. Although several radiation-hardened latches with TNU tolerance have been proposed in the research community [9–15], there are still some

problems that remain. For instance, the TNU is either not self-recoverable, and it does not consume large delay or huge power to do so. Therefore, it is of great significance to study how to improve the performance while reducing the power consumption of TNU self-recoverable latches.

To solve the issues with the latches mentioned above, in this paper, we propose a TNU self-recoverable latch (HLTNURL), which can well balance power cost and delay. Firstly, we propose a dual-node self-recoverable dual interlocked storage cell (DNSR-DICE) based on the DICE (i.e., dual interlocked storage cell). Next, three DNSR-DICE modules are interlocked and connected by redundant interlock techniques. The HLTNURL is combining it with a clock gating C-element. The HLTNURL structure takes three interlocked DNSR-DICEs as an essential part of latching data to achieve the self-recovery of any TNU and improve the reliability of the circuit. In addition, by using clock gating (CG) and fast path techniques, the power dissipation and delay from the circuit are reduced. In comparison with the existing TNU self-recoverable latches, the HLTNURL reduces the power consumption, delay, area overhead, and APDP by 32.41%, 79.73%, 1.32%, and 88% on average. Furthermore, it is less sensitive to changes in PVT.

The other parts of this paper are structured as described below. Section 2 introduces existing TNU latches. Section 3 describes the circuit structure, working principle, hardening principle, and the fault tolerance verifications of the proposed latch. Section 4 compares the performance and overhead of the latch proposed in this paper with existing TNU latches and presents a comparison for several latches under PVT variations. Section 5 concludes this paper.

2. Previous TNU Latch Structures

To solve the problems caused by TNU, some hardened latches that can tolerate TNU are proposed in the existing literature. Among them, the DICE and C-element are widely employed in the design of these latches. Although the DICE can self-recover any SNU, not all the DNUs can be self-recovered. On the other hand, the C-element can filter the SNU of the input nodes, as the output is opposite to the logic value of the inputs when the C element is turned on, or it keeps the original value and enters a high-impedance state (HIS) when the C-element inputs are different. Figure 1 shows the structure and legend representation of several typical units.

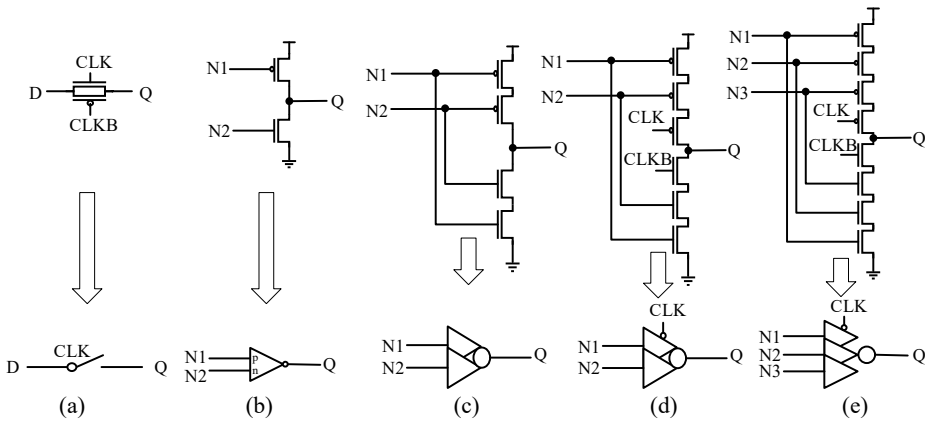


Figure 1. Several typical units: (**a**) transmission gate (TG); (**b**) two-input inverter; (**c**) two-input C-element; (**d**) CG-based two-input C-element; (**e**) CG-based three-input C-element.

2.1. LCTNUT

Figure 2 shows the LCTNUT latch proposed in [9]. The LCTNUT latch mainly takes 4 CG-based two-input inverters and 4 two-input inverters to construct a feedback loop, with the output of each inverter connected to the input of the two downstream inverters. In

addition, soft errors can be filtered by combining 2 two-input C-elements and 1 CG-based two-input C-elements, although it is not self-recoverable, and will cause extra delay.

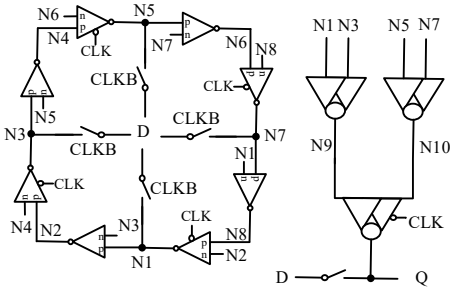


Figure 2. Latch schematic for LCTNUT.

2.2. TNU-Latch

Figure 3 shows the TNU tolerant latch (TNU-latch) proposed in [10]. The TNU-latch employs 4 interlocked CG-based four-input C-elements and 1 four-input C-element to build the feedback loop, as well as a combination of 2 three-input C-elements and 1 two-input C-element to filter soft errors. When TNU occurs at the internal node, the cascaded C-elements ensure that the output node Q is not affected. However, TNUHL is not self-recoverable, and the delay is large.

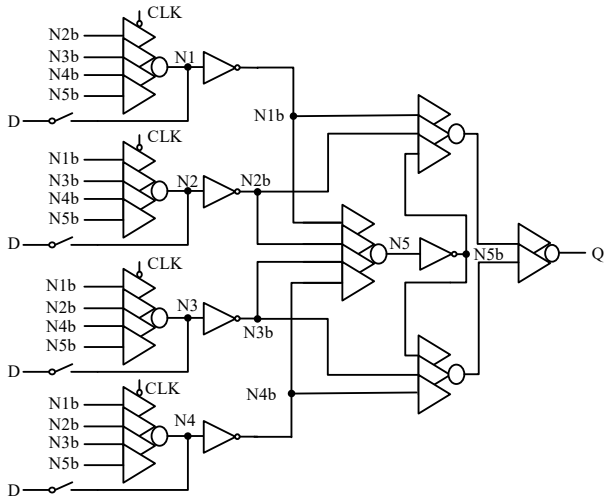


Figure 3. Latch schematic for TNU-latch.

2.3. LOCTNUTRL

Figure 4 shows the LOCTNUTRL latch proposed in [11]. The latch consists of 2 self-recovery cells (SRC), four inverters and 1 CG-based inverter. The SRC can tolerate SNU recovery themselves from particle bombardment. Two SRCs combined with multi-level inverters can achieve tolerant TNU functions. However, LOCTNUTRL is not able to self-recover, either.

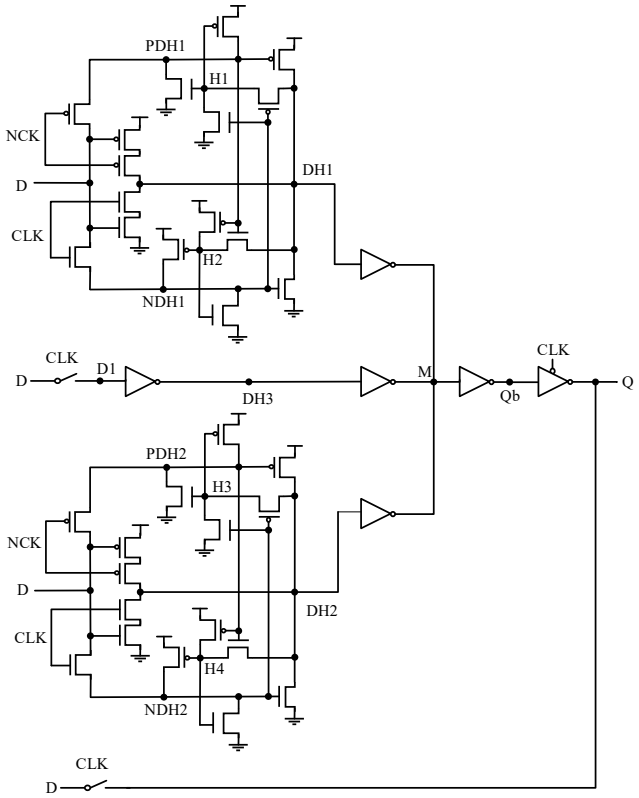


Figure 4. Latch schematic for LOCTNUTRL.

2.4. TNUTL

The triple node upset tolerant latch (TNUTL) [12] is shown in Figure 5. The TNUTL latch mainly consists of 5 three-input-split C-elements and 1 two-input C-element. TNUTL does not have the feedback path, so the downstream node flip does not affect the upstream node. The TNU occurring inside the latch can be filtered through the multi-level C-elements, but this results in a relatively large delay.

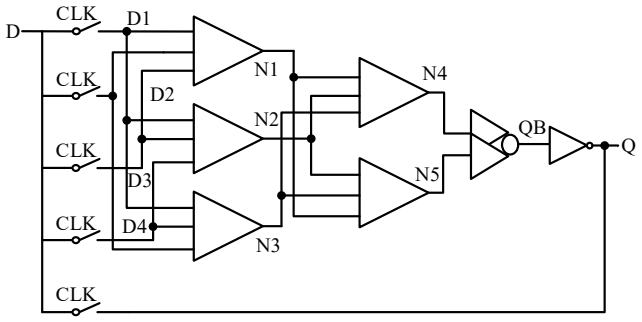


Figure 5. Latch schematic for TNUTL.

2.5. TNURL

Figure 6 presents the TNURL latch proposed in [13]. The TNURL latch primarily comprises of 7 mutually feeding back soft-error-interceptive modules (SIMs) to self-recover the TNU. Each SIM has 2 three-input C-elements and 1 CG-based two-input C-element. When TNU occurs at the internal node, the mutually feeding back mechanism between SIMs can self-recover the flipped node, thus realizing the TNU self-recovery function. However, the power cost and area cost of the TNURL latch are very high.

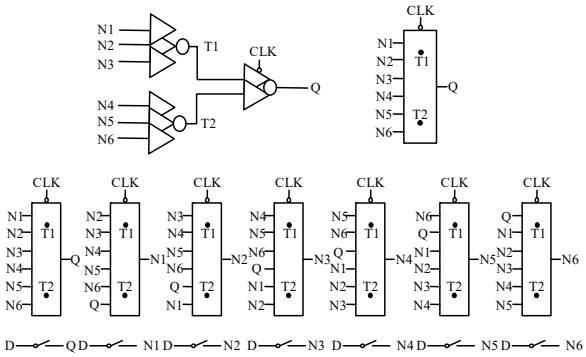


Figure 6. Latch schematic for TNURL.

2.6. LCTNURL

Figure 7 shows the LCTNURL latch proposed in [14]. The LCTNURL latch consumes 12 three-input C-elements to build the feedback loop, with the output of each C-elements linked to the input of the 3 downstream C-elements. Through the feedback loop, the LCTNURL latch can self-recover from the TNU, but its delay is large.

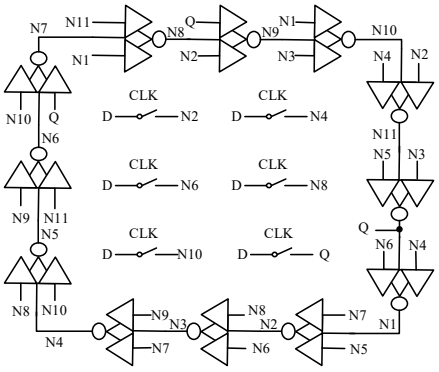


Figure 7. Latch schematic for LCTNURL.

2.7. HTNURL

Figure 8 shows the HTNURL latch proposed in [15]. The latch consists of 4 stage C-element modules, of which the first three modules consist of 4 two-input C-elements and the last module consists of four CG-based two-input C-elements. The output of each C-elements is linked to the inputs of the two downstream C-elements, thus forming a feedback loop. HTNURL enables TNU self-recovery through the feedback loop, but with a large delay.

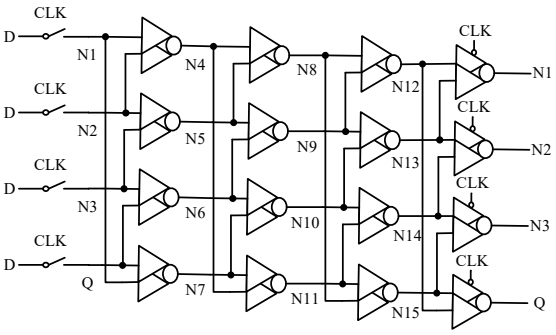


Figure 8. Latch schematic for HTNURL.

3. Proposed Hardened Latch Design

This section introduces our proposed HLTNURL latch, including its circuit structure, working principle, and hardening principle. A fault injection simulation experiment is also conducted to verify its correct function.

3.1. Circuits Structure

The HLTNURL circuit structure designed in this paper is shown in Figure 9. The structure consists of three DNSR-DICEs, seven transmission gates (TG1-TG7), and one CG-based six-input C-element, including 12 internal nodes (N1-N12). D refers to the input signal, Q refers to the output signal, while CLK and CLKB are defined as the system clock and negative system clock, respectively. Each DNSR-DICE adds eight PMOS transistors and eight NMOS transistors based on DICE. The added PMOS transistors and NMOS transistors are connected in pairs, and their gates are controlled by the eight nodes of the other two DNSR-DICEs. When the logical values of two nodes in a DNSR-DICE flip simultaneously, the internal nodes of the remaining two DNSR-DICE are unaffected, allowing the reversed nodes recover back to the original logical values. N2, N4, N6, N8, N10, and N12 connect to the input nodes of the C-element. The clock gating technique on the C-element avoids current competition in the transparent mode of the latch and reduces power consumption. The fast path technique is used between the inputs and outputs to reduce the delay. In particular, in transparent mode, Q can only be driven by D through TG1 since the output of the C-element is obstructed by the CG-based transistors. Therefore, current competition on Q can be avoided, thus reducing power consumption and delay.

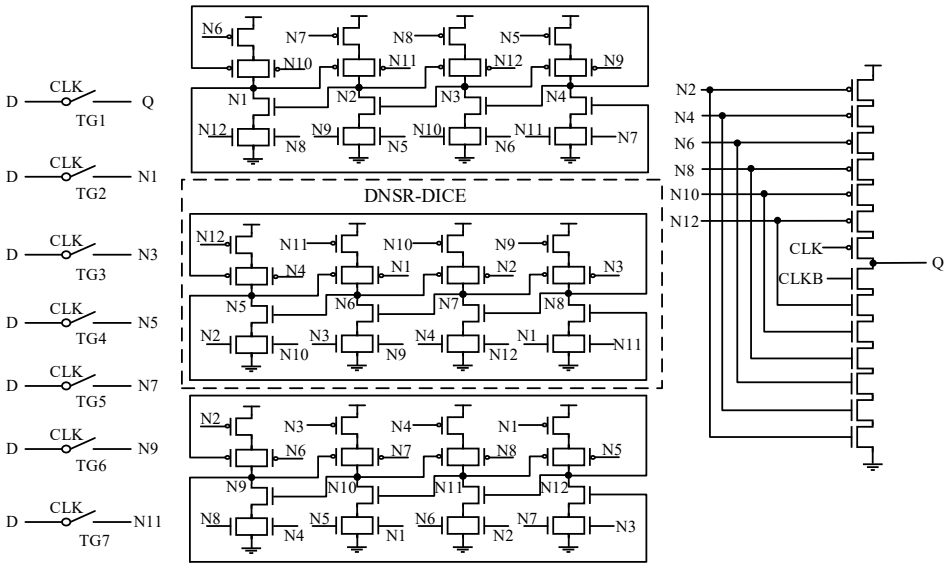


Figure 9. Proposed HLTNURL latch design.

3.2. Working Principle

When CLK = 1, CLKB = 0, the latch operates in transparent mode, seven TGs turn on, and CG-based C-element turns off. The logical value of the input signal D is transported to nodes N1, N3, N5, N7, N9, N11, and the output node Q through the TG1-TG7. The inverse logic value of D is written to nodes N2, N4, N6, N8, N10, and N12 through the three DNSR-DICEs. When CLK = 0 and CLKB = 1, the latch operates in latch mode, the seven TGs turn off, and the CG-based C-element turns on, so the data are maintained.

3.3. Hardening Principle

The HLTNURL latch designed in this paper can achieve complete SNU, DNU and TNU self-recovery in any case. The hardening principle of HLTNURL latch is analyzed and introduced in the following three scenarios.

For SNU, there are two cases: (1) The flipped node is located in the DNSR-DICE. Since the structures of the three DNSR-DICEs are the same, and the construction principles of the internal nodes of DNSR-DICE are the same, the flipping of any of the 12 nodes will be the same. Assuming that node N1 flips from "1" to "0", nodes N5, N7 and N11 are "1", so nodes N2, N6, and N12 are unaffected and node N1 can recover to "1" by nodes N4, N6, and N10. (2) The flipped node is the output node Q. The internal nodes of the latch are unaffected, so the node Q can recover through the C-element.

For DNU, there are three cases: (1) The flipped nodes are located in the same DNSR-DICE. Assuming that N1 flips from "1" to "0" and N4 flips from "0" to "1", without affecting the other nodes. N1 can recover to the "1" by N6 and N10, and N4 can recover to the "0" by N1, N7, and N11. (2) The flipped nodes locate in two different DNSR-DICEs. Assuming that N1 and N11 flip from "1" to "0" simultaneously, then N6 and N12 flip from "0" to "1", while the rest of the nodes are unaffected. At this point, N6 and N12 can recover to "0" by nodes N3, N7, and N9, and N1 and N11 can recover sequentially. (3) One of the flipped nodes is located in the DNSR-DICE and the other is node Q. Since the node Q and the internal nodes do not affect each other, this case is analogous to the SNU and the latch can recover it.

For TNU, there are five cases: (1) The three flipped nodes located in the same DNSR-DICE. Assuming that nodes N1 and N3 flips from "1" to "0", and node N2 flips from "0" to "1", while the rest of the nodes are unaffected. N1 can recover by N4 and N6, N3 can recover by N8 and N12, and N2 can recover by N3 and N5. (2) Two of the flipped nodes are located in the same DNSR-DICE, and the other flipped node is located in another DNSR-DICE. Assuming that nodes N2, N4, and N6 flip from "0" to "1", then nodes N3 and N5 flip from "1" to "0", while the rest of the nodes are unaffected. In this case, nodes N3 and N5 can recover by nodes N8 and N12, and nodes N2, N4 and N6 can recover sequentially. (3) The three flipped nodes are located in three different DNSR-DICEs. In this case, the DNSR-DICEs do not interfere with each other, which is analogous to the SNU, so that the TNU can self-recover. (4) Two of the flipped nodes are located in the same DNSR-DICE, and the other flipped node is Q. Since the node Q and the internal nodes do not interfere with each other, this situation is similar to the first case of DNU and can self-recover. (5) Two of the flipped nodes are located in two different DNSR-DICEs, and the other flipped node is the output node Q. This situation is analogous to the second case of DNU and can self-recover.

3.4. Fault Injection Experiment

To validate the self-recoverable function of HLTNURL latch for SNU, DNU, and TNU, a fault injection experiment was performed by HSPICE using the PTM 32 nm process. All fault injection experiments were carried out during the windows of vulnerability [16] (i.e., clk = 0, the latch is operating in latch mode) and the fault injected nodes are critical (susceptible) nodes (i.e., internal and output nodes) [17]. The supply voltage, temperature, and clock period are set to 0.9 V, 25 °C, and 6 ns, respectively. All the PMOS transistors had W/L = 64 nm/32 nm, and the NMOS transistors had W/L = 32 nm/32 nm. Some references used TCAD to model the charge sharing effect [5,8], while others used a double-exponential current to model MNU [9–15]. We used a double-exponential current source model [18] to simulate the transient pulses generated by energetic particle bombardment:

$$I(t) = \frac{Q}{(\tau_2 - \tau_1)}\left[\exp\left(-\frac{t}{\tau_2}\right) - \exp\left(-\frac{t}{\tau_1}\right)\right] \quad (1)$$

where $I(t)$ is the transient pulse current at time t, Q refers the collected charge at the node by the energetic particle bombardment, τ_1 is the time constant for initially establishing the iontrack, τ_2 is collection time constant of the junction. τ_1 and τ_2 are set to the same values as [19], specifically τ_1 = 164 ps and τ_2 = 50 ps.

The SNU injections simulation results of the HLTNURL are shown in Figure 10. The red lightning arrow indicates that fault injections are performed. As shown in Figure 10,

current was injected into nodes N1, N6, and output node Q, respectively. We can observe from the figure that the voltage always quickly returns to its initial value whether the node flips from high to low or the opposite, which says our proposed HLTNURL latch is able to self-recover in both cases.

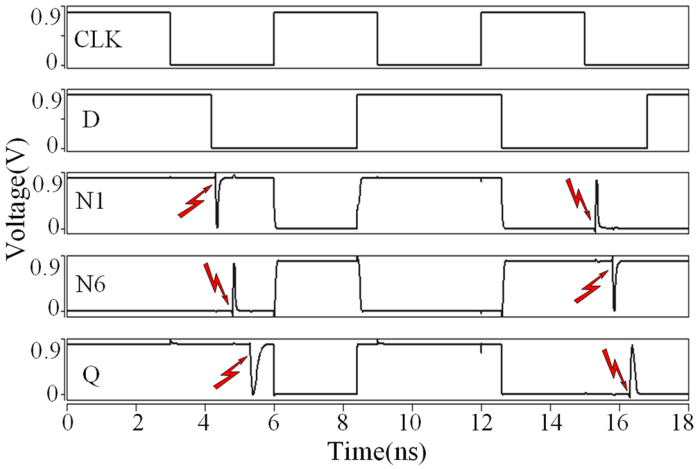


Figure 10. HLTNURL latch simulation: SNU injections.

The DNU injections simulation results of the HLTNURL are shown in Figure 11. As shown in Figure 11, current was injected into (N1, N3) node pair, (N1, N6) node pair, and (N3, Q) node pair, respectively. From the waveform diagram we observe that the HLTNURL is able to quickly self-recover to the initial logic value whether the three node pairs flip from high to low or low to high.

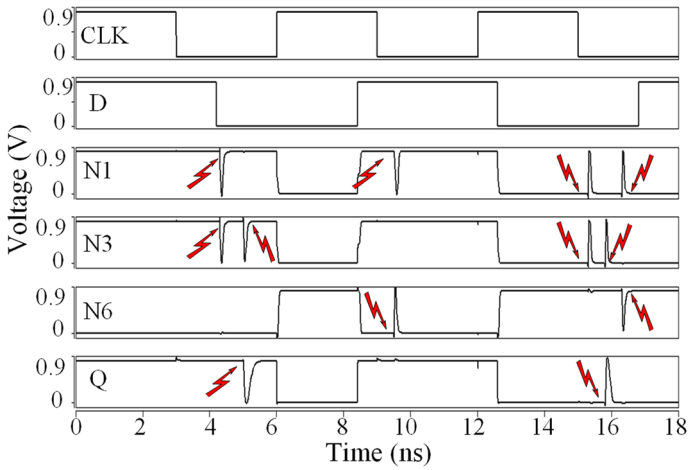


Figure 11. HLTNURL latch simulation: DNU injections.

The TNU injections simulation results of the HLTNURL are shown in Figure 12, where current was injected into {N1, N2, N3}, {N2, N4, N6}, {N3, N5, N9}, {N5, N6, Q} and {N1, N5, Q} in turn, corresponding to the five cases of TNU. We observe that for any case, all the flipped nodes can quickly self-recover to the initial logic value.

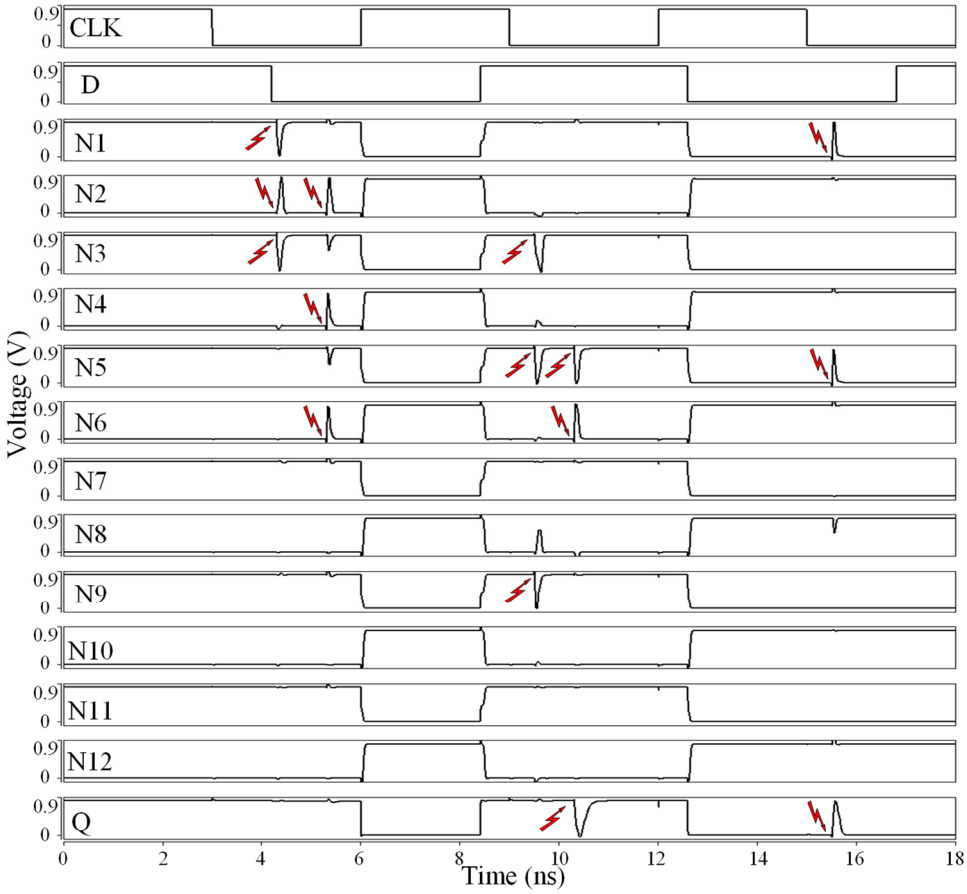


Figure 12. Simulation for TNU injections of HLTNURL latch.

Based on the three experiments and analysis above, we come up with the conclusion that the HLTNURL latch can fully self-recover from TNU in all circumstances.

4. Comparisons and Evaluation

To further evaluate our proposed HLTNURL latch, we conduct a series of comparisons with other latches (as listed in the first column of Table 1), with respect to hardening capability, power consumption, delay, area overhead and PVT fluctuation. All simulations are performed by HSPICE, using the PTM 32 nm process. The supply voltage, temperature, and clock period are set to 0.9 V, 25 °C, and 6 ns, respectively. For a fair comparison, all PMOS transistors were set to W/L = 64 nm/32 nm, and NMOS transistors were set to W/L = 32 nm/32 nm.

Table 1. Robustness comparisons between the existing TNU latches and proposed HLTNURL latch.

Latch	SNU Tolerant	SNU Recoverable	DNU Tolerant	DNU Recoverable	TNU Tolerant	TNU Recoverable
LEAP-DICE	YES	YES	YES	NO	NO	NO
LCTNUT	YES	YES	YES	NO	YES	NO
TNU-Latch	YES	YES	YES	NO	YES	NO
LOCTNUTRL	YES	YES	YES	NO	YES	NO
TNUTL	YES	YES	YES	NO	YES	NO
TNURL	YES	YES	YES	YES	YES	YES
LCTNURL	YES	YES	YES	YES	YES	YES
HTNURL	YES	YES	YES	YES	YES	YES
HLTNURL	YES	YES	YES	YES	YES	YES

4.1. Robustness Comparison

The comparison of the latch hardening capabilities is shown in Table 1. We observe that the designed HLTNURL latch can achieve a full self-recover of the TNU, and its hardening capability is further improved in comparison with the LCTNUT latch, the TNU-Latch, the LOCTNUTRL latch, and the TNUTL latch.

4.2. Performance Overhead Comparison

The power and delay data of each latch are simulated, along with the area and APDP. Table 2 shows the comparison between the HLTNURL latch and the other TNU latches, with respect to the performance and area cost. In Table 2, "Q_{crit}" means critical charge. "Delay" means the average transmission delay from the input signal D to the output signal Q in the transparent mode. "Power" means the average power consumption of the entire circuit within 18 ns with the same input conditions. "APDP" refers to the area-power-delay product for comprehensively evaluating these latches, where the smaller the APDP is, the better the performance of the circuit will be [18]. The latch area is obtained from the equivalent number of the Unit Size Transistors (USTs) [20]:

$$\mathrm{UST} = \sum_{i=1}^{n} (W/L)_i \tag{2}$$

Table 2. Performance and area cost comparisons among the existing TNU latches and proposed HLTNURL latch.

Latch	Q_{crit}/fC	Power/μW	Delay/ps	Area (USTs)	$10^{-3} \times$ APDP
Unhardened	7.64	0.144	15.19	15	0.033
LCTNUT	9.73	0.64	6.28	72	0.289
TNU-Latch	22.82	1.02	113.75	123	14.271
LOCTNUTRL	3.72	0.55	2.29	75	0.0945
TNUTL	18.75	0.45	11.62	54	0.282
TNURL	12.56	1.47	11.99	210	3.701
LCTNURL	5.13	0.803	9.39	126	0.95
HTNURL	4.6	0.434	11.62	120	0.605
HLTNURL	7.96	0.609	2.23	150	0.185

Although latches with higher critical charges are not susceptible to interference from high-energy particle impacts, the HLTNURL latch is still the most robust since the latch can quickly self-recover to the original logical value even if the node flips. Meanwhile, we observe that the proposed HLTNURL latch has the best overall performance of the latch structure as it has the lowest delay and APDP of all TNU self-recoverable latches due to the fast-path technique. To achieve a better hardening effect, the area overhead of this structure is relatively large, but the power consumption is effectively controlled by using the clock gating technique.

To more intuitively compare the proposed latch with other TNU self-recoverable latches, the power, delay, area and APDP were calculated by Equations (3) and (4). The results are presented in Table 3.

$$\Delta = (\textit{proposed latch} - \textit{compared latch})/\textit{compared latch} \times 100\% \tag{3}$$

$$\textit{Average} = (\textit{proposed latch} - \textit{compared latch average})/\textit{compared latch average} \times 100\% \tag{4}$$

Table 3. Relative changes of performance and area cost comparisons of TNU-recoverable latches.

Latch	ΔPower	ΔDelay	ΔArea	ΔAPDP
TNURL	−58.57%	−81.4%	−28.57%	−95%
LCTNURL	−24.16%	−76.25%	19.05%	−80.53%
HTNURL	41.63%	−80.81%	25%	−69.42%
Average	−32.41%	−79.73%	−1.32%	−88%

Table 3 shows that compared to the other three TNU self-recoverable latches, the HLTNURL latch can reduce the power consumption by 32.41%, the delay by 79.73%, the area by 1.32%, and the APDP by 88% on average. The TNURL latch, the LCTNURL latch, and the HTNURL latch all achieve the TNU self-recovery function through the feedback loop. The output node Q is the internal node of the feedback loop, so they all have a relatively large delay. In contrast, the proposed HLTNURL latch utilizes the DNU self-recovery function of the DNSR-DICE unit, hardening the node through redundant interlock techniques to perform the TNU self-recovery function. As there is no feedback loop, its delay is minimal. Although the area overhead of the proposed HLTNURL latch is relatively large, its power dissipation is effectively controlled with the clock gating technique.

4.3. Effect of PVT Variations on Latches

With the continuous reduction of transistor size, nanoscale digital circuits become increasingly sensitive to PVT variations. This section mainly introduces the power consumption and delay analysis of seven TNU latches and the proposed HLTNURL latch under PVT variations.

4.3.1. Comparison of Process Variations

The power cost and delay of the TNU latches are simulated using five process corners, FF, FS, TT, SF, and SS, and the results are shown in Figure 13. We observe from Figure 13 that the delay and power dissipation of the latch vary with different process corners: FF process corner offers the maximum power dissipation and minimum delay, while SS process corner provides the minimum power dissipation and maximum delay. Among them, the power dissipation variation of the HLTNURL latch is relatively small, and the delay variation is the smallest.

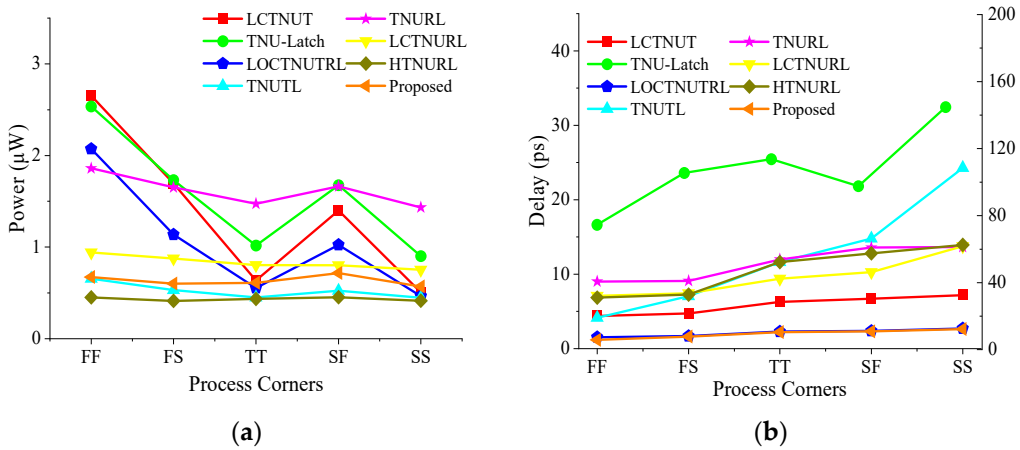
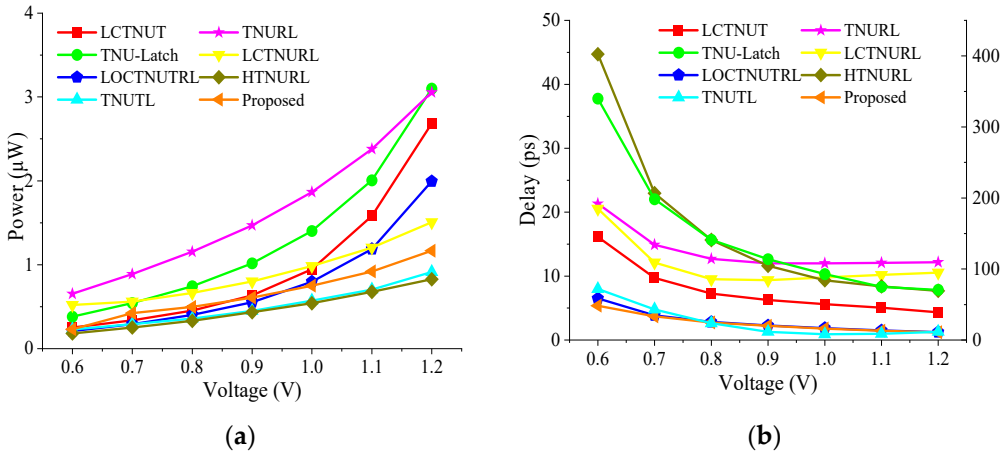


Figure 13. Process variations effect on the latches' performances: (**a**) process corners vs. power; (**b**) process corners vs. delay.

4.3.2. Comparison of Voltage Variations

Figure 14 shows the power cost and delay of the latches at different supply voltages. The supply voltage range is 0.6 V to 1.2 V. We observe that the power consumption of the latches increases, and the delay decreases with increasing supply voltage, because power

consumption is proportional to the square of the supply voltage, while higher voltages lead to higher currents and thus to lower delays. Compared with the other TNU latches, the power consumption variation of the HLTNURL latch is relatively small, and the delay variation is the smallest.

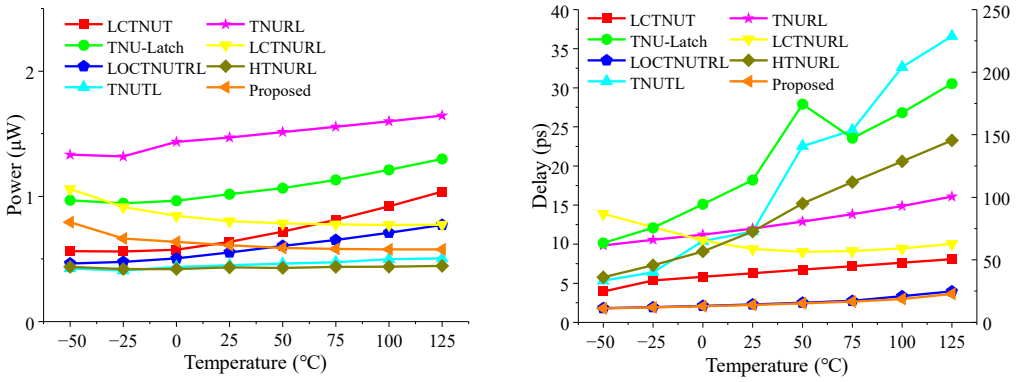


(**a**) (**b**)

Figure 14. Voltage variations effect on the latches' performances: (**a**) supply voltage vs. power; (**b**) supply voltage vs. delay.

4.3.3. Comparison of Temperature Variations

The effects of temperature change on the power consumption and delay of the latches are shown in Figure 15. The temperature is varied from −50 °C to 125 °C. As shown in Figure 15, that the power dissipation of the HLTNURL latch decreases slightly with the increase of temperature, and the delay increases slightly with the increase of temperature, because the increase of temperature will lead to the decrease of carrier mobility. However, compared with the other TNU latches, its power consumption variation is still relatively small, and the delay variation is still the smallest.



(**a**) (**b**)

Figure 15. Temperature variations effect on the latches' performances: (**a**) temperature vs. power; (**b**) temperature vs. delay.

Based on the above experiments and analysis, we conclude that comparing with other TNU latches, the proposed HLTNURL latch is less sensitive to PVT variations.

5. Conclusions

The continuous decrease in the size of the process brings a high probability of TNU. Therefore, in this paper, we propose the HLTNURL latch, which uses DNSR-DICEs and CG-based C-element as the basic structure. Three DNSR-DICE modules are connected by

redundant interlock techniques to achieve TNU self-recovery. The clock gating technique and fast path technique are used to reduce power dissipation and delay. The HSPICE simulation results show that the HLTNURL can tolerate SNU, DNU, and TNU in any case, and can recover all flipped nodes to their correct logic values. Compared with existing TNU-tolerant latches, the HLTNURL latch has better performances in terms of power consumption, delay, and APDP. The proposed latch also has a lower sensitivity to PVT variations, which is suitable for highly reliable digital circuits.

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