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Design of a Capacitorless DRAM Based on Storage Layer Separated Using Separation Oxide and Polycrystalline Silicon

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Abstract: In this study, a capacitorless one-transistor dynamic random-access memory (1T-DRAM) based on a polycrystalline silicon (Poly-Si) metal-oxide-semiconductor field-effect transistor (MOSFET) with a storage layer separated using a separation oxide was designed and analyzed using technology computer-aided design (TCAD). The channel and storage layers were separated using a separation oxide to improve the inferior retention time of the conventional 1T-DRAM, and we adopted the underlap structure to reduce Shockley-Read-Hall recombination. In addition, poly-Si, which has several advantages, including low manufacturing cost and availability of high-density three-dimensional (3D) memory arrays, is used to easily fabricate silicon-on-insulator (SOI)-like structures. Accordingly, we extracted memory performance by analyzing the effect of grain boundary (GB). The proposed 1T-DRAM achieved a sensing margin of 14.10 μA/μm and a retention time of 251 ms at T = 358 K, even in the existence of a GB.

Keywords: one-transistor dynamic random-access memory; metal-oxide-semiconductor field-effect transistor; polycrystalline silicon

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1. Introduction

Conventional one-transistor (1T) one-capacitor (1C) dynamic random-access memory (DRAM) is a key product of the semiconductor industry. It comprises one transistor for reading and writing operations and one capacitor for storing charges. Recently, the transistor size has continued to shrink for improved performance, such as higher speed and lower power consumption, and severe difficulties have arisen in capacitor fabrication. Therefore, many researchers have proposed 1T-DRAM without capacitors to replace conventional DRAM [1–10]. The 1T-DRAM utilizes the floating body effect of a partially depleted silicon-on-insulator (SOI) to retain memory performance [11]. 1T-DRAM program methods include impact ionization, gate-induced barrier lowering, and band-to-band tunneling (BTBT), and excess holes are stored in the floating body [12–14]. However, SOI wafers are significantly costly and difficult to fabricate. A low-cost method for forming SOI-like structures using polycrystalline silicon (poly-Si) has been proposed [15]. In addition, poly-Si can replace conventional silicon fabrication processes and be applied to three-dimensional (3D) memory arrays. However, even if the manufacturing problem of SOI structures is addressed, miniaturization of the device results in an insufficient charge storage region. This increases the recombination/generation rate owing to the strong electric field between the body and source/drain junction, which degrades the retention time.

In this study, we present a 1T-DRAM based on poly-Si with a storage layer separated using a separation oxide. The proposed 1T-DRAM uses an underlap structure and separation oxide to improve the retention time. In addition, because the poly-Si used to fabricate SOI-like structures in a simple manner is an aggregate of grains [16,17], a grain

boundary (GB) is formed where different grains contact each other. Therefore, the memory characteristics were analyzed assuming that a single GB existed at the center of the channel and storage layers. The memory performance of the proposed 1T-DRAM was investigated through a two-dimensional simulation and evaluated in terms of sensing margin and retention time.

2. Device Structure and Simulation

Figure 1 shows a cross-sectional view of the poly-Si-based 1T-DRAM with a storage layer separated using a separation oxide. The program, erase, and hold operations are performed by the top gate, while conventional metal-oxide-semiconductor field-effect transistor (MOSFET) operations are performed by the bottom gate. The bottom gate uses a heavily doped poly-Si to minimize the difficulty in metal-based gate fabrication. The geometric parameters are summarized in Table 1. The underlap structure and separation oxide are considered to be the main parameters that influence the memory performance of 1T-DRAM. The underlap structure reduces the electric field between the storage layer and source/drain. The separation oxide separates the channel and storage layers, enabling the excess holes to be stored more effectively.

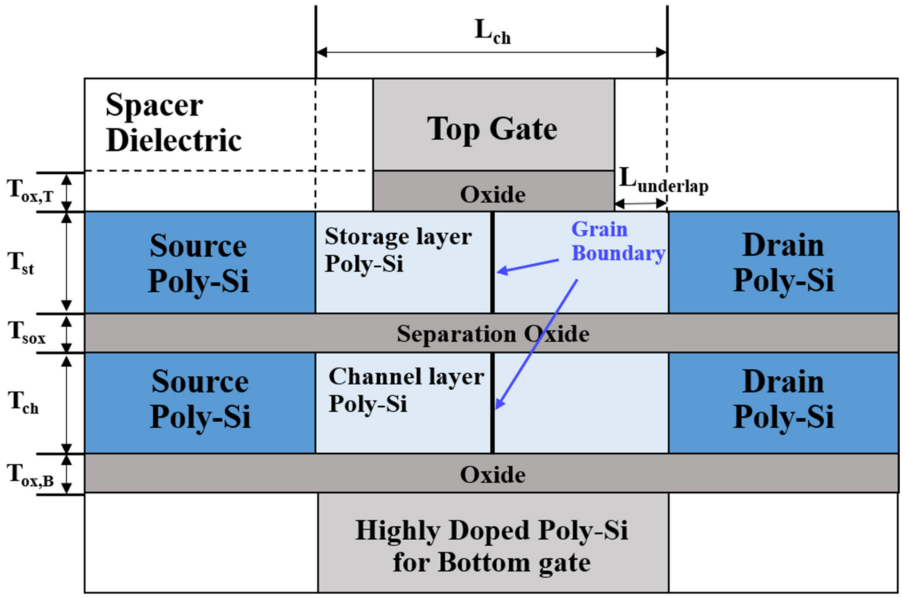


Figure 1. Poly-Si based 1T-DRAM with storage layer separated using separation oxide.

Table 1. Parameters for the proposed 1T-DRAM.

Parameter	Value
Chanel Length (L_{ch})	70 nm
Underlap Length ($L_{underlap}$)	0–20 nm
Top Gate Oxide (HfO_2) Thickness ($T_{ox,T}$)	8 nm
Channel Layer Thickness (T_{ch})	8 nm
Separation Oxide (SiO_2) Thickness (T_{sox})	1–30 nm
Storage Layer Thickness (T_{st})	8 nm
Bottom Gate Oxide (SiO_2) Thickness ($T_{ox,B}$)	3 nm
n^+-Source Doping Concentration	1×10^{20} cm^{-3}
n^+-Drain Doping Concentration	1×10^{20} cm^{-3}
p-Channel Layer Doping Concentration	1×10^{16} cm^{-3}
p^+-Storage Layer Doping Concentration	1×10^{18} cm^{-3}
p^+-Poly-Si Bottom gate doping concentration	1×10^{18} cm^{-3}
Top Gate Work function	5.20 eV

Figure 2 shows the main fabrication steps of a proposed device crystallized via excimer laser crystallization (ELC) [18]. First, SiO_2 is deposited and the bottom gate is etched. Second, amorphous silicon (a-Si) is deposited by LPCVD and activated by excimer laser irradiation to form a poly-Si bottom gate. Third, SiO_2 is deposited to form a bottom gate oxide. Fourth, after deposition a-Si through LPCVD, a channel layer is formed through ELC. Fifth, a hard mask is formed through SiO_2 deposition and etching. Sixth, ion implantation is performed to form the n-type source and drain of the channel layer. Seventh, SiO_2 is deposited to form a separation oxide. Eighth, after deposition a-Si by LPCVD, a storage layer is formed through ELC. Ninth, the top gate oxide is formed through HfO_2 deposition and etching. Tenth, the metal top gate was deposited. Finally, ion implantation was performed to form the n-type source and drain of the storage layer. The device can be fabricated through the above process. In addition, through silicon via process (TSV) is performed to connect the channel layer and the storage layer. The stack structure requires high temperature processing, which can threaten dopant diffusion. These manufacturing challenges can be overcome using ELC.

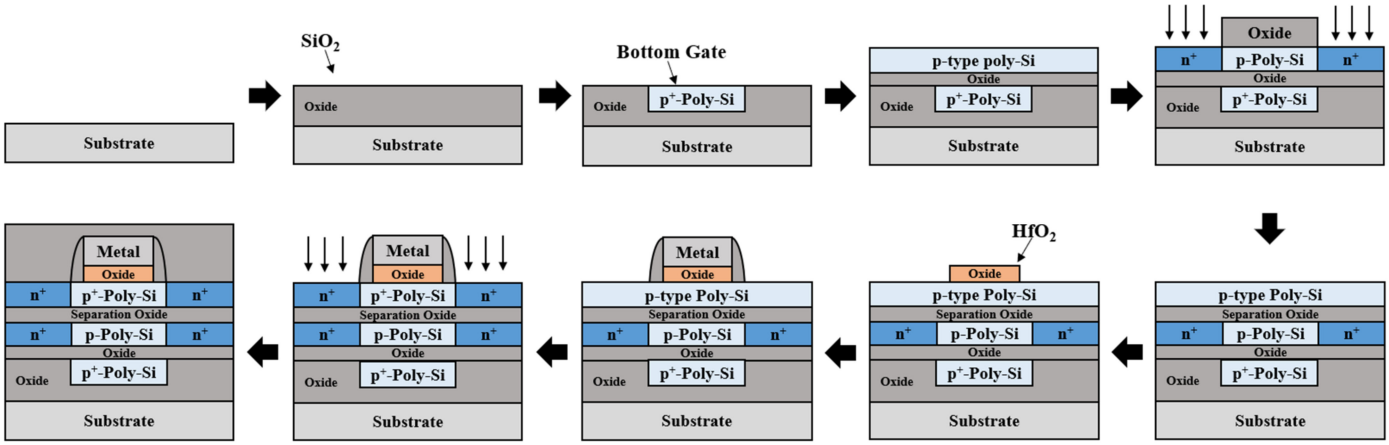


Figure 2. Key fabrication steps of the proposed 1T-DRAM crystallized via excimer laser crystallization [18].

The work function of the top gate is 5.20 eV. The top gate work function increases the energy band of the storage layer, thereby generating a potential well that can store additional holes. The proposed 1T-DRAM consists of an 8 nm thick storage layer and the channel layer. The doping concentrations of the storage and channel layers are 1×10^{18} and 1×10^{16} cm^{-3}, respectively, and that of the source/drain regions is 1×10^{20} cm^{-3}. The channel length is set to 70 nm. A long channel is used because the longer the channel, the wider energy band of the hole storage area, which is advantageous for hole storage [19]. The top gate dielectric is designed with 3 nm thick HfO_2. This is because the high dielectric constant of 22 increases the effect of the top gate controllability. Accordingly, the effect of the top gate work function on the storage layer is increased, so that the hole can be stored more effectively. For high accuracy, physical models such as Fermi-Dirac statistical, Shockley-Read-Hall (SRH) recombination, Auger recombination, nonlocal BTBT, and trap-assisted tunneling (TAT) models, doping-dependent and field-dependent mobility models, bandgap narrowing model, and quantum confinement effect were used in the simulations [20]. The design and analysis of the device were performed using Sentaurus technology computer-aided design (TCAD) simulation tool. Furthermore, the GB trap distribution of poly-Si was used as the calibrated data, which is reported in [15] (Figure 3).

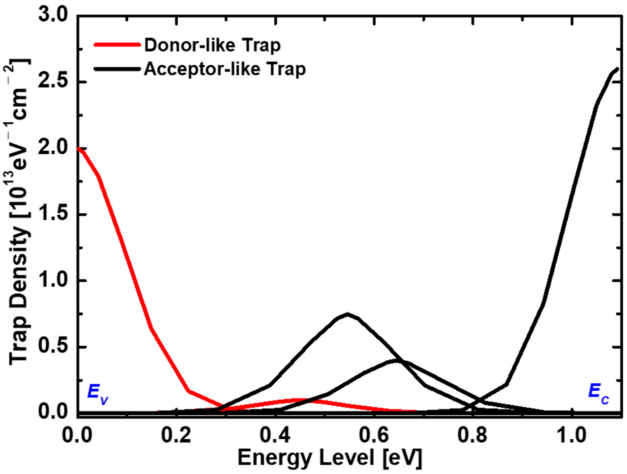
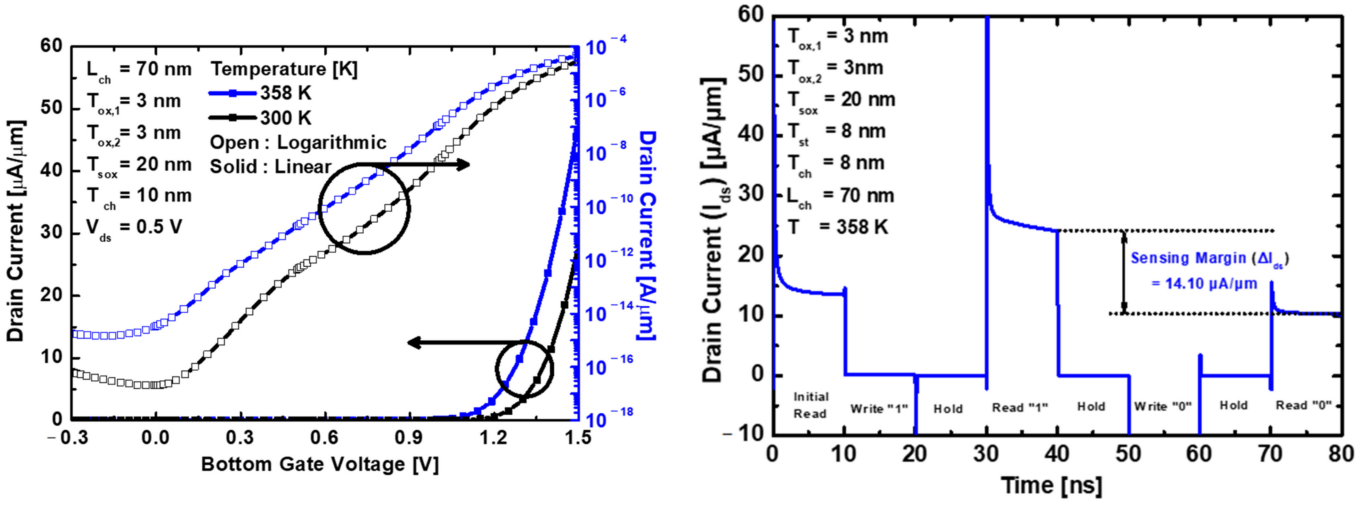


Figure 3. GB trap distribution calibrated using experimental data reported in [15].

3. Results

Figure 4a shows the drain current (I_{ds}) versus gate voltage ($V_{gs,B}$) transfer characteristics of the proposed device. At different temperatures of 300 K and 358 K, the threshold voltage (V_{th}) is 1.00 V and 1.12 V, respectively. The heavily doped poly-Si bottom gate performs the conventional MOSFET operation. Although the gate controllability is reduced compared to that of the metal-based gate, this gate structure can be easily fabricated in a 3D stacked manner.



(**a**) (**b**)

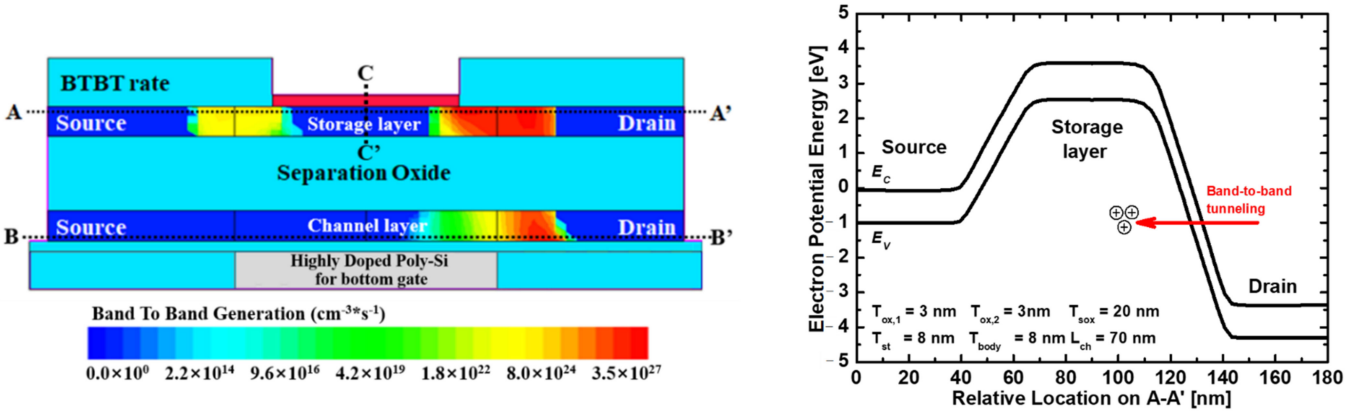
Figure 4. (**a**) Linear (solid symbol) and logarithmic (open symbol) I_{ds}-$V_{gs,B}$ transfer characteristics for the proposed 1T-DRAM at V_{ds} = 0.5 V. (**b**) Transient characteristic of the proposed 1T-DRAM.

Figure 4b shows the transient characteristics of the proposed device. Table 2 summarizes the bias conditions for the memory performance of 1T-DRAM. The program operation uses the BTBT mechanism. Generated excess holes are accumulated in the storage layer. The erase operation reduces the potential barrier of the storage layer and a negative voltage is applied to drain. Thus, accumulated excess holes are removed by drifting towards the drain. As shown in Figure 4b, the proposed device extracted a sensing margin of 14.10 μA/μm at a temperature of 358 K.

Table 2. Operating bias scheme for memory performance.

	Write "1" (Program)	Write "0" (Erase)	Read	Hold
Top Gate Voltage ($V_{gs,T}$)	−3.2 V	0.5 V	0.0 V	−0.3 V
Bottom Gate Voltage ($V_{gs,B}$)	0.0 V	0.0 V	1.3 V	0.0 V
Drain Voltage (V_{ds})	3.0 V	−0.7 V	0.0 V	0.0 V

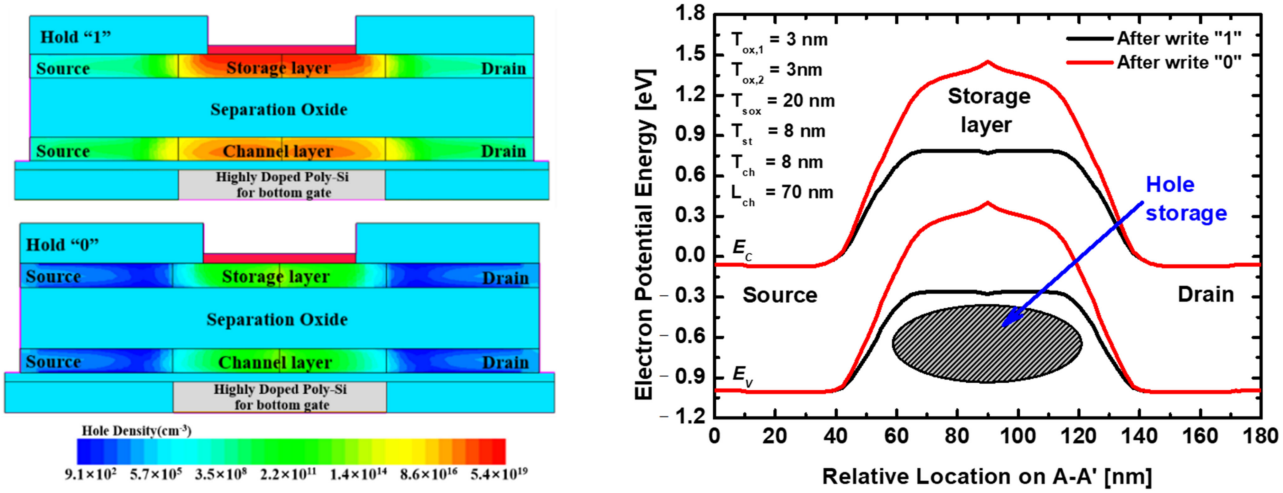
Figure 5a shows the BTBT rate of the proposed device during the program operation. The program operation is performed using BTBT between the storage layer and drain. The program operation of the tunneling method is advantageous because it consumes less power than that of the impact ionization method. As shown in Figure 5b, the top gate voltage ($V_{gs,T}$) = −3.2 V and V_d = 3.0 V are applied to form a thin tunneling barrier between the storage layer and drain. BTBT occurs through a thin tunneling barrier, and the generated excess holes accumulate below the valence band of the top gate oxide. In addition, the stored excess holes are maintained owing to the negative voltage and high work function.



(**a**) (**b**)

Figure 5. (**a**) Simulation profiles of the proposed 1T-DRAM during the program operation showing BTBT rate. (**b**) Energy band diagram of the storage layer. The energy band is extracted at 2 nm below the top gate oxide.

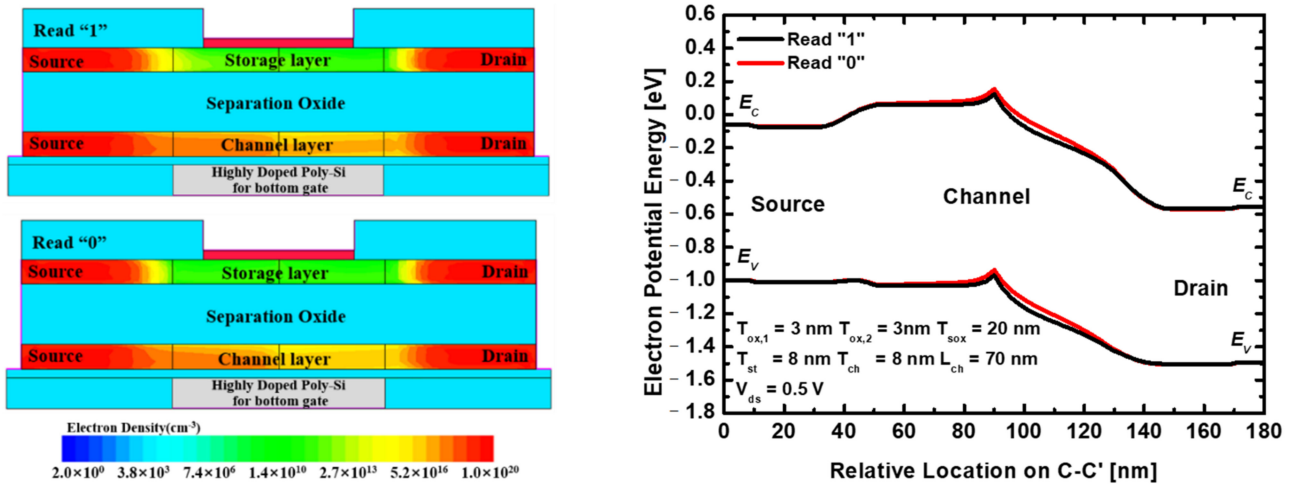
Figure 6a shows the hole density of the proposed device during the hold operation. The hold "1" state is defined after a program operation, and the hold "0" state is defined after an erase operation. As shown in Figure 6a, the hole density is different between hold "1" and hold "0" states. Figure 6b shows the energy band diagram of the storage layer during hold "1" and hole "0" operations in the storage layer. In the hold "1" state, an additional positive voltage is applied to the storage layer by the stored excess holes, reducing the potential barrier than in the hold "0" state. Moreover, a hold voltage of $V_{gs.T}$ = −0.3 V is applied during hold operation to store excess holes more effectively.



(**a**) (**b**)

Figure 6. (**a**) Simulation profile of the proposed 1T-DRAM during the hold operation showing hole density. (**b**) Energy band diagram of the storage layer during the hold operation. The energy band is extracted at 2 nm below the top gate oxide.

Figure 7a shows the electron density of the proposed device during the read operations. During the read operation, the current flows in the channel layer when $V_{gs,B}$ = 1.3 V and V_{ds} = 0.5 V. Figure 7a shows the difference in electron density in the channel layer. As shown in Figure 7b, when excess holes are stored in the storage layer, they affect the potential barrier of the channel layer and have the same effect as that of lowering of V_{th} by applying an additional voltage. However, after the stored holes are erased, the potential barrier of the channel layer increases owing to the low hole density of the storage layer. This causes a drain current difference between read "1" and read "0" states, defined as the sensing margin.



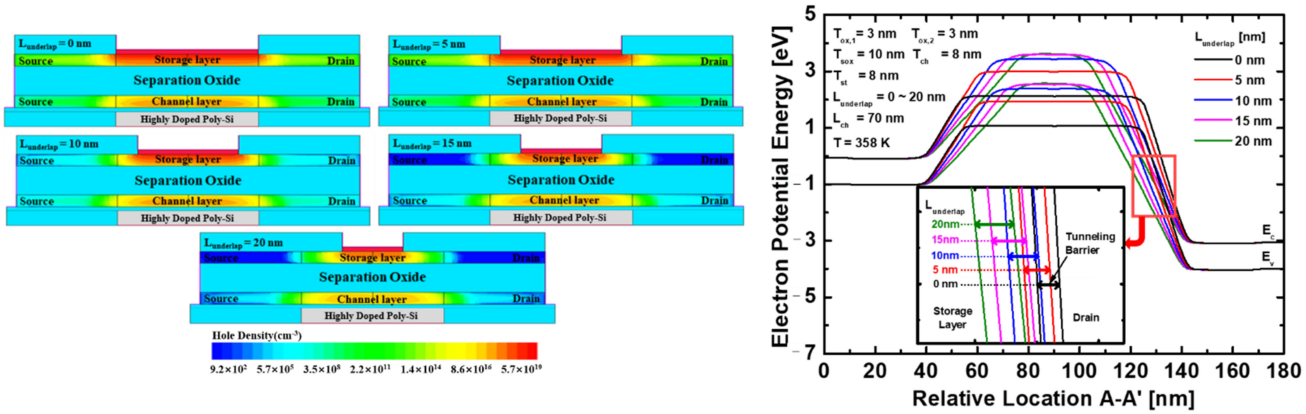
(**a**) (**b**)

Figure 7. (**a**) Simulation profile of the proposed 1T-DRAM during the read operation showing electron density. (**b**) Energy band diagram of the channel layer during the read operation. The energy band is extracted at 2 nm above the bottom gate oxide.

3.1. Effect of $L_{underlap}$ Variation

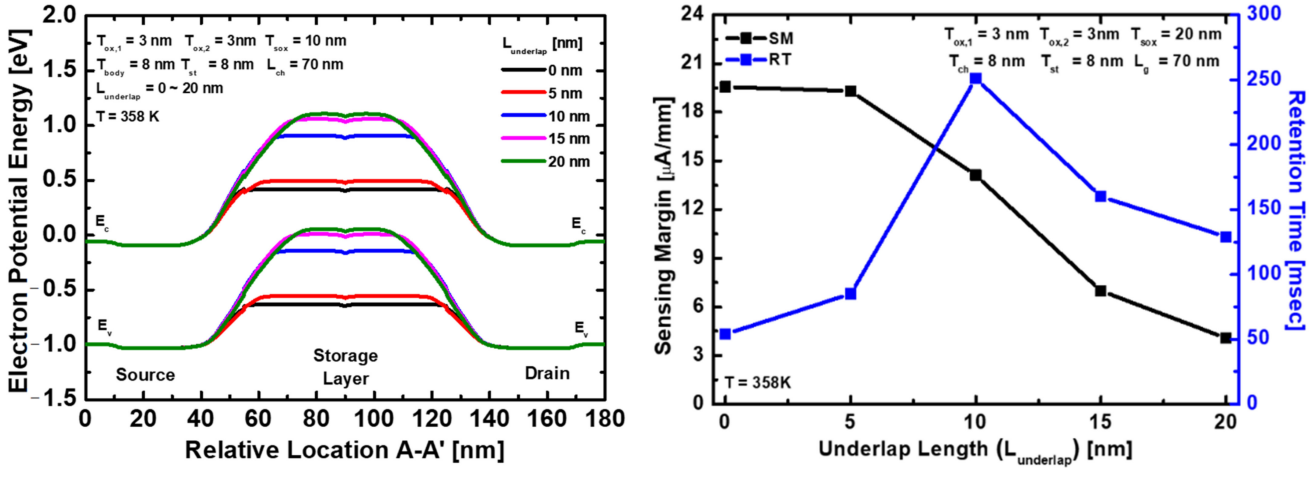
It is important to analyze the retention time among the memory performance of 1T-DRAM. The retention time is the time it takes for accumulated excess holes by recombination/generation during hold operation to return to a steady state after program/erase operation. The retention time of 1T-DRAM is defined as the hold time, which is 50% of the

sensing margin. Figure 8a shows the hole density of the proposed device depending on the $L_{underlap}$ in the hold "1" state. As $L_{underlap}$ increases, the influence of the top gate on the storage layer and the source/drain junction decreases. Therefore, the recombination rate of the storage layer is reduced and the retention time is increased. However, when the effect of the top gate is reduced, it is difficult to form a sufficient tunneling barrier for BTBT to occur at the storage layer and drain junction during program operation, as shown in Figure 8b. This eventually decreases the hole density in the storage layer, as shown in Figure 8a. Moreover, the sensing margin decreases because the hole density in the storage layer is insufficient. On the other hand, when $L_{underlap}$ decreases, the tunneling barrier between the storage layer and drain becomes very thin and excess holes are generated, resulting in a decreased potential barrier of the storage layer, as shown in Figure 9a. This increases the rate of recombination between the storage layer and the source/drain so that the retention time is reduced. Figure 9b shows the sensing margin and retention time depending on the $L_{underlap}$ of the proposed device. At a temperature of 358 K, the sensing margin reached the peak value at $L_{underlap}$ = 0 nm, and the retention time reached the peak value of 251 ms at $L_{underlap}$ = 10 nm. In addition, this performance adheres to the international roadmap for devices and systems (IRDS) [21].



(**a**) (**b**)

Figure 8. (**a**) Simulation profile of the proposed 1T-DRAM with different Lunderlap during hold "1" operation showing hole density. (**b**) Energy band diagram of the storage layer with different Lunderlap during program operation. The energy band is extracted 2 nm below top gate oxide.



(**a**) (**b**)

Figure 9. (**a**) Energy band diagram of the storage layer with different $L_{underlap}$ during hold "1" operation. The energy band is extracted at 2 nm below the top gate oxide. (**b**) Variations in sensing margin and retention time with $L_{underlap}$ of proposed 1T-DRAM.

3.2. *Effect of T_{sox} Variation*

The conventional 1T-DRAM stores excess holes in a floating body. However, the stored holes tend to decrease rapidly during the hold and read operations, limiting the retention time. Therefore, the proposed 1T-DRAM effectively stores excess holes and reduces the SRH recombination rate by separating the channel and storage layers with a separation oxide to improve the retention time.

Figure 10a shows the SRH recombination rate of the proposed device depending on the T_{sox} in the hold "1" state. As T_{sox} decreases, the recombination rate increases because the source/drain junction of the storage layer is influenced by the electric field of the bottom gate. As shown in Figure 10b, when T_{sox} = 1 nm, the SRH recombination rate attains a peak value and decreases gradually. However, when T_{sox} exceeds 20 nm, the effect between the storage and channel layers and the retention time decreases. In terms of the sensing margin, as T_{sox} increases, the effect of the top gate work function on the channel layer gradually decreases, and the potential barrier of the channel layer decreases, as shown in Figure 11a. Consequently, the read current and sensing margin increase. However, when T_{sox} > 15 nm, the relationship between the storage and channel layers weakens. Therefore, the excess holes stored in the storage layer cannot be applied as an additional positive voltage. Therefore, the difference between the read "1" and "0" currents decrease. Figure 11b shows the sensing margin and retention time depending on T_{sox} of the proposed device. At a temperature of 358 K, the sensing margin achieved a peak value of 15.60 μA/μm at T_{sox} = 15 nm, and the retention time achieved a peak value of 251 ms at T_{sox} = 20 nm. Additionally, when T_{sox} = 20 nm, a sufficient sensing margin of 14.10 μA/μm is extracted. Accordingly, optimal memory performance is obtained at T_{sox} = 20 nm.

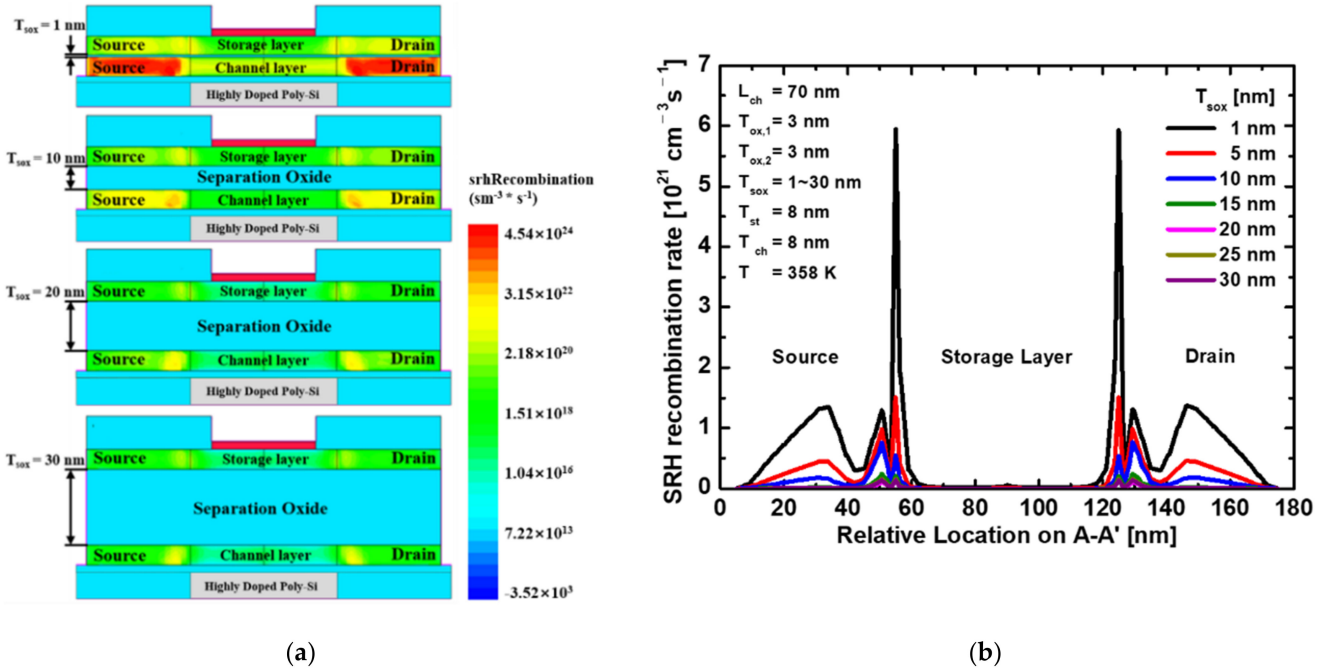
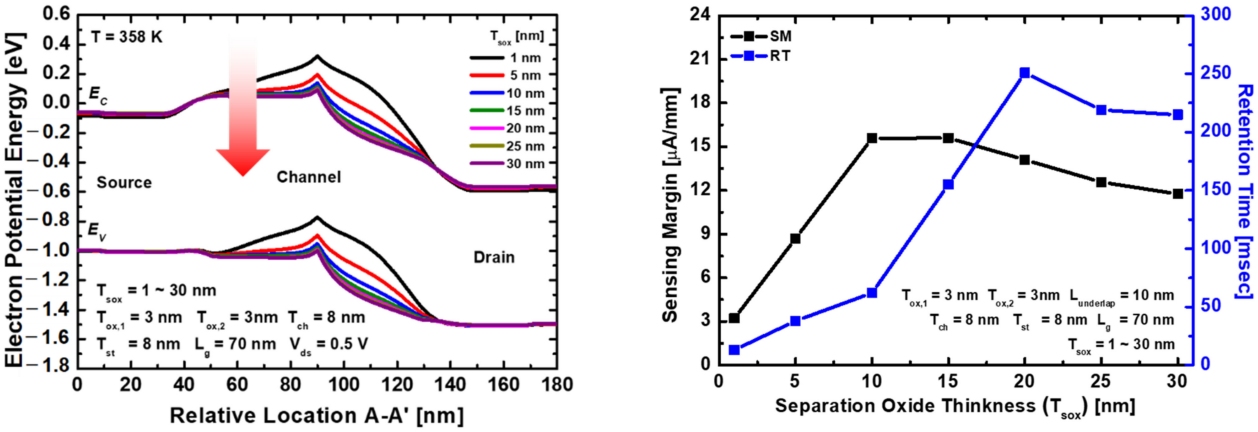


Figure 10. (**a**) Simulation profile of the 1T-DRAM with different T_{sox} during hold "1" operation showing SRH recombination. (**b**) SRH recombination rate of storage layer with different T_{sox} during the read operation. The energy band is extracted at 2 nm below the top gate oxide.

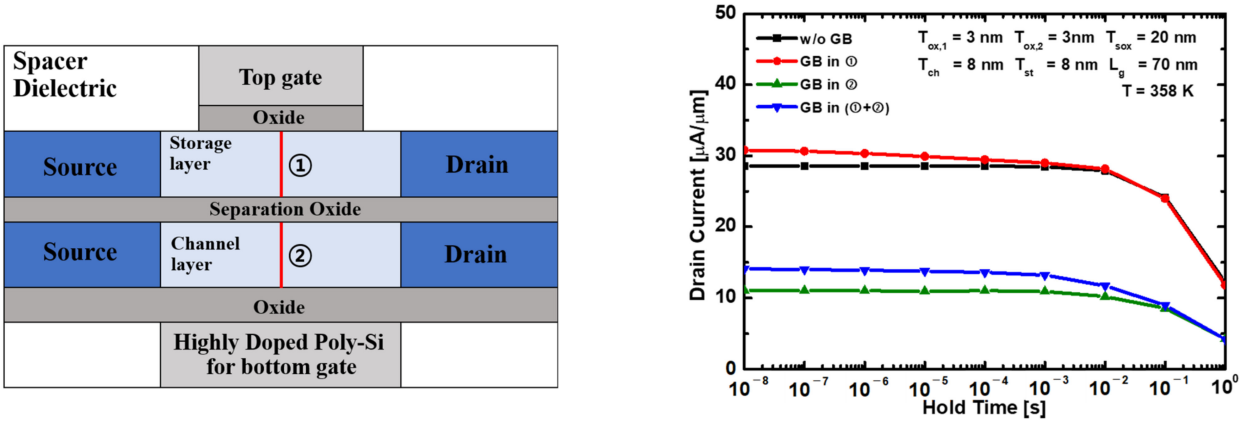


(**a**) (**b**)

Figure 11. (**a**) Energy band diagram of the channel layer with different T_{sox} during the read operation. The energy band is extracted at 2 nm above the bottom gate oxide. (**b**) Variations in sensing margin and retention time with T_{sox} of proposed 1T-DRAM.

3.3. Effect of GB Location

Because the proposed device uses poly-Si to fabricate an SOI-like structure easily, it is necessary to analyze its effect on the GB. The grain size of poly-Si can be adjusted according to the growth and annealing temperatures. Therefore, it can be significantly larger than that of a recently scaled-down device. When investigating the impact of the GB, it is assumed that a single GB is located at the center of the storage and channel layers, as shown in Figure 12a. Figure 12b shows the memory characteristics based on GB location. The sensing margins and retention times at GB locations are summarized in Table 3.



(**a**) (**b**)

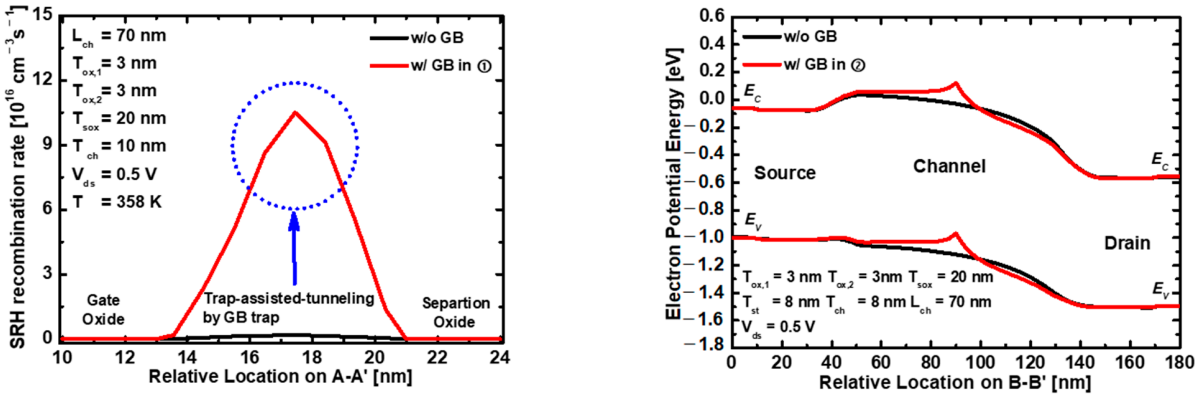
Figure 12. (**a**) Cross-section depending on the GB location of the proposed 1T-DRAM. (**b**) Variation of currents in read "1" and read "0" status depending on the GB position.

Table 3. Memory performance depending on the GB location of the proposed 1T-DRAM.

	Sensing Margin [μA/μm]	Retention Time [ms]
w/o GB	28.58	648
GB in ①	30.79	507
GB in ②	11.09	484
GB in (① + ②)	14.10	251

When a GB exists in the storage layer, the sensing margin is larger than that without a GB in the storage layer. This is because the difference between read "1" and read

"0" increases owing to the hole/electrons captured by the GB trap of the storage layer. However, the retention time is reduced by the TAT mechanism through GB traps, as shown in Figure 13a. This is because the recombination/generation rates of hole are increased by the TAT mechanism. When a GB exists in the channel layer, electrons are captured in the region where the GB is located; therefore, potential barriers increase, as shown in Figure 13b. The increased potential barrier disturbs the current flowing from the source to the drain, significantly decreasing the sensing margin. In addition, the reduced sensing margin degrades the retention time. As a result, the memory performance of the proposed 1T-DRAM exhibits a superior performance of 28.58 μA/μm sensing margin and 648 ms retention time without a GB. Furthermore, when the GB exists in the storage and channel layers, the sensing margin and retention time are 14.10 μA/μm and 251 ms, respectively, which correspond to an excellent memory performance.



(**a**) (**b**)

Figure 13. (**a**) SRH recombination of the hold state with and without GB in ①. The energy band is extracted at the center of the storage region. (**b**) Energy band diagram of the read operation with and without GB in ②. The energy band is extracted at 2 nm above the bottom gate oxide.

Table 4 presents the previously reported memory performance of the 1T-DRAM. The 1T-DRAM developed in this study exhibits a superior memory performance at T = 358 K compared with other devices.

Table 4. Memory performances of various 1T-DRAM reported in the literature.

No	Structure	Sensing Margin [μA/μm]	Retention Time [ms]
1.	Junctionless FinFET-Based 1T-DRAM (Vertical GB) [22]	11.7	64.27
2.	Junctionless FinFET-Based 1T-DRAM (Horizontal GB) [22]	11.3	148
3.	SiGe GAA JLFET-Based 1T-DRAM [18]	0.39	10
4.	Double-gate Si/SiGe 1T-DRAM [23]	6.16	131
5.	Dopingless 1T-DRAM [24]	0.012	170
6.	Dual Gate 1T-DRAM (w/GB) [25]	6.58	340.1
7.	Nanotube 1T-DRAM (w/GB) [26]	422	120
8.	Ge/GaAs TFET-Based 1T-DRAM [27]	1.11	120
9.	This study (w/o GB)	28.58	648
10.	This study (w/GB)	14.10	251

4. Conclusions

In this study, a poly-Si-based 1T-DRAM with a storage layer separated using a separation oxide was designed and analyzed using TCAD simulation. In addition to analyzing the effect of GB on memory performance, the important parameters $L_{underlap}$ and T_{sox} were evaluated. The proposed 1T-DRAM obtained high retention time despite the effect of GB because the storage efficiency was improved by separating the channel and the storage layers with separation oxide. As a result, the optimized parameters are L_{ch} = 70 nm, $L_{underlap}$ = 10 nm, and T_{sox} = 20 nm, achieving a sensing margin of 14.10 μA/μm and a high retention time of 251 ms at T = 358 K. Therefore, the proposed 1T-DRAM has the potential to replace the conventional 1T-1C DRAM.

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