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A New Gate Driver for Suppressing Crosstalk of SiC MOSFET

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Abstract: High switching-speed Silicon Carbide Metal-Oxide-Semiconductor Field-Effect Transistor (SiC MOSFET) has serious crosstalk issues. During the turn-ON transition and turn-OFF transition of the active switch in a phase-leg configuration, the voltage drops across the common-source inductor and the displacement current of the gate-drain capacitor of the OFF-state switch induce a spurious pulse on its gate-source voltage. This paper proposes a new gate driver using two Bipolar Junction Transistors (BJTs) and one diode to connect the gate terminal of SiC MOSFET and the negative driver voltage, which provides a low impedance path to bypass the displacement current of the gate-drain capacitor when crosstalk issues occur. The simulation results prove the proposed driver is valid on suppressing the crosstalk issue. The comparisons between the prior drivers and the proposed driver show the superiority of the proposed driver. Finally, the proposed gate driver is successfully implemented and experimentally verified on a 1.1 kW synchronous buck prototype.

Keywords: crosstalk; SiC MOSFET; driver

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1. Introduction

The next generation power device, SiC MOSFET, is a promising candidate for many applications, because the SiC material properties are superior to a conventional Silicon (Si) material [1–6]. SiC MOSFET has faster switching speeds (shorter switching time), higher switching frequencies, higher voltage blocking capabilities and higher temperature performance. The converter based SiC MOSFET in trains and electric vehicles [7,8], battery chargers for electric vehicles [9], renewable energy [10,11] and industrial automation [12] have excellent performance, such as higher efficiency, higher power density and lighter weight, etc. However, due to the high speed of SiC MOSFET, parasitic parameters cannot be overlooked, although they are not considered in Si device applications [13–15].

Crosstalk issues matter in the reliability of electronic equipment. Independent of SiC or Si device applications, crosstalk issues exist in a phase-leg configuration. However, the high switching speed of SiC MOSFET makes crosstalk issues more acute. Crosstalk issues are the spurious pulses induced on the gate-source voltage of the OFF-state switch during the active switch turn-ON or turn-OFF transition [16–21]. If the positive spurious pulse exceeds threshold voltage V_{th} of the OFF-state switch, this switch can be partially turned ON; if the negative spurious pulse exceeds the maximum allowable negative driver voltage $V_{GS\_MAX(-)}$ of the OFF-state switch, gate overstresses of this switch can occur, which damage the device and may impose serious reliability problems [22,23]. Thus, it is necessary to investigate in more detail the mechanisms of crosstalk issues of SiC MOSFET.

For solutions suppressing the crosstalk issue, several have been done. First, decreasing the switching speed of the active switch is an easy solution. However, the efficiency and the density may be affected. Second, setting an appropriate negative driver voltage to avoid the spurious pulse exceeding the safety value is a common solution [23]. However, the safety allowance ($V_{th} - V_{GS\_MAX(-)}$) of SiC MOSFET is small, so selecting a suitable negative driver voltage is difficult. The most studied solution is to add an assistant circuit to the conventional driver, which is recommended by several SiC power device

manufacturers [21,24,25]. In [26], the added assistant circuit can change the negative driver voltage of the OFF-state switch, which makes the spurious pulse within the safety allowance. However, it may occur that the spurious pulse is so high that shifting the negative driver voltage cannot guarantee that the spurious pulse is within the safety allowance. In [25,27], shifting negative driver voltage and clamping the gate-source voltage to negative driver voltage are realized together, but the implementation of the assistant circuit is complex and needs MOSFETs and control circuits. The authors in [28] propose a capacitor paralleling with the gate-source terminal to bypass a proportion of displacement current of the gate-drain capacitor C_{GD}. However, the performance of SiC MOSFET will be reduced. In [29], a bipolar junction transistor (BJT) and a capacitor are paralleling with the gate-source terminal to avoid affecting the switching speed of SiC MOSFET. However, this assistant circuit can only suppress the negative spurious pulse. In [30], the BJT is replaced by a MOSFET, but this MOSFET needs an accurate control signal and the control circuit. In [31], only two capacitors are added. One capacitor is in parallel with the turn-OFF gate resistor, another capacitor connects the terminal of the negative driver voltage and the common source inductors, and one switch which connects the turn-OFF gate resistor in the driver chip is reused to replace BJT in [29] or MOSFET in [30]. This assistant circuit is simple and has no transistors. However, the driver chip must use split output which separates the turn-ON gate resistor and the turn-OFF gate resistor [32], because the reusable switch guarantees that the added capacitor does not affect the performance of SiC MOSFET during the tun-ON transition. In [33–35], some manufacturers also use the active miller clamping in the driver chip. The operating principle is to sense the gate-source voltage of the OFF-state switch and to compare it with the clamping threshold (typically, 2 V) in the chip. Thus, the crosstalk issue is identified by the measured gate-source voltage. However, due to the parasitic gate inductor, the common source inductor and the inner gate resistor, the measured gate-source voltage is inaccurate and always smaller than the actual value. Moreover, the threshold voltage of SiC MOSFET is low and the switching speed is fast, so it is very possible that the positive spurious pulse exceeds the threshold voltage before the clamping transistor turns ON. These kinds of driver chips with the active miller clamping can only detect the positive spurious pulse; the negative spurious pulse is also needed suppression for limiting it smaller than the maximum negative driver voltage ($V_{GS\_MAX(-)}$) of SiC MOSFET.

Therefore, this paper focuses on a suppressing solution for the crosstalk issue of SiC MOSFET. First, the crosstalk mechanisms of SiC MOSFET are analyzed in this paper. The voltage drops across the common-source inductors and the displacement current of the gate-drain capacitor of the OFF-state switch cause the crosstalk issue. Second, a new gate driver for suppressing crosstalk issue is proposed, which adds two BJTs and one diode to the gate terminal of SiC MOSFET and the negative driver voltage. This assistant circuit provides a low impedance path to bypass the displacement current of the gate-drain capacitor. The operating principle and simulation results of the proposed driver are presented in the paper. The prior drivers and the proposed driver are compared based on the simulation results. Finally, the proposed gate driver is successfully implemented and effectively verified on a 1.1 kW synchronous buck prototype.

2. Crosstalk Mechanisms of SiC MOSFET

In a phase-leg configuration, such as synchronous boost, synchronous buck, half bridge and full bridge, a crosstalk issue is likely to occur on the OFF-state switch. Figure 1 shows a synchronous buck converter. In this figure, Q_1 is the upper switch and Q_2 is the lower switch. Crosstalk issue occurs on the gate-source voltage of Q_2 during Q_1 switching transitions.

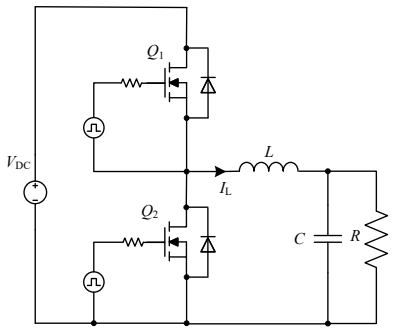


Figure 1. Synchronous buck converter.

In Figure 2, the parasitic parameters existing on the device and loop are considered, which cannot be overlooked in SiC device applications due to their high-speed switching. The junction capacitors of Q_1 and Q_2 are the gate-source capacitor C_{gs1} and C_{gs2}, the gate-drain capacitor C_{gd1} and C_{gd2}, and the drain-source capacitor C_{ds1} and C_{ds2}. The parasitic inductors in the package of Q_1 and Q_2 are the gate inductor L_{g1_in} and L_{g2_in}, the drain inductor L_{d1_in} and L_{d2_in}, the source inductor L_{s1_in} and L_{s2_in}. The internal gate drive resistors of Q_1 and Q_2 are R_{g1_in} and R_{g2_in}. L_{g1_ex}, L_{d1_ex}, L_{s1_ex}, L_{g2_ex}, L_{d2_ex}, and L_{s2_ex} represent the parasitic inductors of the package leads. L_{g1_loop}, L_{g2_loop}, L_{loop1}, and L_{loop2} represent the interconnection parasitic inductors of PCB traces. In addition, L_{s1_in}, L_{s1_ex}, L_{s2_in} and L_{s2_ex} are the common source inductors [31]. R_{g1_ex} and R_{g2_ex} are external gate resistor. v_{pulse1} and v_{pulse2} are gate signals, the voltages of which are from V_{G1} to V_{G2}, and V_{G2} is negative. The input voltage source V_{DC} and the current I_L are assumed constant because crosstalk issue occurs during the switching transition. Figure 3 shows the switching waveforms of Q_1 and Q_2 during Q_1 turn-ON and turn-OFF transition.

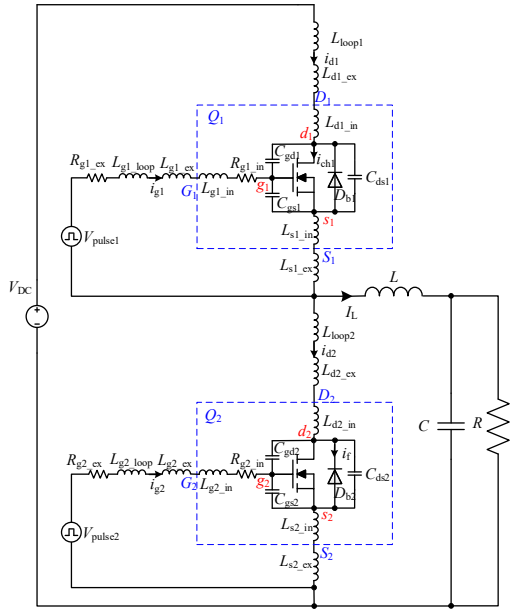


Figure 2. Synchronous buck considering the parasitic parameters.

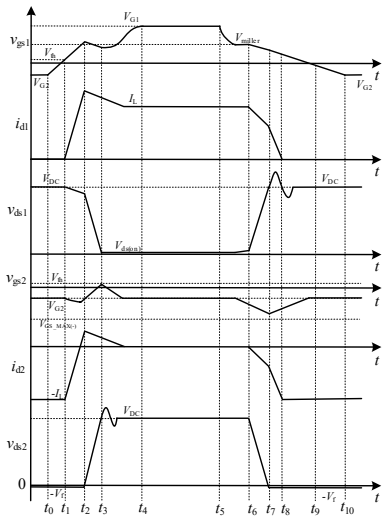


Figure 3. Theoretical waveforms during Q_1 turn-ON and turn-OFF transition.

2.1. Crosstalk Issue during Q_1 Turn-ON Transition

v_{gs1} is the gate-source voltage of Q_1, i_{d1} is the drain current of Q_1. v_{ds1} is the drain-source voltage of Q_1. v_{gs2} is the gate-source voltage of Q_2, i_{d2} is the drain current of Q_2. v_{ds2} is the drain-source voltage of Q_2. Before Q_1 is turned ON, the current I_L flows through D_2, Q_1 and Q_2 are OFF-state.

Stage 1 [t_0~t_1], at t_0, Q_1 is turned ON. Since the gate-source voltage v_{gs1} does not reach the threshold voltage V_{th}, the channel of Q_1 is OFF and the crosstalk issue does not occur in this stage.

Stage 2 [t_1~t_2], when the gate-source voltage v_{gs1} reaches the threshold voltage V_{th}, the current I_L commutates from D_2 to Q_1. This stage ends when D_2 begins to block the voltage. The equivalent circuit of this stage is shown in Figure 4a. Figure 4a neglects the gate inductors due to their less obvious effects on crosstalk issue. The spurious pulse on the gate-source voltage of Q_2 during this stage is given by Equation (1). The falling drain current i_{d2} brings the voltage drops across the common source inductors L_{s2_in} and L_{s2_ex}, which results in charging the gate-source capacitor C_{gs2}.

$$\Delta v_{gs2} = V_1\left(1 - e^{\frac{-t}{\tau}}\right) \tag{1}$$

where $\tau = (R_{g2\_in} + R_{g2\_ex})C_{gs2}$, and $V_1 = -(L_{s2\_in} + L_{s2\_ex})\mathrm{d}i_{d2}/\mathrm{d}t$. V_1 decides the change trend of the gate-source voltage v_{gs2} during this stage.

At Stage 3 [t_2~t_3], when D_2 is able to block the voltage, the drain-source voltage v_{ds2} of Q_2 increases. The drain current i_{d2} charges the gate-drain capacitor C_{gd2} and the drain-source capacitor C_{ds2}. This stage ends when the drain-source voltage v_{ds1} decreases to the ON-state voltage of SiC MOSFET. The equivalent circuit of this stage is shown in Figure 4b. The spurious pulse on the gate-source voltage of Q_2 during this stage is given by Equation (2). The drain current i_{d2} still induces the voltage drops across the common source inductors L_{s2_in} and L_{s2_ex}. In addition, the displacement current of the gate-drain capacitor C_{gd2} also passes through the gate-source capacitor C_{gs2}.

$$\Delta v_{gs2} = V_2\left(1 - e^{\frac{-t}{\tau}}\right) \tag{2}$$

where $V_2 = (R_{g2\_in} + R_{g2\_ex})C_{gd2}\mathrm{d}v_{ds2}/\mathrm{d}t - (L_{s2\_in} + L_{s2\_ex})\mathrm{d}i_{d2}/\mathrm{d}t$. V_2 decides the change trend of the gate-source voltage v_{gs2} during this stage.

Stage 4 [t_3~t_4], during this stage, the drain-source voltage v_{ds2} and the drain current i_{d2} of Q_2 may have the ringing. Therefore, the ringing also exists on the gate voltage v_{gs2}.

After t_4, the circuit is steady after the Q_1 turn-ON transition.

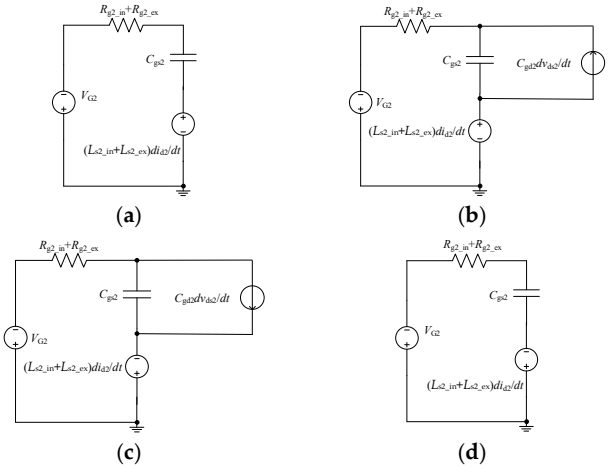


Figure 4. Equivalent circuit during Q_1 turn-ON and turn-OFF transition. (**a**) Stage 2, (**b**) Stage 3, (**c**) Stage 7 and (**d**) Stage 8.

2.2. Crosstalk Issue during Q_1 Turn-OFF Transition

Before Q_1 is turned OFF, the current I_L flows through Q_1, and Q_2 are OFF-state.

Stage 6 [t_5~t_6], at t_5, Q_1 is turned OFF. Since the gate-source voltage v_{gs1} does not reach the miller voltage V_{mil}, Q_1 is still in the ON-state and the crosstalk issue does not occur in this stage.

Stage 7 [t_6~t_7], when the gate-source voltage v_{gs1} reaches the miller voltage V_{mil}, the drain-source voltage v_{ds1} of Q_1 increases and the drain-source voltage v_{ds2} of Q_2 declines. When the drain-source voltage v_{ds2} reaches to the forward voltage of D_2, this stage ends. The equivalent circuit of this stage is shown in Figure 4c. The spurious pulse on the gate-source voltage of Q_2 during this stage can be also expressed as Equation (2). The drain current i_{d2} discharges the gate-drain capacitor C_{gd2} and the drain-source capacitor C_{ds2}. Therefore, the voltage drops across the common source inductors L_{s2_in} and L_{s2_ex} and the displacement current of the gate-drain capacitor C_{gd2} induce the crosstalk issue of Q_2 in this stage.

At Stage 8 [t_7~t_8], when D_2 is on state, the current I_L commutates from Q_1 to D_2. This stage ends when the channel of Q_1 is OFF. The equivalent circuit of this stage is shown in Figure 4d. The spurious pulse on the gate-source voltage of Q_2 during this stage can be also expressed as Equation (1). The falling drain current i_{d2} brings the voltage drops across the common source inductors L_{s2_in} and L_{s2_ex}, which makes the gate voltage change v_{gs2} of Q_2 fluctuate.

At Stage 9 [t_8~t_9], the drain-source voltage v_{ds2} and the drain current i_{d2} of Q_2 may have ringing. Therefore, the ringing also exists on the gate voltage v_{gs2}.

After t_9, the circuit is steady after Q_1 turn-OFF transition.

Based on the previous discussions, the voltage drops across the common-source inductors and the displacement current of the gate-drain capacitor cause the crosstalk issue of SiC MOSFET.

3. A New Gate Driver for Suppressing Crosstalk Issue of SiC MOSFET

The common source inductors L_{s2_in} and L_{s2_ex} are the parasitic inductors of the bonding wires and leads of the package. The common source inductor L_{s2_in} is immutable. Nevertheless, the common source inductor L_{s2_ex} can be decoupled from the driver loop by adding a capacitor to the negative driver voltage and node S1 (or node S2) in Figure 2, like in [31]. In addition, the common source inductor L_{s2_ex} can also be reduced by shortening the length of package leads connected into circuit. In this paper, the solution of making the driver board connect to the nodes G1 and S1 (or nodes G2 and S2) in Figure 2 is adopted, like in [36]. This solution makes the leads connected into driver loop much less.

The effects of common source inductors on the crosstalk issue are reduced. A new gate driver is proposed to bypass the injected current into the gate-source capacitor from the gate-drain capacitor. The proposed driver is shown as Driver_Q_1 or Driver_Q_2 in Figure 5. Driver_Q_1 is composed of the power supply V_{1H} and V_{2H}, two switches S_{1H} and S_{2H}, the gate resistor R_H, two BJTs T_{1H} and T_{2H}, diode D_H and resistor R_1 and R_2. Driver_Q_2 is composed of the power supply V_{1L} and V_{2L}, two switches S_{1L} and S_{2L}, the gate resistor R_L, two BJTs T_{1L} and T_{2L}, diode D_L and resistors R_3 and R_4.

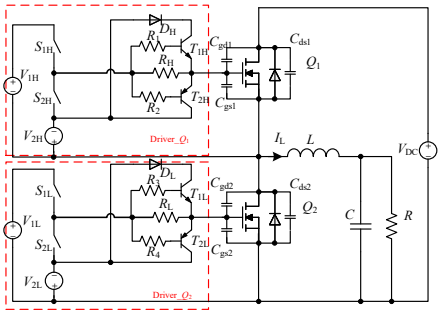


Figure 5. Proposed driver for suppressing the crosstalk issue.

3.1. Operating Principle

Figure 6 shows the logic signals of switches S_{1H}, S_{2H}, S_{1L} and S_{2L}. The proposed driver has four operating modes. Before t_0, Switches S_{2H} and S_{2L} are ON-state, switches S_{1H} and S_{1L} are OFF-state, T_{1H}, T_{2H}, T_{1L} and T_{2L} are OFF-state. Q_1 and Q_2 are OFF-state, and the current I_L flows through D_2.

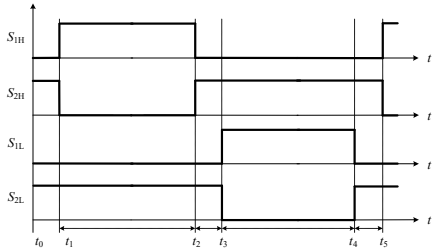


Figure 6. Logic signals of S_{1H}, S_{2H}, S_{1L} and S_{2L} in the proposed driver.

Mode 1 [t_1~t_2]: S_{1H} is turned ON, S_{2H} is turned OFF. S_{1L} is still OFF-state and S_{2L} is still ON-state. Q_1 is turned ON and Q_2 remains OFF-state. The current I_L commutates from D_2 to Q_1. The displacement current of the gate-drain capacitor C_{gd2} of Q_2 flows through the gate resistor R_L and the gate-source capacitor C_{gs2}. Then, the voltage drop on the gate resistor R_L turns ON the BJT T_{2L}, which clamps the gate-source voltage v_{gs2} as the negative driver voltage V_{2L}. When the displacement current of the gate-drain capacitor C_{gd2} is zero, the BJT T_{2L} is turned OFF. The impedance of the BJT T_{2L} is small, most of the displacement current of the gate-drain capacitor C_{gd2} is bypassed. Therefore, the effect of the displacement current of the gate-drain capacitor C_{gd2} on the crosstalk issue of Q_2 is suppressed during Q_1 turn-ON transition.

Mode 2 [t_2~t_3]: S_{1H} is turned OFF, S_{2H} is turned ON. S_{1L} is still OFF-state and S_{2L} is still ON-state. Q_1 is turned OFF and Q_2 remain OFF-state. The current I_L commutates from Q_1 to D_2. The displacement current of the gate-drain capacitor C_{gd2} flows through gate resistor R_L and gate-source capacitor C_{gs2}. The voltage drop on the gate resistor R_L turns ON the BJT T_{1L} and diode D_L is ON-state, which clamps the gate-source voltage v_{gs2} as the negative driver voltage V_{2L}. When the displacement current of the gate-drain capacitor C_{gd2} is zero, the BJT T_{1L} is turned OFF as same with Mode 1. Most of the displacement current of the gate-drain capacitor C_{gd2} is also bypassed by T_{1L} and D_L. Therefore, the effect of the

displacement current of the gate-drain capacitor C_{gd2} on the crosstalk issue of Q_2 is also suppressed during Q_1 turn-OFF transition.

Mode 3 [t_3~t_4]: S_{1L} is turned ON, and S_{2L} is turned OFF. S_{1H} remains OFF-state, and S_{2H} remains ON-state. During this mode, Q_2 is turned ON, and Q_1 remains OFF-state. The current I_L commutates from D_2 to Q_2, so the drain-source voltage v_{ds2} and the drain current i_{d2} scarcely change and no crosstalk issues occur for Q_2.

Mode 4 [t_4~t_5]: S_{1L} is turned OFF, and S_{2L} is turned ON. S_{1H} remains OFF-state, and S_{2H} remains ON-state. During this mode, Q_2 is turned OFF, and Q_1 remains OFF-state. The discharging current of the gate-source capacitor C_{gs2} of Q_2 flows through the gate resistor R_L. The voltage drop on the gate resistor R_L turns ON the BJT T_{2L}. When the discharging current of the gate-source capacitor C_{gs2} is zero, T_{2L} is turned OFF. The current I_L commutates from Q_2 to D_2, so the drain-source voltage v_{ds2} and the drain current i_{d2} also scarcely change and no crosstalk issue occurs for Q_2.

3.2. Simulation Results

In order to verify the operating principle of the proposed driver, the simulation model of the proposed driver based on the synchronous buck is made in LTspice. In the simulation model, the spice model of C2M0080120D by Cree Inc. is used, the parameters of which are shown in Table 1. The parameters in the simulation model are presented in Table 2. Considering that the gate voltage oscillation should be avoided, the gate resistor needs to meet the limitation condition [37] shown in Equation (3). Calculated based on Tables 1 and 2, the gate resistor selected 10 Ω.

$$R_{g\_in} + R_{g\_ex} \geq 2\sqrt{\frac{L_{g\_in} + L_{g\_ex} + L_{g\_loop} + L_{s\_in} + L_{s\_ex}}{C_{gs}}} \quad (3)$$

Table 1. Parameters of C2M0080120D.

Parameter	Value	Parameter	Value
Inner gate resistor (R_{g_in})	3.9 Ω	Threshold voltage (V_{th})	2.9 V
Gate inductors (L_{g_in} + L_{g_ex})	15 nH	Gate-source capacitor (C_{gs})	1122 pF
Common source inductors (L_{s_in} + L_{s_ex})	9 nH	Gate-drain capacitor (C_{gd})	8 pF
Drain inductors (L_{d_in} + L_{d_ex})	6 nH	Drain-source capacitor (C_{ds})	92 pF
Maximum negative driver voltage ($V_{GS\_MAX(-)}$)	−10 V		

Table 2. Parameters of the simulation model based on synchronous buck and proposed driver.

Parameter	Value	Parameter	Value
Input voltage	400 V	Power loop inductor	25 nH
Output current	21 A	Power loop inductor	25 nH
Switching frequency	500 kHz	Positive driver voltage (V_{1H} and V_{1L})	18 V
Width of the gate signal	500 ns	Negative driver voltage (V_{2H} and V_{2L})	−5 V
Dead time	500 ns	Gate resistor (R_H and R_L)	10 Ω
Gate loop inductor	10 nH	Base resistor of BJT(R_1~R_4)	1 Ω

Figure 7 shows the waveforms of the simulation model, which include the gate-source voltage v_{gs2}, the drain-source voltage v_{ds2}, the drain current i_{d2}, the gate current i_{g2}, the R_L current i_{RL}, the T_{1L} current i_{T1L} and the T_{2L} current i_{T2L}. From Figure 7a, when the current passes through the gate, resistor R_L is positive, the voltage drop on R_L makes T_{1L} turn ON; when the current passes through the gate, resistor R_L is negative, the voltage drop on R_L makes T_{2L} turn ON. Therefore, the displacement current of the gate-drain capacitor C_{gd2} is shunted by the gate-source capacitor C_{gs2}, the gate resistor R_L, the BJTs T_{1L} and T_{2L}. Due to the impedance of T_{1L} and T_{2L} being lower, much of the displacement

current passes through T_{1L} and T_{2L}. From Figure 7b, it is the same with Figure 7a that T_{1L} is turned ON when the current passes through the gate, resistor R_L is positive and T_{2L} is turned ON when the current passes through the gate, resistor R_L is negative. On basis of the simulation results, it is proved that the proposed driver is valid for suppressing the crosstalk issue.

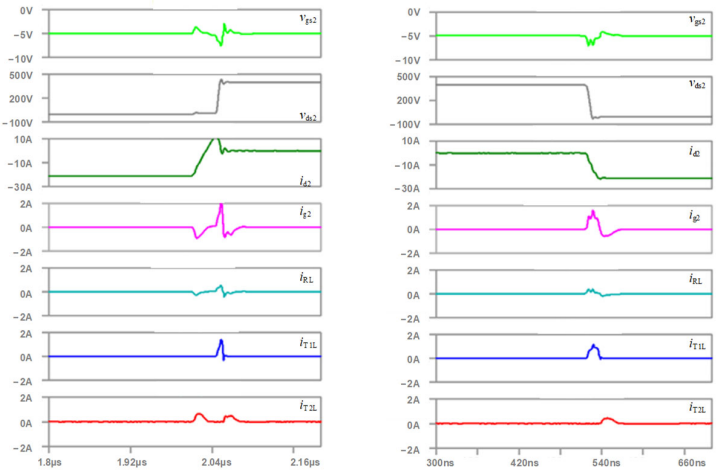


Figure 7. Simulation waveforms of the proposed driver. (**a**) during Q_1 turn-ON transition and (**b**) during Q_1 turn-OFF transition.

3.3. Comparisons

The comparisons between the prior drivers in [24–27,30,31] and the proposed driver are presented in this section. The driver in [24] is the conventional driver, which is a simple and generally-used SiC device application. Drivers in [25–27,30,31] add assistant circuits to the conventional driver in [18]. The simulation waveforms of Q_2 based on the prior drivers in [24–27,30,31] and the proposed driver are shown in Figure 8, which is obtained under the same switching performance of Q_1. The parameters of the prior drivers in [24–27,30,31] and the proposed driver are shown in Table 3. In addition, the suppression method, assistant components, implementation and suppression effectiveness of the prior drivers and the proposed driver are compared in Table 4. Drivers in [25–27] shift the driver voltage to make a spurious pulse in the safety allowance. Drivers, except in [19], provide a low impedance path for the displacement current of the gate-drain capacitor. From simulation results, it is observed that drivers with the low impedance path have lower spikes of the spurious pulse than the conventional driver in [24] and the driver in [26]. The driver in [25] has the lowest spikes of the spurious pulse on the gate voltage but the assistant circuit is complex. The driver in [31] has the simplest circuit structure because of no added transistor. However, the driver chip in [31] needs split output because the switch S_{2L} is reusable to connect the turn-OFF gate resistor and the capacitor C_{a1}, which guarantees no effect on the turn-ON performance of SiC MOSFET. Comparing drivers in [25–27,30], which do not need to use the driver chip with split output, the proposed driver is easier to implement owing to no MOSFET and no driver circuit. Therefore, considering the suppression effectiveness and the implementation, the proposed driver is a good choice.

Table 3. Parameters of prior drivers in [24–27,30,31] and the proposed driver.

	Parameter
Driver in [24]	V_{1L} = 18 V, V_{2L} = 5 V, R_L = 10 Ω
Driver in [25]	V_{1L} = 23 V, V_{2L} = 5 V, R_L = 10 Ω
Driver in [26]	V_{1L} = 18 V, V_Z = 4.7 V, R_{L_ON} = 10 Ω, R_{L_OFF} = 10 Ω, R_C = 1 Ω, R_M = 0.1 Ω, C_Z = 100 nF
Driver in [27]	V_{1L} = 18 V, V_{2L} = 5 V, R_L = 10 Ω
Driver in [30]	V_{1L} = 18 V, V_{2L} = 5 V, R_L = 10 Ω, C_a = 5 nF
Driver in [31]	V_{1L} = 18 V, V_{2L} = 5 V, R_{L_ON} = 10 Ω, R_{L_OFF} = 10 Ω, C_{a1} = 5 nF
Proposed driver	V_{1L} = 18 V, V_{2L} = 5 V, R_L = 10 Ω

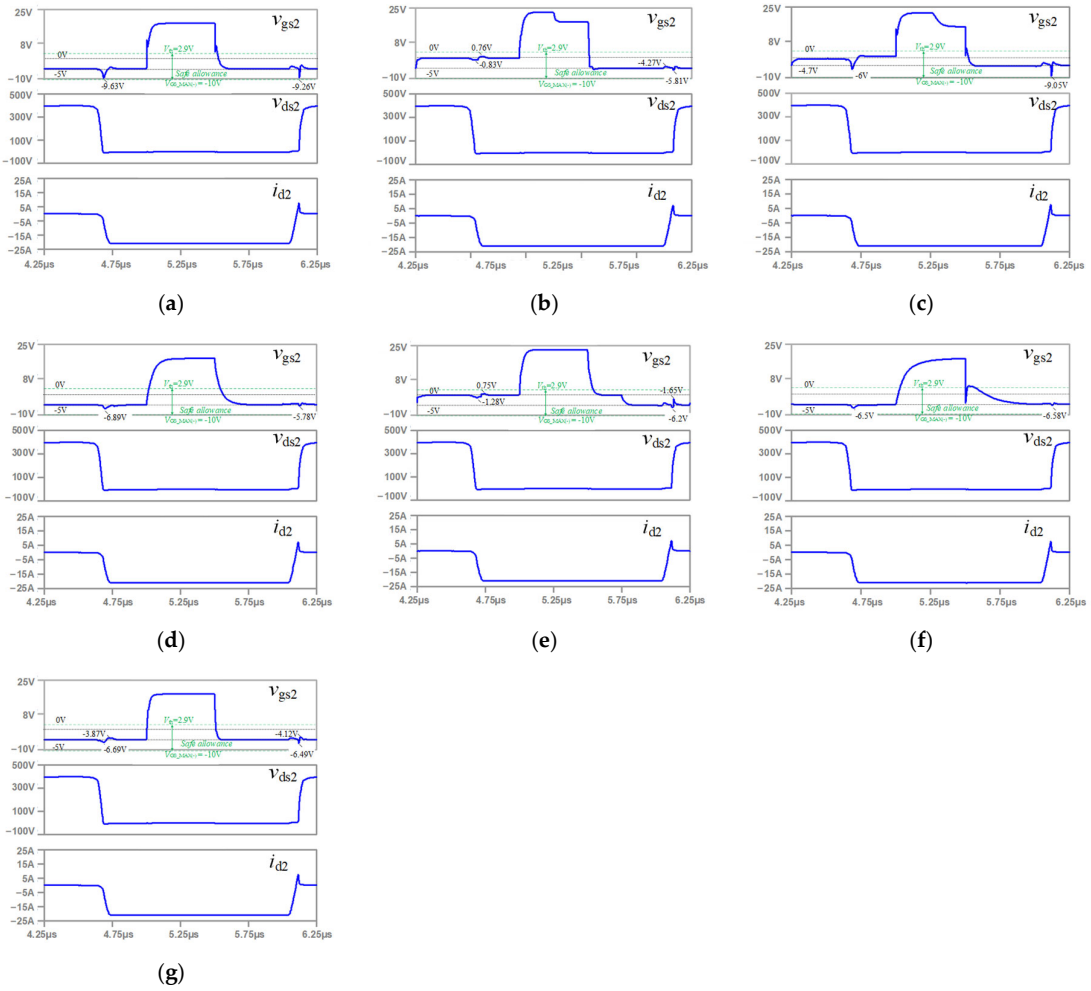


Figure 8. Simulation results of the prior drivers in [24–27,30,31] and the proposed driver. (**a**) the conventional driver in [24], (**b**) driver in [25], (**c**) driver in [26], (**d**) driver in [27], (**e**) driver in [30], (**f**) driver in [31] and (**g**) the proposed driver.

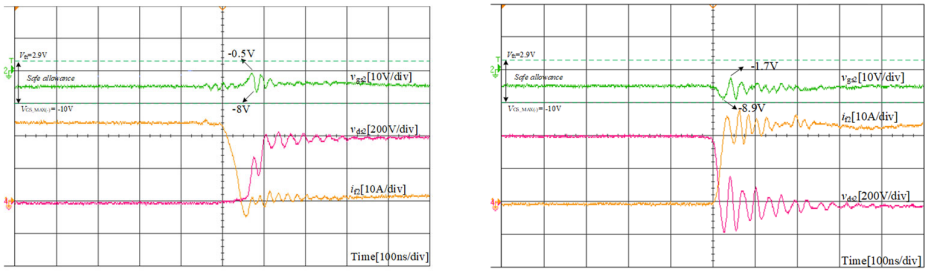
Table 4. Comparisons between the prior drivers in [25–27,30,31] and proposed driver.

	Suppression Method	Assistant Components	Implementation	Suppression Effectiveness
Driver in [25]	Shift driver voltage and provide a low impedance path	One diode, two MOSFETs and drivers for MOSFETs	hard	Good
Driver in [26]	Shift driver voltage	One resistor, one MOSFET and driver for MOSFET	Medium	Bad
Driver in [27]	Shift driver voltage and provide a low impedance path	Two diodes, two switches (if MOSFETs, drivers are needed)	hard	Medium
Driver in [30]	provide a low impedance path	One capacitor, one MOSFET and driver for MOSFET	Medium	Good
Driver in [31]	provide a low impedance path	Two capacitors	Easy	Good
Proposed driver	provide a low impedance path	Two BJTs and one diode	Easy	Good

4. Verification

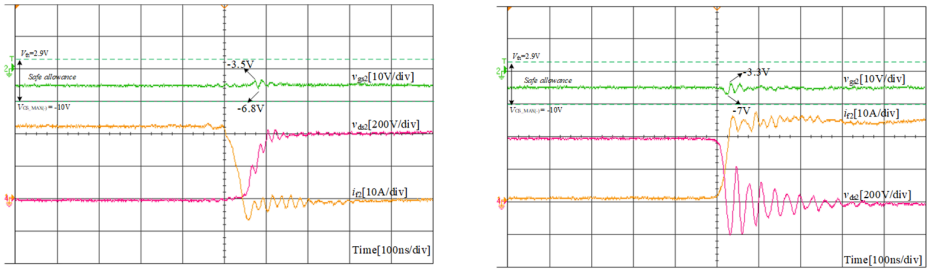
Comparison experiments are implemented between the conventional driver and the proposed driver to verify the proposed driver. C2M0080120D by Cree Inc. is tested in this paper and the related parameters of C2M0080120D are shown in Table 1. The Parameters of synchronous buck and driver are the same with the simulation model shown in Table 2. The driver PCB boards must be mounted as close as the plastic package of SiC MOSFET, and the leads connected into the driver loop are shortest which reduces the common source inductors.

Figure 9 presents the switching waveforms with the conventional driver. Figure 10 presents the switching waveforms with the proposed driver. The conventional driver is realized by removing the assistant circuit in the proposed driver. The forward current i_{f2} of D_2, the drain-source voltage v_{ds2} of Q_2 and the gate-source voltage v_{gs2} of Q_2 are tested. From Figure 9, the spikes of the spurious pulse on the gate-source voltage of Q_2 with conventional drivers are tested as −0.5 V and −8 V during Q_1 turn-ON transition, and −1.7 V and −8.9 V during Q_1 turn-OFF transition, respectively. From Figure 10, the spikes of the spurious pulse on the gate-source voltage of Q_2 with the proposed driver are tested as −3.5 Vand−6.8 V during Q_1 turn-ON transition, and −3.3 V and −7 V during Q_1 turn-OFF transition, respectively. Comparing Figures 9 and 10, the spikes of the spurious pulse on the gate-source voltage of Q_2 are obviously decreased by using the proposed driver.



(**a**) (**b**)

Figure 9. Experimental results with the conventional driver. (**a**) during Q_1 turn−ON transition, and (**b**) during Q_1 turn-OFF transition.



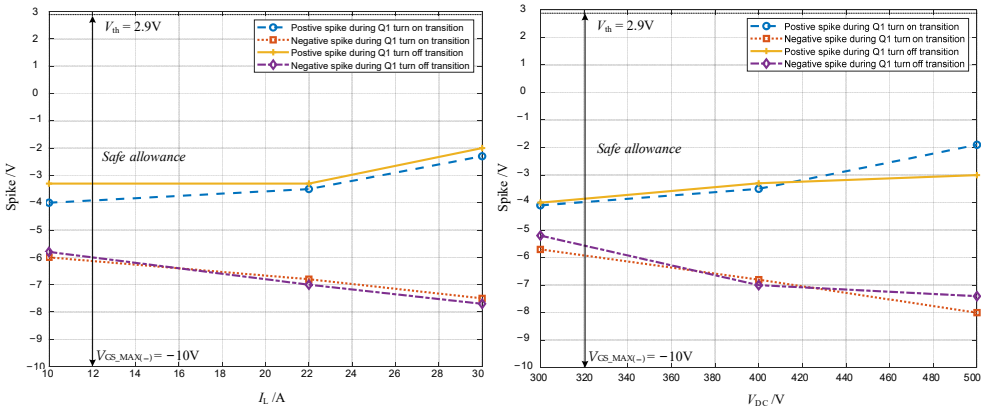
(**a**) (**b**)

Figure 10. Experimental results with the proposed driver. (**a**) during Q_1 turn-ON transition, and (**b**) during Q_1 turn-OFF transition.

Figure 11a,b show the spikes of the spurious pulses under different currents I_L and different voltages V_{DC}. As shown in Figure 11, the higher operating current or voltage makes the crosstalk issue more severe. However, it is observed that the proposed driver is effective to suppress crosstalk issues and guarantees the spikes of the spurious pulses within safe allowance. Figure 12 presents the efficiency of 1.1 kW synchronous buck with the conventional driver or the proposed driver. The tested conditions of synchronous buck are presented in Table 5 and the efficiency is tested under open-loop control. From Figure 12, it is observed that the efficiency of synchronous buck converter is higher than with the proposed driver, and the maximum efficiency is 96.7%.

Table 5. Efficiency tested conditions of synchronous buck.

Parameter	Value	Parameter	Value
Input voltage	400 V	Dead time	500 ns
Output voltage	100 V	Output inductor	100 μH
Output power	700~1100 W	Output capacitor	220 μF
Switching frequency	50 kHz		



(**a**) (**b**)

Figure 11. Spikes of spurious pulses at different working conditions, (**a**) I_L and (**b**) V_{DC}.

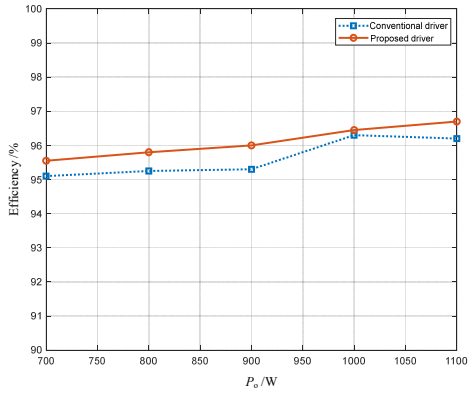


Figure 12. Efficiency of synchronous buck with the conventional driver and the proposed driver.

5. Conclusions

Crosstalk issues impact the reliability of SiC MOSFET applications. The crosstalk mechanisms of SiC MOSFET are analyzed in this paper, which can be divided into two perspectives: the voltage drops across the common-source inductors and the displacement current of the gate–drain capacitor. A new gate driver for suppressing crosstalk issues is proposed in this paper. Two BJTs and one diode are used to connect the gate terminal of SiC MOSFET and the negative driver voltage, which provides a low impedance path to bypass the displacement current of the gate-drain capacitor. The operating principle and simulation results show the proposed driver is valid on suppressing crosstalk. In addition, the comparisons between the prior drivers and the proposed driver show the proposed driver is a good choice when trading off the suppression effectiveness and circuit complexity. The experiments also prove the proposed driver is effective on suppressing crosstalk issues. In addition, the efficiency of 1.1 kW synchronous buck with the proposed driver is higher than with the conventional driver, which can reach 96.7%.

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