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The Effects of Total Ionizing Dose on the SEU Cross-Section of SOI SRAMs

Peixiong Zhao [1,*], Bo Li [2], Hainan Liu [2], Jinhu Yang [1,3], Yang Jiao [1,3], Qiyu Chen [1,3], Youmei Sun [1] and Jie Liu [1,*]

[1] Institute of Modern Physics, Chinese Academy of Sciences, Lanzhou 730000, China
[2] Institute of Microelectronics, Chinese Academy of Sciences, Beijing 100029, China
[3] School of Nuclear Science and Technology, University of Chinese Academy of Sciences, Beijing 100049, China
* Correspondence: zhaopeixiong@impcas.ac.cn (P.Z.); j.liu@impcas.ac.cn (J.L.)

Abstract: The total ionizing dose (TID) effects on single-event upset (SEU) hardness are investigated for two silicon-on-insulator (SOI) static random access memories (SRAMs) with different layout structures in this paper. The contrary changing trends of TID on SEU sensitivity for 6T and 7T SOI SRAMs are observed in our experiment. After 800 krad(Si) irradiation, the SEU cross-sections of 6T SRAMs increases by 15%, while 7T SRAMs decreases by 60%. Experimental results show that the SEU cross-sections are not only affected by TID irradiation, but also strongly correlate with the layout structure of the memory cells. Theoretical analysis shows that the decrease of SEU cross-section of 7T SRAM is caused by a raised OFF-state equivalent resistance of the delay transistor N5 after TID exposure, which is because the radiation-induced charges are trapped in the shallow trench, and isolation oxide (STI) and buried oxide (BOX) enhance the carrier scattering rate of delay transistor N5.

Keywords: single event upset (SEU); total ionizing dose (TID); silicon-on-insulator (SOI); synergistic effect; radiation-hardened by design (RHBD)

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1. Introduction

In the space environment, there are many high-energy radiation particles, such as electrons, protons, heavy ions, and so on [1,2]. These high-energy radiation particles will cause the macroscopic electrical properties of devices to change, degrade, or even fail. The single-event effect (SEE) and effect of total ionizing dose (TID) are the main causes of the failure of spacecrafts and satellites [3–11]. The radiation hardening technology of integrated circuits mainly include radiation-hardened by design (RHBD) storage cells (heavy ion tolerant cell, dual interlocked storage cell, etc.) [12–14] and radiation-hardened-by-process (RHBP) front-end-of-line (guard-band, silicon-on-insulation, etc.) [15–17]. The silicon-on-insulation (SOI) process, realized physically, isolates the channel region from the substrate region, which not only significantly reduces the effective collection region, but also eliminates the single event latch-up (SEL) [18,19] and tunneling [20] effects commonly found in bulk silicon devices. Therefore, the SOI process is naturally resistant to irradiation [21–23] and has important applications in the field of radiation-hardened integrated circuits (ICs).

The SEE, TID effect, and synergy between the TID and SEE in electronic devices have been extensively studied. The effect of ion parameters on the multi-bit upset effect in 45 and 28 nm SOI static random access memories (SRAMs) has been investigated by Raine et al., in which the 4-bit upsets phenomenon was observed under oblique incidence conditions [24], and the multi-bit upsets phenomenon caused by the non-charge sharing effect was observed under positive incidence conditions [25]. Moreover, Liu et al. have carried out proton and heavy ion irradiation experiments on radiation-hardened SOI SRAMs. The results showed that single-event upset (SEU) can be triggered only when secondary ions hit both the delay transistor and OFF-state NMOS transistor [26]. Schwank et al. have irradiated many kinds of SRAM devices with various radiation sources, such as γ, X-ray, and proton, and then measured the SEU cross-section of the devices. The experimental results showed

that the TID irradiation has a significant effect on the SEU cross-section of the device, and the SEU cross-section increases with increasing irradiation dose. Meanwhile, the SEU cross-section had a certain dependence on parameters such as test data patterns, irradiation test temperature, etc. [27–32].

Previous studies have shown that TID significantly affects the SEU cross-section of the electron device, and numerous studies have been conducted on the irradiation doses, data patterns, and experimental temperature. However, the effect of the layout structure on the SEU cross-section after TID irradiation has had relatively few studies, and the physical mechanism is not yet fully understood. Therefore, in this paper, we design two SOI SRAM devices with different layout structures and investigate the mechanism of the effect of the layout structure on SEU cross-section of SOI SRAMs. This paper is organized as follows. In Section 2, the test circuits and experimental methods are presented. The experimental results for TID effects on SEU hardness of SOI SRAMs with 6T and 7T cell designs are described in Section 3. In Section 4, the experimental results are discussed. In Section 5, conclusions are drawn.

2. Test Circuit and Experimental Setup

2.1. Test Circuit

We design two SOI SRAMs with different layout structures, based on the 130 nm SOI CMOS process. The memory capacity is 64 kbit and organized by 8 k × 8 bits. Device operates using a dual power supply for the input–output (I/O) circuitry (higher voltage) and memory array (lower voltage). The nominal supply voltages (Vdd) are 1.5 and 3.3 V for the core blocks and I/O, respectively. Figure 1a shows a schematic diagram of the layout structure and size of the 6T SRAM cell with dimensions 3.7 × 3.2 µm. The access transistors N3 and N4 share drain electrodes with the pull-down transistors N1 and N2, respectively. Figure 1b shows the layout structure and size of the 7T SRAM memory cell after hardened design by the delay transistor N5. The cell size of the 7T SRAM is 3.9 × 3.4 µm. The gate electrode of the delay transistor N5 is connected to the gate electrode of the access transistors N3 and N4. During the read/write operation, the delay transistor N5 will be in the ON-state, which has a very low resistance. While the delay transistor N5 will be in the OFF-state when the data hold state is entered, and the resistance of OFF-state N5 is very high, which can effectively suppress the single-event transient disturbance and significantly improve the stability of the 7T memory cell. As shown in Figure 1c, the structures of N1, N2, N3, N4, P1, and P2 were designed via body under source FET (BUSFET) [33]. Figure 1d shows a schematic diagram of the device structure of the delay transistor N5, which is equivalent to a resistor and transistor in parallel.

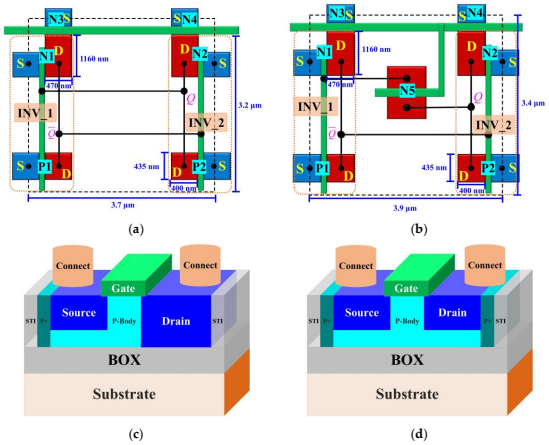


Figure 1. Schematics of memory cell structure of (**a**) 6T SRAM, (**b**) 7T SRAM, (**c**) BUSFET (body under source FET) structure of N1, N2, N3, N4, P1, P2, and (**d**) delay transistor N5 structure.

2.2. TID Experiment

As shown in Figure 2, TID exposures were carried out with 60 Co-γ ray at The Xinjiang Technical Institute of Physics and Chemistry, Chinese Academy of Sciences, with dose rate of 200 rad(Si)/s. A data pattern of 55 h was written into SRAM before irradiation, and it was then set to data hold operation during irradiation. Different devices from the same wafer were chosen for two times of SEU tests. For Kr ion, we chose nine devices and divided them into three groups, with one group irradiated to 200 krad(Si), another group irradiated to 400 krad(Si), and the last group being the reference sample without TID irradiation. Additionally, six devices were divided into two groups for Bi ion SEU test: 800 krad(Si) and reference sample without TID irradiation.

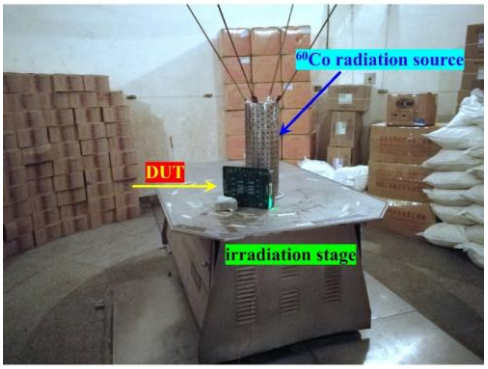


Figure 2. DUT in the terminal of the ^{60}Co irradiation.

2.3. Heavy Ion Irradiation

As shown in Figure 3, the heavy ion irradiation experiments were performed at the heavy ion research facility in Lanzhou (HIRFL) in the Institute of Modern Physics, Chinese Academy of Sciences. The ion species, energy, LET, and range are shown in Table 1. The LET values calculated by SRIM2013 [34] varied from 20.5 to 99.8 MeV·cm^2/mg. In the following experiments, the LET values were at the device surface. The ion ranges in silicon were always greater than 50 μm. Three levels of metal were applied to the SOI SRAM studied in this paper, and the thickness of the overlayer was measured at 7.2 μm. The range of Kr and Bi ion was enough to punch through the silicon film of our 130-nm SOI SRAM because the thickness of silicon film was only 260 nm. The SEU cross-sections of SRAMs were characterized in a dynamic mode, i.e., the SRAMs were written with a specific pattern to the memory array, and the read repeatedly and errors were counted until 200 errors were recorded. To evaluate the effect of the data pattern applied during TID exposure on SEU hardness, the SEU characterizations were performed with TID data pattern 55h and its complement data pattern AAh.

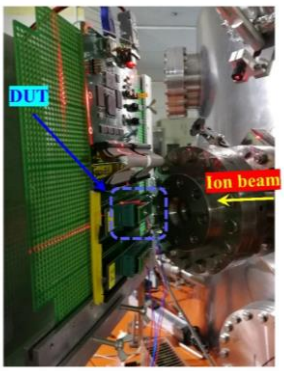


Figure 3. DUT in the terminal of the heavy-ion beamline.

Table 1. Ion spices, energy, LET, and range in silicon.

Ion Species	Air/Al-Foil (mm)/(μm)	Energy at Device Surface (MeV)	LET at Device Surface (MeV·cm^2/mg)	Ion Range (μm)
^{86}Kr	30/0	1841	20.5	274
	50/100	1154	27.2	150
	50/180	480	37.6	59
^{209}Bi	30/0	923	99.8	54

3. Experimental Results

3.1. Effect of TID on the 6T SRAM SEU cross-section

Figure 4 provides the results for the SEU cross-sections of 6T SRAM characterized by Kr ion of devices in three different groups: (1) fresh; (2) after deposition of 200 krad(Si); and (3) 400 krad(Si). The mean value of SEU data with an error bar at each dose level is depicted in Figure 4. As shown in Figure 4, SEU cross-section of 6T SRAM increased by a factor of 0.1% (20.5 MeV·cm^2/mg), 12.9% (27.2 MeV·cm^2/mg), and 5.2% (37.6 MeV·cm^2/mg) of after deposition of 200 krad(Si), with respect to the fresh condition, and increased by a factor of 3.7% (20.5 MeV·cm^2/mg), 4.0% (27.2 MeV·cm^2/mg), and 13.7% (37.6 MeV·cm^2/mg) of after deposition 400 krad(Si). It can be clearly observed that the SEU cross-section of 6T SRAMs shows an increasing trend after TID irradiation, and the maximum increase is 13.7%.

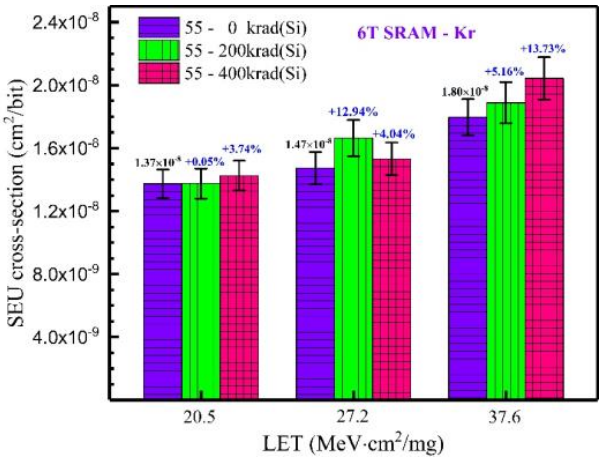


Figure 4. SEU cross-sections versus LET for 6T SRAMs. The purple horizontal column represents data for TID = 0 rad(Si), the green vertical column represents data for TID = 200 krad(Si), and the pink checkerboard represents data for TID = 400 krad(Si).

Zheng et al. investigated the effect of the total dose effect on the SEU cross-section of the SRAMs. The experimental results show that the SEU cross-section of the SRAMs gradually increases after the TID irradiation, and the main oxide trap charge regions of the nanoscale feature device are the buried oxide and shallow trench isolation oxide regions [27,31,35–37]. For the test chip we designed, the SEU cross-section of the 6T SRAM increases slightly after TID irradiation, due to two main reasons: (1) the gate oxide layer thickness of our test chip is only 1.5 nm, so the gate oxide layer cannot trap enough trap charges; (2) the transistor used in the test chip adopts the structure of body under source FET (BUSFET), which eliminates the formation of parasitic leakage channels between the source and drain electrodes caused by the radiation-induced charges trapped in buried oxide (BOX). Therefore, the radiation-induced charges trapped in the shallow trench isolation oxide (STI), rather than in the BOX, were responsible for the increase of the SEU cross-section of the 6T SRAM.

3.2. Effect of Data Pattern on the 6T SRAM SEU cross-section

Figure 5 provides the results for the SEU cross-sections characterized by the Kr ion (20.5 MeV·cm^2/mg) of devices in three different groups: (1) fresh; (2) after deposition of 200 krad(Si); and (3) 400 krad(Si). The mean value of SEU data with error bar at each dose level is depicted in Figure 5. As shown in Figure 5, the mean SEU cross-section of 6T SRAM increases by a factor of 0.1% (55 h), 2.8% (AAh) after deposition 200 krad(Si), with respect to the fresh condition, and it increases by a factor of 3.7% (55h), 6.8% (AAh) after deposition 400 krad(Si). It was observed that the data patterns have little effect on the SEU cross-section of the 6T SRAM after TID irradiation. There are two main reasons for these experimental results. First, the degree of ionization damage of the ultrathin gate oxide layer at 1.5 V was basically the same as the case without voltage addition; second, the main sensitive area of TID of the nanodevice shifted from the gate oxide region to the STI and BOX regions. Therefore, the SEU cross-section of the 6T SRAM after TID irradiation dose had no dependence on the data pattern that was applied during TID exposure.

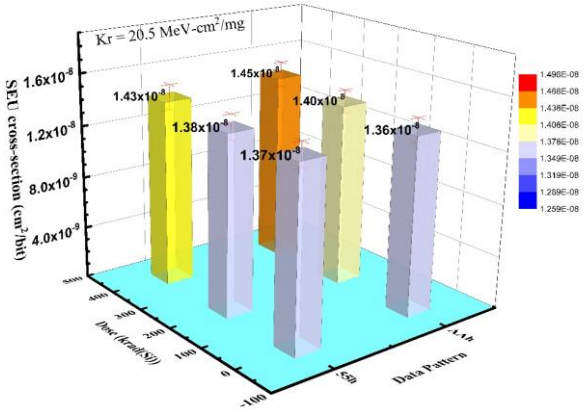
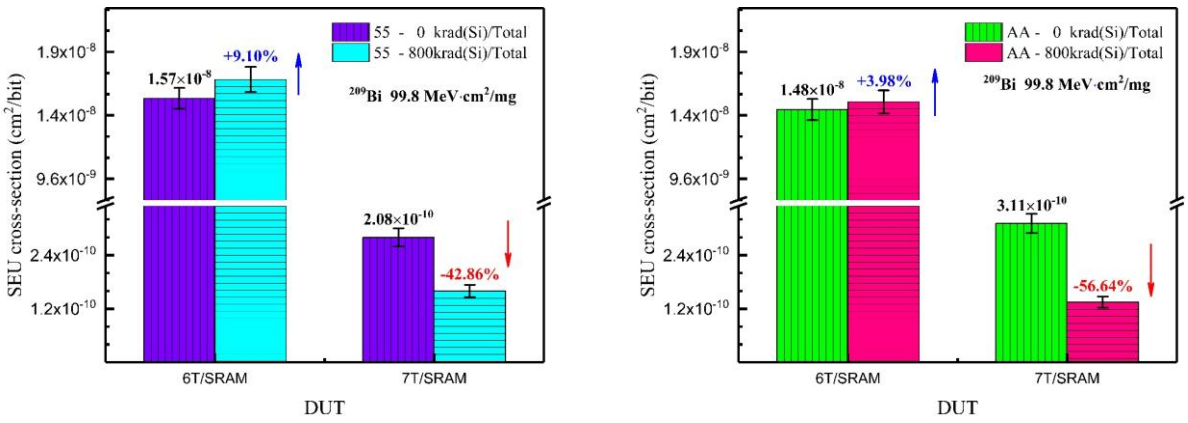


Figure 5. SEU cross-sections characterized by Kr ion versus TID for 6T SRAMs under different data patterns.

3.3. Effect of TID on the 7T SRAM SEU cross-section

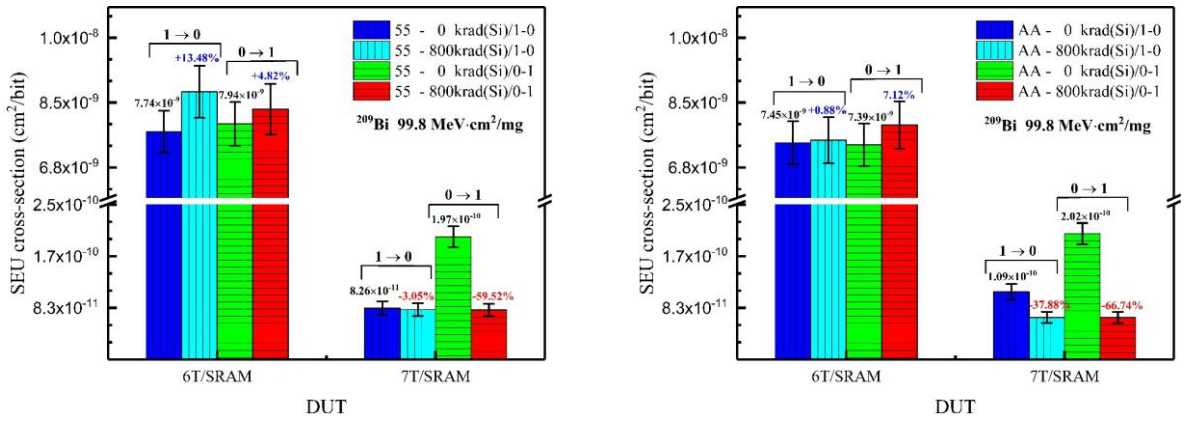
Figure 6 shows the SEU cross-sections of 6T SRAM and 7T SRAM characterized by the Bi (99.8 MeV·cm^2/mg) ion as a function of TID. The SEU cross-sections of 6T SOI SRAM characterized by Bi ion are also increased by TID. As shown in Figure 6, the SEU cross-section of 6T SRAM increased by a factor 9.1% (55 h) and 4.0% (AAh) of after deposition 800 krad(Si), with respect to the fresh condition. Similarly, we did not observe a significant correlation between the SEU cross-section and data pattern applied during TID exposure for 7T SRAM. However, it is interesting to note that the SEU cross-section of the 7T SRAM showed an opposite changing trend to the 6T SRAM. As shown in Figure 6, SEU cross-section of 7T SRAM decreased by factors of 42.9% (55 h) and 56.6% (AAh) after deposition 800 krad(Si), with respect to the fresh condition. Because the 6T SRAM and 7T SRAM were fabricated in the same wafer, the physical dimensions and electrical characteristics of all transistors (N1, N2, N3, N4, P1, and P2) in the memory cell are very similar, except for the delay-hardened transistor, N5. Therefore, we can conclude that the change in the electrical characteristics of the N5 was responsible for the reduction in the SEU cross-section of the 7T SRAM after TID irradiation.



(**a**) (**b**)

Figure 6. SEU cross-sections characterized by Bi ion versus layout structure for SOI SRAMs. The vertical column represents data for TID = 0 rad(Si), and the horizontal column represents data for TID = 800 krad(Si). The data pattern applied during SEU testing was (**a**) 55h and (**b**) AAh.

Furthermore, we investigated the TID effect on the "1→0" upset and "0→1" upset for 7T SRAM SEU types. As shown in Figure 7, the mean "1→0" upset cross-section of 7T SRAM decreased by a factor of 3.1% (55 h), 37.9% (AAh) of after deposition 800 krad(Si), with respect to the fresh condition, and the mean "0→1" upset cross-section decreased by a factor of 37.9% (55 h), 66.7% (AAh) after deposition 800 krad(Si). Therefore, the decrease of the cross-section of "0→1" upset was mainly responsible for the decrease of 7T SRAM SEU cross-section.



(**a**) (**b**)

Figure 7. SEU cross-sections characterized by Bi ion versus layout structure for SOI SRAMs after deposition 800 krad(Si). The vertical column represents data for the "1→0" upset, the horizontal column represents data for the "0→1" upset. The data pattern applied during SEU testing is (**a**) 55h and (**b**) AAh.

4. Discussion

4.1. Transient Propagation Circuit Analysis for 7T SRAM

It is generally believed that, in silicon, electrons have much higher mobility than holes, resulting in the electrons are quickly collected at the drain contacts. Thus, the pull-down nMOSFET biased OFF-state determines the SEU resistance of the 7T SRAM. The equivalent circuits of transient pulse propagation, corresponding to two different SEU types in the 7T SRAM, are shown in Figure 8.

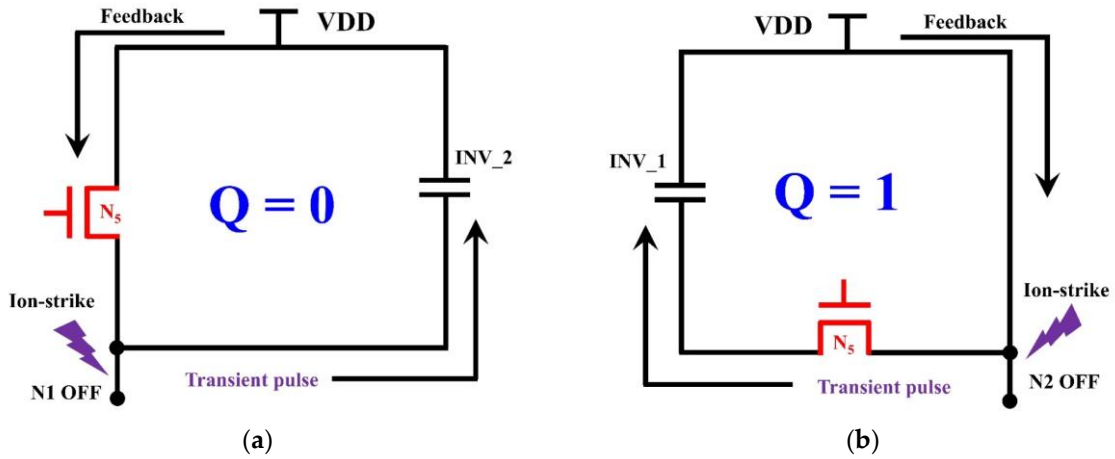


Figure 8. The equivalent circuits of transient pulse propagation corresponding to the (**a**) "0→1" upset type and (**b**) "1→0" upset type in the 7T SRAM.

As shown in Figure 8a, when the Q node is set to low potential, the pull-down nMOSFET N1 in the inverter 1 is turned OFF. Normally, incident heavy ions hitting the N1 will produce a transient pulse, caused by charge collection in the drain. After that, the transient pulse acts on the gate of inverter 2 to gradually increase the potential of the Q node. The potential perturbation in the Q node well further feeds back to the gate of inverter 1 through the delay transistor N5 to gradually decrease the potential of the $\overline{Q}$ node. Finally, the single event transient pulse signal is latched to the memory cell of the 7T SRAM. In this case, the delay transistor N5 indirectly delayed and suppressed the feedback signal of the single event transient pulse, so that the delay-efficiency was lower; thus, the cross-section of "0→1" upset was higher.

As shown in Figure 8b, when the Q node was set to the high potential, the pull-down nMOSFET N2 in the inverter 2 was turned OFF, when the incident heavy ions hitting the N2 produced a transient pulse, caused by charge collection in the drain. After that, the transient pulse through the delay transistor N5 acted on the gate of inverter 1 to gradually increase the potential of the $\overline{Q}$ node. The potential perturbation in the $\overline{Q}$ node well further fed back to the gate of inverter 1 to gradually decrease the potential of the Q node. Finally, the single event transient pulse signal was latched to the memory cell of the 7T SRAM. In this case, the delay transistor N5 directly delayed and suppressed the single event transient pulse, so that the delay-efficiency was higher; thus, the cross-section of "1→0" upset was lower.

4.2. Effect of TID on the OFF-State Equivalent Resistance of Delay Transistor N5

According to previous studies, TID irradiation significantly affects the device's carrier mobility [37–40]. As shown in the equation 1, the carrier mobility of the transistors was mainly affected by three scatterings: phonon scattering, surface scattering, and charged impurity scattering. It has been found that the scattering rate of charged impurities is mainly determined by the semiconductor process, and it is rarely affected by TID. However, phonon and surface scattering are proportional to the electric field intensity perpendicular to the channel direction; the higher the density of oxide trap charge is, the stronger the vertical electric field component is. Therefore, the effect of the TID on the carrier scattering rate was mainly to increase the phonon and surface scattering rates.

$$\frac{1}{\mu_{\mathrm{n}}} = \frac{1}{\mu_1}\left(E_{eff}\right)^{|\alpha_1|} + \frac{1}{\mu_2}\left(E_{eff}\right)^{|\alpha_2|} + \frac{1}{\mu_3}Q_{\mathrm{ot}}\left(\frac{1}{N_i}\right)^{\alpha_3} \quad (1)$$

where α_i and μ_i are the fitting parameters, N_i is the charge density of inversion layer, E_{eff} is effective vertical electric field intensity, and Q_{ot} is the oxide trap charge density.

As shown in Figure 9, a substantial amount of radiation-induced charge was trapped in the STI and BOX of the delay transistor N5 after TID radiation. As a result, the oxide trapped charge generated a vertical electric field in the channel region of the transistor N5. This results in an increase in phonon and surface scattering. Finally, the carrier mobility rate of the delay transistor N5 decreased, and the equivalent OFF-state resistance increased, thus leading to a decrease in the SEU cross-section of the 7T SRAM.

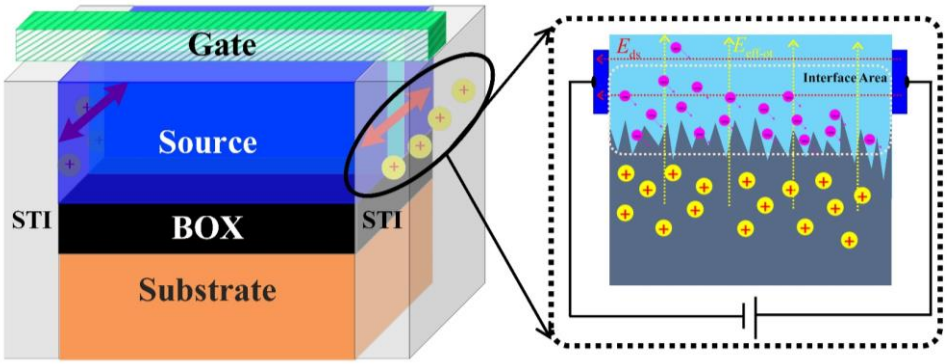


Figure 9. Schematic illustration of the physical mechanism of radiation-induced carrier scattering rate increases in the delay transistor N5 of the 7T SRAM.

4.3. The Advantages of Suppressing SEU with TID

In the natural space radiation environment, there are protons and electrons that can cause TID effects, as well as heavy ions that can cause transient SEE. When the integrated circuit is on-orbit, it will be affected by a variety of radiation effects; that is, there is electrical performance degradation caused by TID, and there is also the transient voltage pulse caused by SEE. Hence, TIDs and SEEs have a natural synergy in the space radiation environment. We found that, when delay transistors are used for hardened circuit design, the TID can cause degradation in the performance of delay transistors, thus suppressing the SEU. Therefore, not only does using delay-hardened transistors for hardened circuit design not affect the operating speed of nano-devices, it also improves the stability of memory cells. Furthermore, the TID effect can be used to suppress the transient SEE and achieve self-optimizing design in natural radiation space radiation environments. Our study provides new insight into radiation-hardened by design (RHBD) technology for nano-integrated circuits.

5. Conclusions

The total ionizing dose (TID) effects on single-event upset (SEU) hardness of silicon-on-insulator (SOI) static random access memories (SRAMs) with 6T and 7T cell designs were explored in this paper. Experimental results show that the SEU cross-section of 6T SOI SRAM is increased by TID and has no dependence on the data pattern applied during TID exposure. However, it is interesting to note that the SEU cross-section of 7T SRAM decreases significantly after TID exposure. Furthermore, in our experiment, opposite changes intendencies of SEU cross-section for 6T and 7T SOI SRAMs were observed after TID irradiation. The mechanism behind the experimental results of 6T SRAM is that OFF-state leakage of pull-down nMOSEFTs increases after TID irradiation, since the parasitic transistor is turned ON by radiation in the shallow trench isolation oxide (STI) region. However, the radiation-induced decrease in carrier mobility in delay transistor N5 of the 7T SRAM is responsible for the decrease of the SEU cross-section. Because radiation-induced charges trapped in the STI and buried oxide (BOX) improve the carrier scattering rate, the OFF-state equivalent resistance of delay transistor N5 increases, causing the stronger suppression of transient pulses and feedback signals, ultimately leading to SEU cross-section decreases. Our experimental results provide a new insight into the radiation-hardened by design (RHBD) used in nano ICs.

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Data Availability Statement: Data available on request due to restrictions eg privacy.The data presented in this study are available on request from the corresponding author. The data are not publicly available due to the research results having potential commercial value.

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Conflicts of Interest: The authors declare no conflict of interest.

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