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Review

Recent Trends in Copper Metallization

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Abstract: The Cu/low-k damascene process was introduced to alleviate the increase in the RC delay of Al/SiO_2 interconnects, but now that the technology generation has reached $1\times$ nm or lower, a number of limitations have become apparent. Due to the integration limit of low-k materials, the increase in the RC delay due to scaling can only be suppressed through metallization. As a result, various metallization methods have been proposed, including traditional barrier/liner thickness scaling, and new materials and integration schemes have been developed. This paper introduces these methods and summarizes the recent trends in metallization. It also includes a brief introduction to the Cu damascene process, an explanation of why the low-k approach faces limitations, and a discussion of the measures of reliability (electromigration and time-dependent dielectric breakdown) that are essential for all validation schemes.

Keywords: BEOL; interconnect; copper; low-k; metallization; scaling

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1. Introduction

Continuous developments in integrated chip scaling have improved circuit density and chip performance in recent decades. Moore's law, which states that the number of transistors on a microchip doubles every two years, is now accepted as an empirical law. These advances have been achieved not only with simple reductions in dimensions; they have also been spurred by new patterning approaches, innovative device architectures, tool improvements, design–technology co-optimization, and the integration of new materials [1,2].

The increasing number of transistors on an integrated chip usually leads to an increase in the complexity of the interconnections. This can be resolved by increasing the number of vertical stacking levels based on hierarchical wiring schemes for effective design allocation [3,4]. A hierarchical wiring system is commonly constructed by vertically distributing various metal levels with different minimum pitches. Depending on their purpose, these interconnects can be divided into three groups: local, intermediate, or global interconnects.
Local interconnects: The minimum metal pitch is applied to the levels closest to the transistor. They adopt state-of-the-art processes and technologies with low-k dielectrics and metallization to minimize the resistance−capacitance (RC) delay, which is most affected by patterning.
Intermediate interconnects: They connect primitive cells or signal transmission, such as the system clock. Because the congestion is lower than for local interconnects, a relaxed metal pitch and an increase in thickness are allowed.
Global interconnects: These are the wiring levels at the top of the integrated chip and are used to minimize the power transmission and voltage drop. They typically have a thick metal layer and a relaxed pitch. However, they are subject to additional requirements related to connections with the outside of the chip, i.e., the packaging.

The purpose of scaling is to aggregate more transistors within the same unit area while improving the performance of the semiconductor chip [5]. When the dimensions of a transistor are reduced, the transit time of the carriers passing through the transistor channel decreases. However, the interconnect performance is degraded due to an increase in the RC delay,

which is the product of the conductor resistance (R) and the dielectric capacitance (C). R and C are calculated using Equations (1) and (2), respectively:

$$R = \rho \frac{L}{WT} \tag{1}$$

$$C = k\frac{LT}{S} \tag{2}$$

where ρ is the metal resistivity and k is the dielectric constant. L, W, and T are the length, width, and thickness of the metal lines, respectively, while S is the spacing between the metal lines. Based on these equations, it can be seen that the interconnect RC delay is determined by the physical dimensions and constituent material of the wiring.

W and S are determined by the physical scaling in terms of the minimum pitch. However, T and H (where H is the via height, the space between M_x and M_{x+1}) can be optimized during the fabrication process. Therefore, attempts have been made to improve the RC delay by optimizing the physical dimensions via process integration based on the given material and the target electrical and reliability specifications. Another consideration is the metal and dielectric insulators in the interconnects. Traditionally, aluminum (Al) and SiO_2 have been used as metal and dielectric insulators, respectively, since the introduction of 3 μm technology. However, as shown in Figure 1, when the technology generation reached 0.25 μm, the interconnect RC delay began to exceed the gate delay, leading to a bottleneck for integrated chip performance [6].

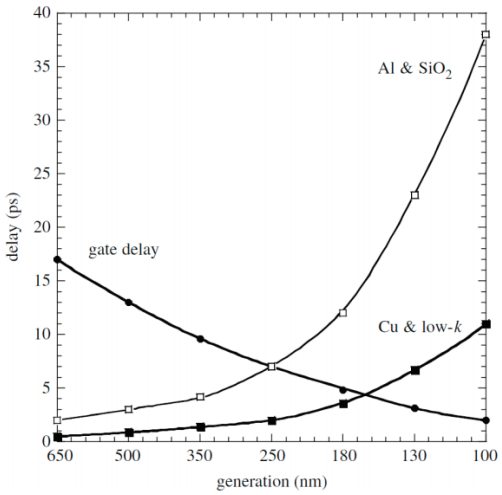

Figure 1. Gate and interconnect delay in accordance with technology generations (ITRS '99) [6].

In order to address this increase in the RC delay, new materials to replace Al and SiO_2 have been sought. Due to their low resistivity, copper (Cu), gold (Au), and silver (Ag) have been considered as replacements for Al, with Cu in particular showing lower resistivity and producing better electromigration (EM) performance [7]. In addition, porous SiCOH (pSiCOH) has been developed from fluorinated silicon glass (FSG) and SiCOH (organosilicate glass; OSG) as a low-k material to replace SiO_2 (k~4.3). The replacement of Al with Cu was successfully achieved with the release of mass-produced products in 1997 [8], and low-k materials began to be introduced in earnest with the emergence of 90 nm technology [9,10]. Furthermore, over the last 25 years, Cu and low-k materials have served as successful platforms for back-end-of-line (BEOL) interconnects.

However, as the minimum metal pitch approaches the electron mean free path (eMFP) of Cu (39 nm), various interconnection problems have emerged, including patterning restrictions. In particular, while dual-damascene (DD) schemes, which include a metal hard mask (HM), are unaffected, single patterning (SP) is no longer possible at the wavelength of argon fluoride (ArF; 193 nm). Various resolution enhancement techniques (RETs) and

immersion lithography have been employed to overcome the limitations of SP, but the use of multiple patterning (MP) is inevitable. If scaling continues at its current rate despite the introduction of extreme ultraviolet (EUV) lithography, MP will be required for future nodes.

Another issue is the limitations of low-k materials. The porous low-k material pSiCOH has been successfully implemented at 45 nm [10], but the development of increasingly low-k materials is hindered by the loss of mechanical strength with an increase in porosity and integration issues arising from plasma-induced damage (PID) [11]. Finally, challenges also arise for Cu metallization as the metal dimensions shrink [12–14]. Cu resistivity increases with higher refractory metal ratios, surface scattering, and grain boundary (GB) scattering in the Cu lines. Various attempts have been reported to overcome this, with the most recent trend being to employ metals with barrier-free advantages and the ability to be used in direct metal etching (DME) [15,16]. From this perspective, ruthenium (Ru) has emerged as the most promising metal to replace Cu [15,17]. This suggests that BEOL interconnects will no longer be confined in Cu damascene structures only.

2. Cu Dual-Damascene Interconnects

Unlike Al, Cu cannot be easily patterned using reactive ion etching (RIE) due to the low volatility of $CuCl_2$ and CuF at low temperatures. Due to this constraint, the damascene process was introduced as a replacement for subtractive etching [18,19]. Cu also has reliability issues due to its high diffusivity into the surrounding dielectric material unless it is perfectly encapsulated [20–22]. Many studies have sought to resolve the diffusion issue, with tantalum nitride (TaN) mostly employed as a diffusion barrier based on comprehensive comparisons of many candidate materials [23]. IBM announced the first product implementation of a Cu damascene structure in 1997 [7], since which this structure has become the standard platform for on-chip interconnects with improved resistivity and reliability compared with Al interconnects.

In the damascene process, the dielectric is first deposited onto the substrate and then etched to form a metal and via profile. Finally, the incoming profile is filled with Cu metal and the excess Cu removed using chemical mechanical polishing (CMP).

Damascene interconnects have two variations: single-damascene (SD) and dual-damascene (DD) structures. Figure 2 presents a schematic comparison of SD and DD interconnects. The SD process produces the via and the trench separately, while the DD process conducts via and trench patterning separately but their metallization together. Due to the economic advantages of reducing the number of steps in a process, the DD process is widely preferred. However, the SD process is still used for particular purposes such as M1 or with thick metal layers used for global interconnects. SD interconnects are employed for M1 because connection with the CNT module is required, and an SD structure is effective if a thick metal such as an inductor is required.

The DD fabrication process can be divided into via-first and trench-first schemes according to the patterning order. In the trench-first scheme, which was the first DD process, there is no fence between the via and trench, so depositing the seed Cu for electroplating is easy. However, this approach suffers from indirect alignment and a narrower depth of focus for via lithography due to the step height, leading to a non-planar resist. These issues place a restriction on scaling. In contrast, the via-first scheme has a broader lithography processing window, though it is susceptible to plasma damage to the dielectric when employing a porous low-k material. Therefore, DD processing with a metal HM has generally been employed since the 32 nm technology generation [19]. This method effectively combines the advantages of the via-first and trench-first schemes. Figure 3 presents the differences in the plasma damage arising from the via-first and trench-first schemes using a titanium nitride (TiN) metal HM.

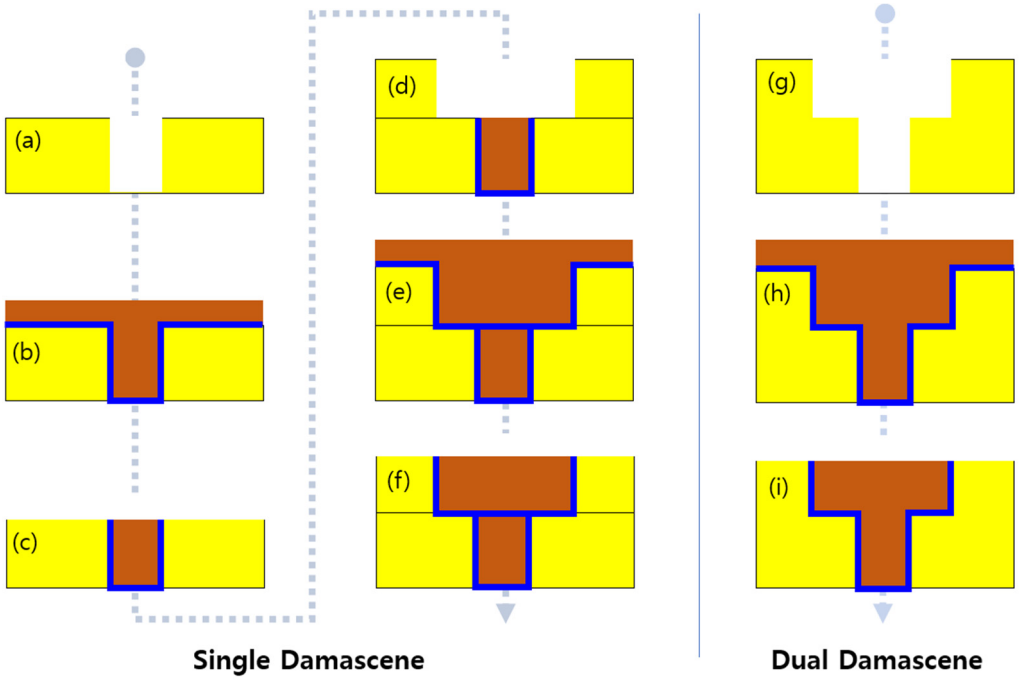

Figure 2. Process comparison of the (**a**–**f**) SD and (**g**–**i**) DD schemes: (**a**) etching of the via in the deposited ILD, (**b**) filling of the via with Cu, (**c**) CMP of the excess Cu from the via, (**d**) etching of the trench in the deposited ILD, (**e**) filling the trench with Cu, (**f**) CMP of the excess Cu from the trench, (**g**) trench/via etching in the ILD, (**h**) filling with Cu, and (**i**) CMP of the excess Cu.

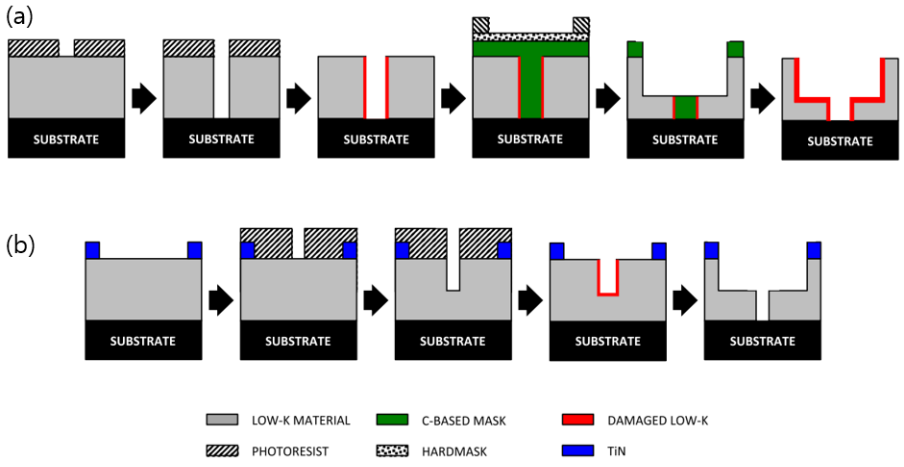

Figure 3. Process flow for (**a**) via-first and (**b**) trench-first approaches with a metal hard mask (HM) [11]. The plasma damage to the low-k material is lower for the trench-first scheme.

Patterned profiles created using the DD process need to be filled using metallization. Cu metallization consists of three steps: barrier/liner deposition, seed Cu deposition, and bulk Cu deposition [12]. Physical vapor deposition (PVD) is employed for the first two steps, while electroplating with additives is used as the standard process for the third. Following metallization, the excess Cu is removed using CMP to produce the final wiring. A dielectric barrier (DB) covers the surface after Cu CMP has been completed. This process is repeated until the final metal is connected to the bonding structure.

The Cu/low-k damascene process has served as a platform for the successful fabrication of BEOL interconnects while satisfying the scaling roadmap over the past 25 years. However, as scaling progresses, patterning, low-k materials, and metallization are all subject to process limitations. The next section summarizes these limitations and describes the approaches that have been proposed to overcome them.

3. Low-k Dielectric Materials

A dielectric material electrically insulates interconnections. When a voltage is applied to an electric wire, the dielectric material induces parasitic capacitance, causing cross-talk noise, power dissipation, and RC delay. These parameters are proportional to the dielectric constant k of the material [8]. However, dielectric materials should not only serve as electrical insulators; they also require reliable mechanical, thermal, chemical, and physical stability under the processing conditions and compatibility with other materials for successful integration [24].

SiO_2 is a dielectric material used for 2 to 0.25 µm CMOS technology generations with a dielectric constant of ~4.2. Though SiO_2 satisfies the dielectric requirements mentioned above, its k value no longer mitigates the RC delay. Therefore, efforts have been made to find materials with a lower k value that also satisfies the other insulator requirements.

The dielectric constant represents the ratio of the permittivity of a material to that of a vacuum and is generally described using Equation (3) [25]:

$$\frac{k-1}{k+2} = \frac{N}{3}\alpha \tag{3}$$

where $k = \varepsilon/\varepsilon_0$ and ε and ε_0 are the permittivity of the material and vacuum, respectively, N is the number of molecules per unit volume (density), and α is the total polarizability, consisting of electronic (α_e) and distortion (α_d) polarization.

By decreasing the total polarizability (α) and/or density (N), the k value of the dielectric can be reduced. Density has a more substantial effect on the dielectric constant than does polarizability because density can be reduced to 0 (in an air), leading to $k = 1$. In the first-generation low-k material obtained using this method, some Si-O bonds were replaced by less polarized Si-F bonds, resulting in FSG [25,26]. In the second generation, a low dielectric constant was achieved using silsesquioxane-based materials and the chemical vapor deposition (CVD) of OSG (SiCOH) [25]. The low dielectric constant of these materials is partially due to the lower density compared with SiO_2. The density is reduced by breaking the 3D Si-O-Si bonding network via the incorporation of terminating Si-H or Si-R (where R is an organic moiety such as CH_3) [27].

Porosity must also be introduced in order for dense low-k materials to achieve k values below 2.5. This can be accomplished using sacrificial nanoparticles (i.e., porogen) desorbed in a high-temperature baking step, though maintaining a solid matrix structure is essential to avoid weakening the mechanical properties. The resulting material is pSiCOH [8,28]. Table 1 compares the characteristics of low-k materials for each generation.

Table 1. Essential properties of representative dielectric materials [6].

Properties	SiO_2	FSG	Dense Low-k (Osg)	Porous Low-k
density (g/cm^3)	2.2	2.2	1.8~1.2	1.0~1.2
dielectric constant (k)	4	3.5~3.8	2.8~3.2	1.9~2.7
modulus (gpa)	55~70	~50	10~20	3~10
hardness (gpa)	3.5	3.36	1.2~2.5	0.3~1.0
cte (ppm/k)	0.6	~0.6	1~5	10~18
thermal conductivity (w/mk)	1.0	1.0	~0.8	0.26
porosity (%)	NA	NA	<10	25~50
average pore size (nm)	NA	NA	<1.0	2.0~10
breakdown field (mv/cm)	>10	>10	8~10	<8

However, low-k materials with high porosity suffer from lower mechanical strength, lower thermal conductivity, poor adhesion to barriers, plasma damage, and moisture absorption [29]. Figure 4 presents the relationship between mechanical strength and changes in the k value. For FSG, the difference from SiO_2 is insignificant in terms of the elastic modulus, but a rapid decrease occurs for dense low-k OSG and pSiCOH.

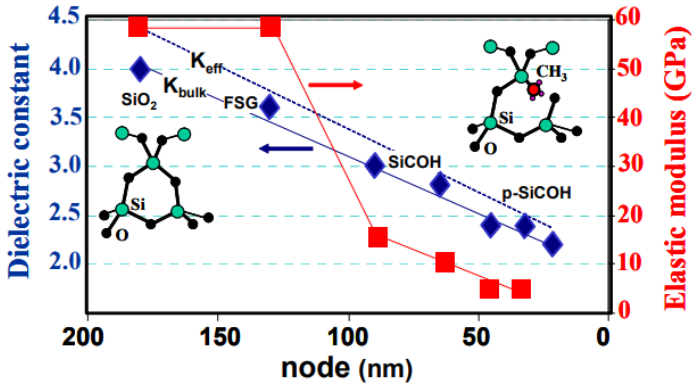

Figure 4. Relationship between the dielectric constant and the elastic modulus for different generation low-k materials. Reprinted/adapted with permission from Ref. [18]. 2009, IEEE.

Unlike low-k inter/intralayer dielectrics (ILDs), low-k DBs offer the integration requirements for downstream manufacturing processes [30]. Low-k DBs are essential components of BEOL interconnects and contribute to their capacitance. This has an increasingly significant impact on technology generations, allowing a decrease in interconnect dimensions. New DBs have a low k value and a low thickness, which reduces the impact on the capacitance of the interconnection and increases reliability concerns. SiN DBs (k~7.0) were replaced by SiCH and SiCNH (k~5.3) caps in 90 nm technology, and thus, the contribution of these DBs to total capacitance has been relatively small in several subsequent technical nodes. However, this contribution has since increased because low-k DBs have not scaled in proportion with the ILDs [8]. In other words, though the thickness of ILDs has decreased every time a new technology node is created, the thickness of low-k DBs cannot decrease at the same rate without degrading the DB characteristics [31,32].

Although low-k dielectrics have been introduced, ensuring a reliable interconnect process under k~2.4 is challenging. However, the use of an air gap is a promising approach to significantly reducing the capacitance because it can achieve an effective dielectric constant below 2.0. Figure 5 presents a cross-sectional image of an air gap.

Although this concept was already known beforehand [33–37], it was first commercially implemented in Intel's 14 nm technology using an 80 nm pitch multilayer (M4 and M6), with RC benefits of up to 17% [38,39]. In addition, IBM recently suggested the possibility of extending the air gap to the thin-wire level by achieving a capacitance reduction of about 20% compared with the baseline process using an ultra-low-k (ULK) dielectric (k~2.4) [40]. However, air gaps have been limited to selectively applied critical paths.

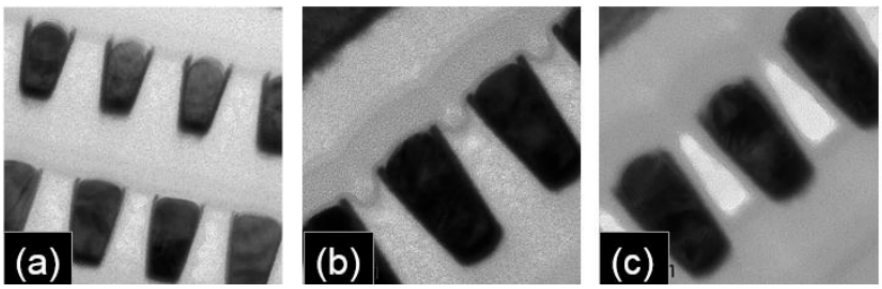

Figure 5. Cross-sectional images of (**a**) a baseline wafer without air gaps, (**b**) with air gaps excluded, and (**c**) with air gaps Reprinted/adapted with permission from Ref. [40]. 2017, IEEE.

4. Metallization

A typical DD Cu line is surrounded by a barrier, a liner, and a cap (Figure 6) [41]. The barrier promotes metal adhesion to the dielectric, protects Cu from oxidation, and acts as a nucleation layer for the liner metals. The liner facilitates Cu seeding and the plating process and, more importantly, improves the Cu interface for the suppression of

EM. After the emergence of 14 nm technology, a metal cap was applied to the top of the line to improve for EM performance due to the small volume of Cu [42]. A diffusion barrier is required to prevent the Cu from mixing with the surrounding dielectric material when manufacturing a Cu interconnect with a damascene structure. The barrier layer reduces the cross-sectional area of the interconnect, and the effective resistance of the Cu line becomes higher than that of a barrier-free Cu line. The increase in resistivity due to the barrier increases significantly when the width of the interconnect line is reduced. According to Matthiessen's law, line resistivity consists of bulk resistivity, impurity scattering, surface scattering, and GB scattering [43,44]. Before the emergence of 7 nm technology, bulk resistivity and impurity scattering usually determined line resistivity. However, since then, surface scattering and particle boundary scattering have taken on greater importance. For surface scattering, it is essential to minimize the volume fraction of Cu occupied by the barrier and liner, while particle boundary scattering is likely to affect scattering at the interface and the Cu grain size. This section summarizes important studies reported to date on these issues.

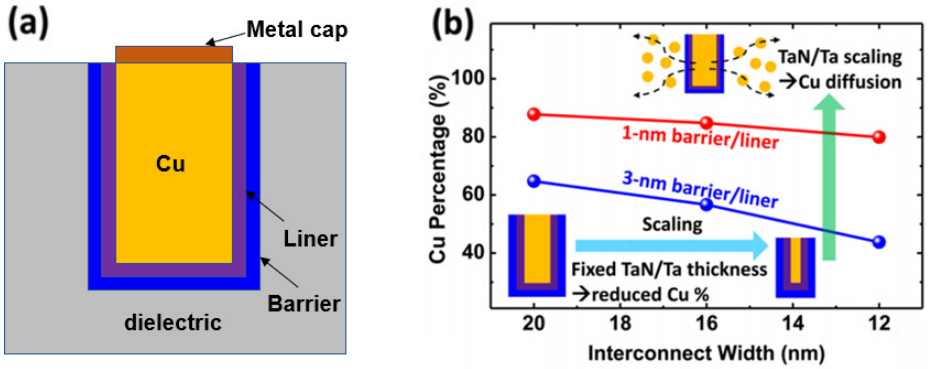

Figure 6. (**a**) Typical metallization of a Cu line with a barrier, liner, and metal cap. (**b**) Scaling challenges for the barrier and liner; in particular, a lower cross-sectional area is occupied by Cu with scaling [41].

4.1. TaN Barrier/Liner Scaling

In order to maximize the Cu volume fraction, the TaN/Ta liner thickness must be reduced. In addition, the thickness of the Cu seed needs to be reduced to prevent the top pinch-off shape during subsequent Cu electroplating. However, the nonconformal step coverage of PVD results in gap-fill problems caused by the overhang and high resistance due to the thick barrier at the via bottom. Therefore, atomic layer deposition (ALD)/CVD is preferred for maximizing the gap-filling window and minimizing the resistance.

Several approaches have been explored for reducing the TaN barrier thickness. First, the minimum thickness can be reduced without sacrificing TaN barrier properties using PVD [45]. In particular, based on time-dependent dielectric breakdown (TDDB) measurements using a planar capacitor structure, TaN barrier characteristics have been shown to be retained even if the thickness is reduced to as low as 0.8 nm. In addition, it has been reported that using a Co/Ru liner instead of a Ta liner significantly improves the overall integrity of the TaN barrier [45]. However, due to the step coverage limit and the overhang problem associated with PVD, it is necessary to switch to ALD as the dimensions decrease. However, TaN thermally deposited using ALD has a higher number of impurities than PVD-fabricated TaN films, a lower film density, a higher resistance, and a lower interface quality, meaning that it cannot emulate the performance of PVD TaN at the same thickness. For this reason, PVD Ta and ALD TaN have been employed as bilayers (1 nm/1 nm) to reduce the thickness while ensuring the barrier properties [46]. Another approach is treating ALD-fabricated TaN in a PVD chamber to transform it into PVD-like film with optimal density and resistivity [47,48]. Using this method, the TaN thickness is 1.2 nm, compared with 1.5 nm for a Co liner and 2.0 nm for a Ru liner [48]. As a result, ALD has been combined with PVD to maintain the barrier properties and a low TaN thickness.

Scaling of the liner has also been actively carried out. The ALD/CVD method is required to overcome the step coverage and overhang problems, but a Ta liner cannot be used. Therefore, replacements for the Ta liner have been considered. Of these, Ru has received significant attention due to its suitability for ALD/CVD and the possibility of direct Cu plating without a PVD Cu seed layer [49–55]. In addition, Co has also been considered as a replacement for the Ta liner [56]. In [41], a Ru liner was found to be superior to a Co liner for Cu filling and electroplating with a liner thickness of 2 nm. However, the resistance of Ru was about 10% higher than that of Co as revealed by the temperature coefficient of resistance (TCR), which was believed to be due to interface and GB scattering. A Co liner has also been shown to outperform a Ru liner in terms of EM characteristics [57].

However, in order to fully exploit the excellent void-free gap-fill performance of Ru liners, approaches to improving their EM deficiencies have been reported. Co caps have been established as a standard process since the emergence of 14 nm technology. As a result, a significant improvement in EM performance has been observed with a Ru liner as the Co cap thickness increases [57]. It has also been demonstrated that the EM problem arises from the diffusion of Co from the cap to the liner due to the Co concentration gradient between the two [57–59]. Thus, a Co-doped Ru liner has been proposed to overcome this problem, and EM improvements have been reported [58,59]. Efforts to scale the TaN barrier and Co/Ru liner continue, but if the metal half-pitch decreases below 10 nm, the barrier/liner scaling limit is reached.

4.2. Selective Barrier Schemes

As advanced technologies emerge, the importance of the resistance and reliability of the vias increases. In particular, via resistance is strongly affected by the bottom thickness of the TaN. Therefore, as scaling progresses, the via resistance rapidly increases due to the thicker TaN. Furthermore, one of the most critical areas of a Cu-based DD structure is the bottom of the via, where the two metal levels meet [60], so selective deposition control of the via bottom barrier is advantageous for improved reliability. In this vein, argon (Ar) sputtering was used as a precleaning PVD barrier/liner [60]. The barrier-first process was conducted in the order of TaN/Ar sputtering/Ta instead of Ar sputtering/TaN/Ta to remove TaN in the via bottom and obtain a Cu/Ta/Cu interface. However, this process disappeared when the precleaning method for removing Cu oxide was changed from Ar sputtering to the oxide-reduction method.

Now that the via size is much smaller, self-assembled monolayers (SAM) have been pursued [61,62]. Figure 7 presents the process for the formation of a selective barrier on the via bottom. The Cu surface is passivated by depositing a SAM on the Cu surface subjected to the CuO_x reduction treatment. The SAM should be highly selective and self-limited and be adsorbed onto metals but not other peripheral dielectrics. However, when the SAM attaches to the metal surface, it interferes with the adsorption of ALD TaN precursors, resulting in significant nucleation delays in ALD TaN growth [61,62]. As a result, ALD TaN does not deposit on the via bottom area where the SAM is located. The SAM is finally removed. The SAM process needs to be developed further before it can be adopted for mass production. Nevertheless, because it can achieve a reduction in the via resistance of about 50% and its TDDB and EM results are equivalent to the process of record (POR), it is likely to be useful in future advanced technologies [61].

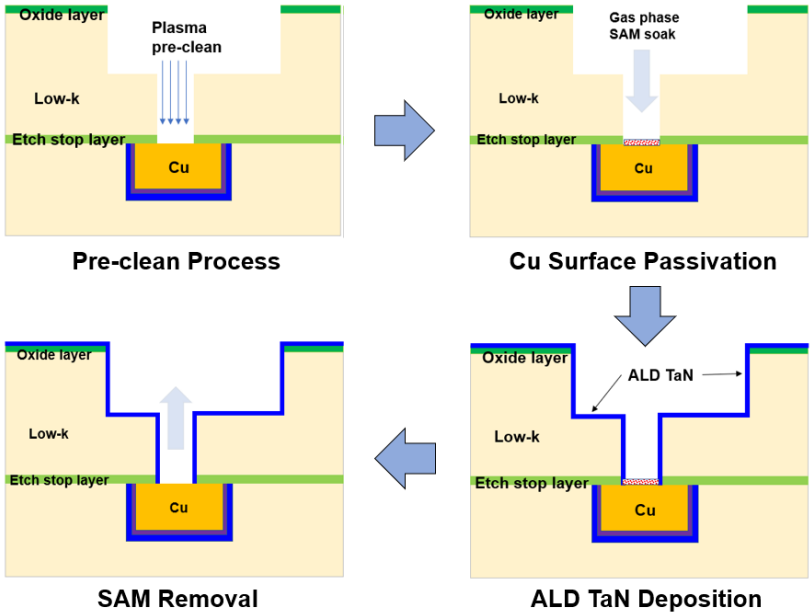

Figure 7. Selective barrier integration process. Reprinted/adapted with permission from Ref. [61]. 2021, IEEE.

4.3. Self-Forming Barriers

Another promising approach to Cu extendibility is the through Co self-forming barrier (tCoSFB), a method in which manganese (Mn) atoms added to the seed Cu diffuse through the thin Co liner layer to form a strong diffusion barrier at the interface between the trench and the dielectric, as seen in Figure 8 [63–66].

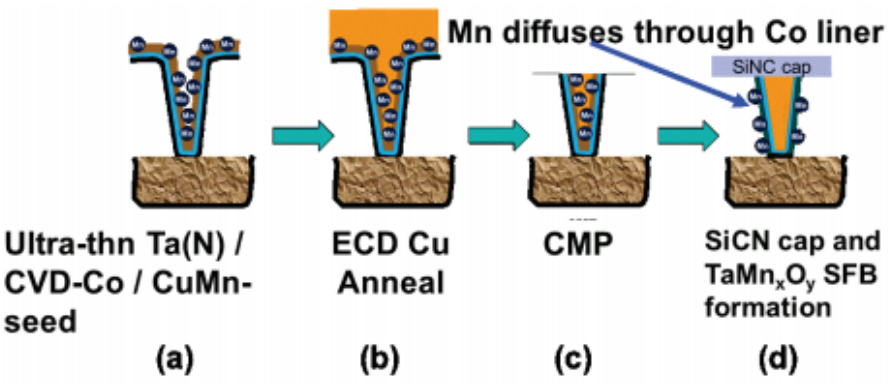

Figure 8. Through Co self-forming barrier (tCoSFB) structure and fabrication process. (**a**) an ultra-thin Ta(N)/CVD-Co film stack is formed on the patterned ULK pSiCOH surfaces, followed by a high-Mn% PVD-Cu(Mn) seed layer. (**b**) Cu electroplating and post-plating anneal. (**c**) CMP. (**d**) a PECVD SiCN(H) dielectric cap is deposited. Reprinted/adapted with permission from Ref. [63]. 2015, IEEE.

Initially, the Mn dopant is employed to form $MnSi_xO_y$ at the dielectric and Cu interface [64,65,67,68]. If CuMn seed deposition occurs without a barrier/liner and Cu plating and annealing are conducted, an SFB is created. This $MnSi_xO_y$ barrier is very thin and uniform, and its EM and TDDB performance is similar to that of POR. However, vertical trench triangular voltage sweep (VT-TVS) and O_2 barrier tests indicate that $MnSi_xO_y$ is inadequate for blocking Cu and O_2 diffusion, which led to the switch from the SFB to tCoSFB containing thin Ta(N) and Co [69].

The advantage of the tCoSFB process is that the cross-sectional area of Cu in the wiring can be maximized, and low line resistance can be obtained due to the 1 nm thickness of

the Co liner and Ta barrier. However, because the line resistance and reliability balance are controlled by the Mn concentration of Cu(Mn) PVD, an increase in resistance may occur. Nevertheless, compared with the POR process, the results are encouraging, with improved resistance and EM and TDDB performance [66,70].

4.4. Hybrid Metallization

At the system-on-chip level, vias have become much more important for signal routing, and via resistance has increased significantly when downscaling the bottom contact area of the via. Therefore, introducing barrierless metal to the via is valuable, and metal−metal selective deposition is essential for the high-aspect-ratio (AR) vias. Hybrid metallization is a method of pre-filling a via with a barrierless metal and then filling the remaining metal area using Cu metallization, as seen in Figure 9 [71].

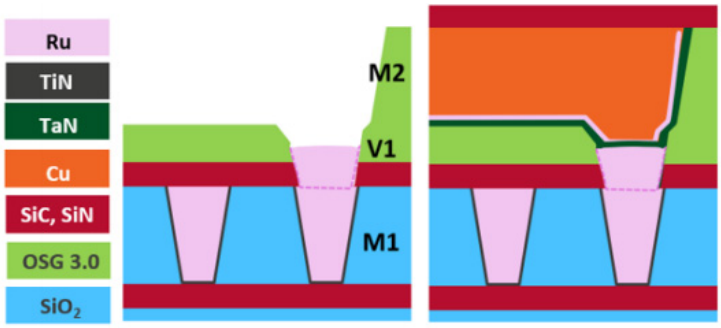

Figure 9. Schematic diagram of Cu hybrid metallization in a two-metal system: (**left**) Ru pre-fill on Ru followed by (**right**) barrier/liner Cu trench metallization. Reprinted/adapted with permission from Ref. [71]. 2020, IEEE.

A barrierless prefill has a number of advantages. First, the prefill moves the barrier position of the Cu DD from the bottom to the top of the via, increasing the tapered via cross-section and reducing the resistance. Second, the gap–fill margin increases because SD trench metallization is employed. Third, because the high-AR vias are excluded, step coverage can be achieved with a thinner barrier/liner [72]. In addition, the optimized barrierless prefilling process may reduce RC delay by increasing the height of the vias and trenches, which can significantly improve circuit performance [73].

The first reported via prefill used Co [73]. However, due to Co ion drift, it was found that barrierless Co was not possible and that TiN barriers are required [72,74]. Ru has been found to be suitable for barrierless prefilling, resulting in a 40% reduction in via resistance and EM results that are similar to those for POR [71].

4.5. Alternative Metals

The thickness of the barrier layer cannot arbitrarily be reduced. If the thickness is less than a certain threshold, it no longer functions as a Cu diffusion barrier. Based on past experimental results, it is unclear whether the barrier/liner combination can have a thickness lower than 2 nm [45–47,75]. However, a barrierless solution is required when the half pitch falls below 10 nm, and thus, new metals to replace Cu have been sought. Some of these metals have a larger bulk resistivity than Cu but do not require a thick barrier/liner and exhibit lower resistance at sufficiently small dimensions because their inelastic average free path is shorter than that of Cu (39 nm) [76,77]. Examples of metals and substitutes proposed under these conditions include Ir, Rh, Mo [78], and W [79], but experimentally verified cases are rare except for Co and Ru [80–83].

Figure 10 displays the line resistance derived from the TCR according to the cross-sectional area of the conductor. Cu has a higher resistance than Ru and Co below ~400 nm^2 at a 16-nm metal width and an AR of 2 [84].

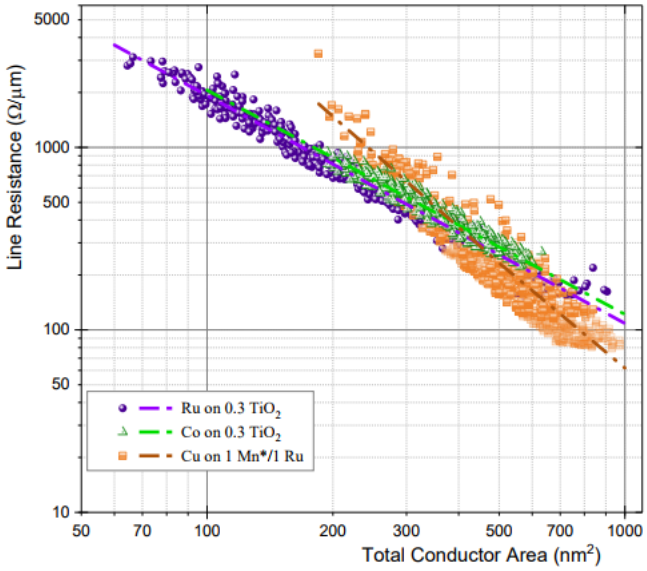

Figure 10. Logarithmic comparison of the damascene line resistance versus the total conductor cross-sectional area for Ru, Co, and Cu nanowires as determined using the TCR. The dotted lines are used to highlight the general trend. Reprinted/adapted with permission from Ref. [84]. 2018, IEEE.

4.6. Ru Semi-Damascene Schemes

Ru can be used in barrierless damascene structures and direct metal etching (DME). Figure 11 shows Ru metal implemented with subtractive etching.

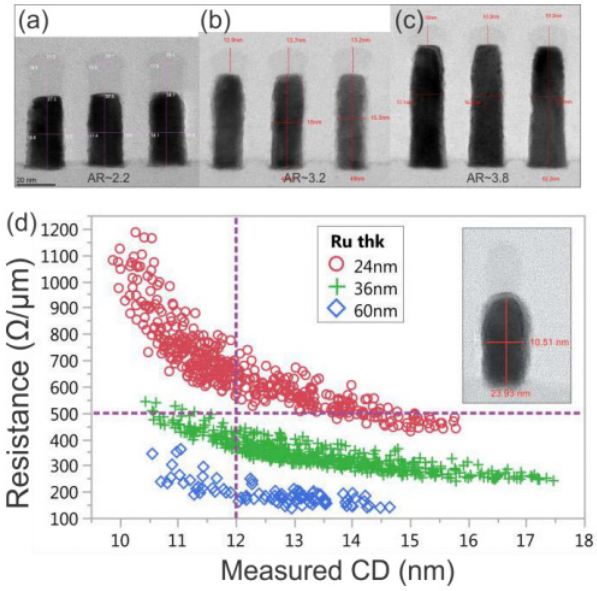

Figure 11. Cross-sectional TEM of patterned Ru films with a thickness of (**a**) 24 nm, (**b**) 36 nm, and (**c**) 60 nm. (**d**) Corresponding R vs. CD for all structures on each wafer. Reprinted/adapted with permission from Ref. [85]. 2018, IEEE.

The use of subtractive etching opens up many possibilities that have not previously been possible for Cu damascene structures. First, because the Ru film is deposited on the entire wafer, the grain size is not limited by the damascene profile width. Therefore, it can significantly restrain the increase in resistance due to GB scattering. Second, the metal thickness is determined by Ru deposition, not by metal CMP. Therefore, if necessary, the resistance can be reduced by increasing the Ru thickness, and there is no AR-related filling problem. Third, because the metal thickness is not affected by the pattern density but is

determined by the uniformity of the deposited Ru film, the variation in the metal Rs will be reduced. Finally, a space between Ru metal with an increase in the AR could be introduced by employing an intentional air gap.

The semi-damascene process is an interesting approach that utilizes the advantages of Ru, such as barrierless designs and subtractive etching. This method begins with vias fabricated in a low-k material, and the vias and trench layers are filled using a single deposition step. Subtractive etching is then applied to the trench patterning [14,85–87]. According to the latest result, Ru line resistance outperforms Cu at 270 nm^2 or lower (CD < 12 nm) based on line resistance vs. conducting area plot, and the EM and TDDB results are promising so far [17]. For this reason, the Ru semi-damascene process is the most competitive candidate for use in 3 nm technology and lower.

Figure 12 shows the conceptual summary of the metallization approaches mentioned in this section as they have evolved. As shown in the figure, the main trend of metallization has been to reduce the area ratio occupied by the barrier in the scaled wire. Traditional attempts were to reduce the existing barrier/liner (TaN/Ta) thickness by replacing a new process method (ALD) and a new liner material (Co/Ru). After that, it was gradually developed to implement a barrier-free process using Co or Ru. Moreover, the boundary has recently been extended to the subtraction etch process using Ru instead of the Cu damascene scheme.

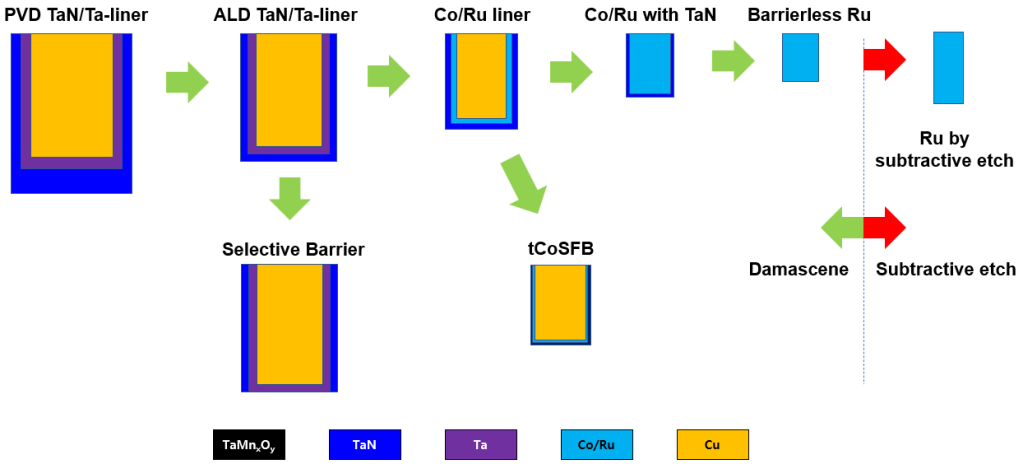

Figure 12. Trends in recent metallization approaches.

In addition to the metallization approaches mentioned here, various studies are being conducted. One of them is the study of a 2D-like barrier. The approach is to minimize the volume fraction of Cu occupied by the barrier by replacing the thick Ta or TaN barrier with 2D-like materials such as graphene [88,89], MoS_2 [41,90], TaS_2 [41], and WSe_2 [41].

In the process of these efforts, the limitation of Cu metallization in CMOS interconnects is becoming more apparent. However, it is interesting that Cu plating is actively applied in other areas, such as solar cells' silicon heterojunction (SHJ) [91,92].

5. Reliability

Recognizing the underlying causes of reliability problems in scaled Cu/low-k interconnects and clearly understanding the degradation mechanisms are essential. EM and TDDB are standard methods for assessing the reliability of metal and dielectrics. Therefore, EM and TDDB are summarized in this section, and countermeasures proposed for improving reliability in the pursuit of scaling are discussed.

5.1. Electromigration

EM is a phenomenon in which metal atoms move in a metal conductor due to a high current density [93]. When EM stress is continuously applied, voids appear on the cathode side of the wire as the metal atoms accumulate on the anode side, resulting in hydrostatic

stress. This stress also produces an inverse flux of atoms in the opposite direction to the electron transport flux, which is referred to as the Blech effect or the short-length effect [94,95]. This back-stress force is more evident as the wire length decreases, preventing EM failure because it prevents the formation of a void when it is shorter than the critical threshold length [94,95].

In a Cu damascene structure, the TaN/Ta barrier and the DB act as a boundary for the Cu, and this is where the depletion of metal atoms begins. As a result, Cu EM shifts into the voids through the nucleation, incubation, and growth phases [96]. The dimensions of the vias and metal determine the likelihood that the voids produced in this manner will affect the resistance. Therefore, early failure initiates near the via bottom, and late failure is observed as a void in the metal line.

EM testing is performed under high-current-density and high-temperature conditions to obtain a failure time for when the resistance increases experimentally. The failure time (t) is widely described using Black's equation [97]:

$$t = Aj^{-n} \exp\left(\frac{E_a}{kT}\right) \quad (4)$$

where j is the current density, E_a is the activation energy for diffusion, k is the Boltzmann constant, T is the temperature, A is a constant, and n is the current exponent, whose value is typically between 1 and 2.

The activation energy for diffusion depends on the specific metal atoms involved and the diffusion path. Table 2 summarizes the activation energy for Al and Cu, with the diffusion paths divided into bulk, GB, interface, and surface. It is expected that the lower the activation energy, the faster the failure time detection will be.

Table 2. Activation energy for different diffusion paths for Al, Al/Cu, and Cu metal [12].

Metal	Activation Energy for Different Diffusion Paths (Ev)			
	Bulk	Grain Boundary	Surface	Interface
Al	1.4	0.4~0.5	NA	–
Al/Cu (Alloy)	1.2	0.6~0.7	NA	0.9~1.1
Cu	2.1	1.1~1.2	0.6~0.7	0.8~1.3

GB diffusion is the fastest path for Al, while surface diffusion is the fastest path for Cu due to the low activation energy. Therefore, to improve the EM lifetime, it is necessary to improve the paths with the lowest activation energy. For example, for Cu, the surface and interface should be improved first. For the surface diffusion path, strengthening the adhesion between Cu and the DB is the most important goal, with HN_3 plasma employed to remove Cu oxidation. CoWP [98] is then added, along with a Co cap [42,99] to maintain EM performance and meet the higher current density requirements of advanced technology generations. Similarly, at the interface, there is an adhesion issue between the liner and Cu. Therefore, EM improvement must be verified when evaluating new materials such as Co and Ru liners and reducing barrier/liner thickness [46,47,57–59,75]. For the GBs, the lower the metal width, the more difficult it is to improve the EM because the grain growth is limited by the metal width. However, it has been reported that the grain size increases with a longer annealing time when Cu reflowing is employed, although the result is not yet clear [48]. Finally, there is a method of improving EM by depositing doping impurities together with the seed Cu. Various metals (e.g., Al, Ag, Mn, Mg, and Zr) have been tested in this respect, and Mn is currently the most commonly used. However, the resistance increases as the doping concentration increases, so optimizing EM and resistance are required.

5.2. Time-Dependent Dielectric Breakdown

When long-term stress is applied in a strong electric field, electrical damage occurs to the dielectric material, and insulation is lost, ultimately leading to TDDB [100]. This TDDB has been treated as an essential reliability item in the gate oxide. In the past BEOL interconnects, the size of the electric field applied to the insulator did not become a problem because of the excellent insulation characteristics of SiO_2 and sufficient gaps between wirings. However, as scaling progressed, the size of the electric field across the dielectric gradually increased, and porous low-k materials were introduced, leading to TDDB becoming an essential measure of reliability for BEOL interconnects [101]. The breakdown strength of a porous low-k material decreases as the dielectric constant decreases.

The pores in a porous low-k material shorten the percolation paths, weaken the bonds at the metal−insulator interface, and have a high trap density. The interface between the low-k material and the DB is the most problematic in this respect because of the possibility of a high trap density due to CMP, bond mismatches due to material differences, and the shorter distances arising from a tapered morphology [102]. In addition, a breakdown current may be generated by the defects in the porous low-k material in its as-deposited state or following plasma damage received during the fabrication process such as RIE etch.

In addition to these intrinsic causes, Cu metallization also affects TDDB. Cu diffusion into the dielectric may occur through the metal barrier and DB. Thus, TDDB should be evaluated when applying a change in the characteristics or thickness of a new barrier material. Since the TDDB test is performed at a deliberately high acceleration voltage, a TDDB lifetime model is required for predicting the actual lifetime at the standard operating voltage from the TDDB measurement results. E and $E^{1/2}$ models are widely used as standards for TDDB reliability testing, which is important because they are the most conservative predictors of low-k TDDB [103]. Of these, the $E^{1/2}$ model is most capable of explaining low-k TDDB behavior due to Cu diffusion.

6. Summary

Because introducing a new dielectric material with a lower *k* value to microchip interconnects is likely to prove difficult, efforts to suppress the increase in RC delay due to scaling have concentrated on the metallization process. Furthermore, more innovative approaches to metallization are required when the minimum metal pitch required by the process node is less than 40 nm (10 nm technology or lower).

These innovative approaches, as mentioned earlier, are traditionally moving toward implementing a barrier-less method by introducing new materials from an approach that reduces the thickness of the barrier/liner. Moreover, in recent years, due to the limitations of Cu damascene structures, subtractive etching has been employed as a process option. However, no single metallization approach can satisfy all BEOL interconnect levels simultaneously. Therefore, depending on the purpose of each level, maximum chip performance can be achieved by selectively employing the various metallization options.

As the scaling of interconnects continues, it is doubtful that current metallization approaches will continue to satisfy the requirements for minimizing the RC delay. As in the case of low-k materials, it may no longer be practical to pursue the scaling of metallization. Rather, the innovative approaches proposed to date can contribute to scaling requirements not through direct scaling but with architectural innovations such as super vias and buried power rails.

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