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A Nonisolated Transformerless High-Gain DC–DC Converter for Renewable Energy Applications

Mohammad Zaid [1], Ifham H. Malick [1], Imtiaz Ashraf [1], Mohd Tariq [1,*], Basem Alamri [2] and Eduardo M. G. Rodrigues [3,4,*]

[1] Department of Electrical Engineering, ZHCET, Aligarh Muslim University, Aligarh 202002, India; zaidahmadzhcet@gmail.com (M.Z.); ifhmal@gmail.com (I.H.M.); iashrafamu@gmail.com (I.A.)
[2] Department of Electrical Engineering, College of Engineering, Taif University, P.O. Box 11099, Taif 21944, Saudi Arabia; b.alamri@tu.edu.sa
[3] INESC-ID, Sustainable Power Systems Group, Av. Rovisco Pais 1, 1049-001 Lisboa, Portugal
[4] Instituto Superior Tecnico, University of Lisbon, Av. Rovisco Pais 1, 1049-001 Lisboa, Portugal
* Correspondence: tariq.ee@zhcet.ac.in (M.T.); eduardo.g.rodrigues@tecnico.ulisboa.pt (E.M.G.R.)

Abstract: Dc–dc converters with a high gain, continuous input current, and common ground are usually employed in renewable energy applications to boost the generated output voltage of renewable energy sources. In this paper, a high-gain dc–dc converter comprising a voltage multiplier cell (VMC) and a common ground with continuous input current and low-voltage stress across semiconductor devices is proposed. The converter produces a voltage gain of about ten times compared to the conventional boost converter at a duty ratio of 50% by utilizing switched capacitors and switched inductors. The simultaneous operation of both the switches with the same gate pulse offers easy and simple control of the proposed converter with a wide range of operations. The boundary operation of the converter is analyzed and presented in both modes, i.e., continuous conduction mode (CCM) and discontinuous conduction mode (DCM). Ideal and nonideal analysis of the converter is carried out by integrating real models of passive elements and semiconductor devices by using PLECS software. The simulation is also used to calculate the losses and hence the working efficiency of the converter. The performance of the converter analyzed in the steady state is compared with various similar converters based on the voltage boosting capability and switching stresses. A hardware prototype is also developed to confirm and validate the theoretical analysis and simulation of the proposed converter.

Keywords: dc–dc converter; high gain; low-voltage stress; voltage multiplier cell; nonisolated converter

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1. Introduction

High-gain boost converters have gained prominence in recent times due to their suitability in various applications such as solar PV systems [1], switch-mode power supplies (SMPS), electric vehicles, and aerospace applications. A conventional boost converter has certain shortcomings such as discontinuous input and output currents and increased losses in the system at higher duty cycle operations, which leads to its limited solar PV and fuel cell applications. The traditional quadratic boost converter (TQBC) shown in Figure 1 uses a single switch of high voltage and a current rating which results in low efficiency at higher duty ratios. In the literature, many high-gain dc–dc converters are being published [2,3] to overcome the limitations of the conventional boost and quadratic boost converter. The use of coupled inductors, Z-source converters, switched inductors, switched capacitors, and voltage multiplier cells (VMCs) are popular methods to increase the gain of high-gain dc–dc converters.

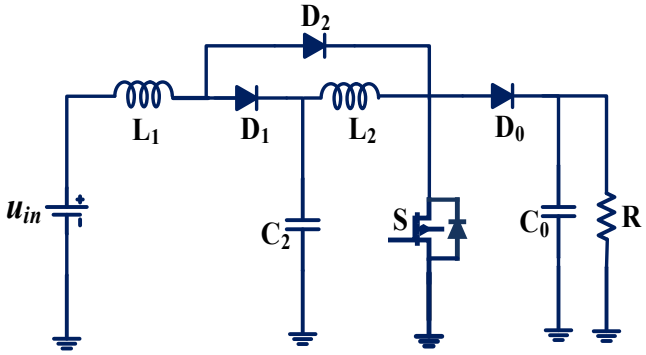


Figure 1. A traditional quadratic boost converter (TQBC).

Isolated step-up quadratic boost converters are implemented in [4,5] with coupled inductors that have a high-voltage gain and low switching stress. The converter in [4] has a voltage doubler cell and produces a higher gain as compared to [5]. Soft switched dc–dc converters eliminate the switching losses [6,7] however their hardware implementation and operation are difficult. Various Z-source converters [8–11] have been proposed in the literature that contains a unique impedance network. In [10], a quasi-Z source converter is implemented using a switched capacitor and switched inductor configuration for achieving a high-voltage gain along with low-voltage stress on capacitors and a continuous input current, but the topology lacks a common ground. In [11], the hybrid quasi-Z source converter is proposed by a combination of traditional Z source converters.

A set of nonisolated switched inductors and switched capacitor converters are discussed in [12–17]. The converter proposed in [12] has a switched capacitor and quadratic gain with a common ground and low input current ripples. The converter is lightweight due to the absence of a transformer and can be utilized for solar PV applications. In [13], the authors have proposed a switched inductor boost converter that has low current stress in inductors but suffers from a low-voltage gain and high-switch stresses. In [14], the twin duty cycle and three switches configuration add to the complexity of the circuit [14,15] as compared to [16] which has two switches following the same duty cycle. A non-isolated converter is proposed in [17] and has a simple design as compared to [15,16] along with a high gain and reduced voltage stresses on switches, diodes, and capacitors. It has a symmetrical structure that helps to ease the choice of the components and its design. In [18], a single switch nonisolated topology is implemented with low switch stress. In [19], the transformerless converter shown in Figure 2 is proposed. It consists of a VMC, with a gain of six times that of a conventional boost converter with a single switch and two inductors. The converter shown in Figure 2 has a single switch but the converter lacks a common ground. Moreover, the input current pulsates. The converter proposed in this paper has a common ground and continuous input current.

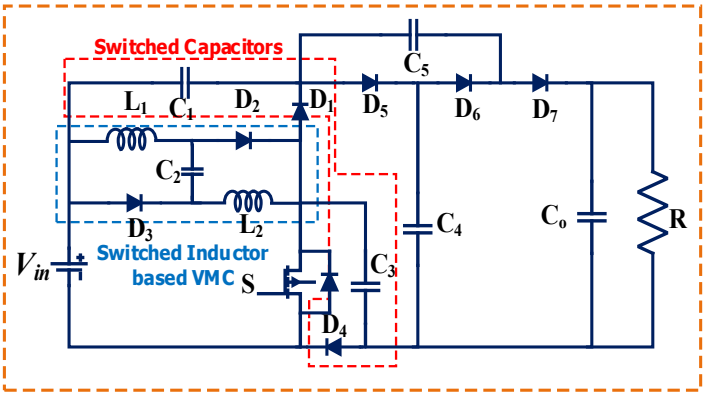


Figure 2. Converter proposed in [19].

In [20], a modified Ćuk converter is proposed with switched capacitors. The authors have proposed a buck-boost converter in [21] for renewable energy applications with continuous input. The converter exhibits high efficiency above 95% around the 56.5% duty cycle; however, the switching stress also increases drastically. In [22], an extendable boost converter employing active-passive inductor cells (APIC) is proposed. The efficiency and voltage gain at a lower duty ratio decrease drastically as the number of APICs is increased. The authors in [23] have introduced an extended boost converter by implanting a cell consisting of switched capacitors and inductors between a conventional boost converter. The converter has the same voltage gain for the complementary duty ratio, which is nearly constant, while the duty ratio is varied from 30% to 70%. A quadratic boost converter is proposed in [24]. The gain of the converter is lower as compared to similar topologies. A variety of quadratic boost converters are introduced in [25–30], each with its set of advantages and disadvantages. The authors in [25] have proposed a simple quadratic boost converter, but it lacks a common ground, whereas a modified quadratic boost converter in [26] is implemented, resulting in twice the gain as compared to the quadratic boost converter. The converter proposed in [27] has a common ground but a lower gain as compared to the topology proposed in [28], which lacks a common ground. The quadratic converter proposed by the authors in [29] has more components as compared to [30] but has a higher gain at the cost of a decreased efficiency due to increased heat losses.

In this paper, a new transformerless high-gain dc–dc converter is implemented that employs a VMC to boost the voltage. The attractive features of the proposed topology are

- The converter achieves a high gain of 10 times the conventional boost and 5 times that of the quadratic boost converter at a 50% duty ratio.
- The converter has low voltage stress of 5% of the output voltage across switch S_1.
- The converter uses the same gate signal for both switches, which leads to its easy operation.
- The topology has a continuous input current and a common ground, making it feasible for PV applications.

The paper discusses the structure of the proposed topology and its detailed ideal analysis in Section 2 followed by the nonideal analysis in Section 3. The comparison of the proposed topology with various similar converters is carried out in Section 4. The simulation and the experimental results are presented in Section 5 along with the efficiency of the proposed converter at different input voltages and power.

2. Structure of Proposed High-Gain DC–DC Converter Topology

The components of the proposed nonisolated dc–dc converter topology depicted in Figure 3 consist of a fixed DC input voltage source V_{in}; two switches (MOSFETs) S_1 and S_2; three inductors L_1, L_2, and L_3; seven diodes D_1, D_2, D_3, D_4, D_5, D_6, and D_O; five capacitors C_1, C_2, C_3, C_4, and C_O; and a resistive load R_O with an output voltage of V_O. The circuit also consists of a VMC with elements L_2, L_3, C_4, D_5, and D_6. The nonisolated converter does not include a high-frequency transformer and hence contributes to its low bulkiness, size, and cost reduction. This further aids in easier control of the topology as compared to isolated converters.

2.1. Operation of the Converter in Continuous Conduction Mode (CCM)

The proposed converter operates in two modes in each cycle while working in the CCM state. Each mode is discussed in detail by providing the voltage and current equations of each component in both modes.

Mode 1 ($0 \leq t \leq t_O$): In mode 1, both switches S_1 and S_2 are turned ON simultaneously, as shown in Figure 4, by applying the appropriate gate pulse. In this mode, diodes D_2, D_4, D_5, and D_6 are forward-biased, whereas the other diodes D_1, D_3, and D_O are reverse-biased. The inductor L_1 is charged through the input voltage source and the inductors L_2 and L_3 are charged through the capacitor C_3. The capacitor C_3 is discharged,

while the capacitor C_5 is charged in this mode. The output capacitor C_O discharges and feeds the load to maintain a constant voltage V_O across the output load resistor.

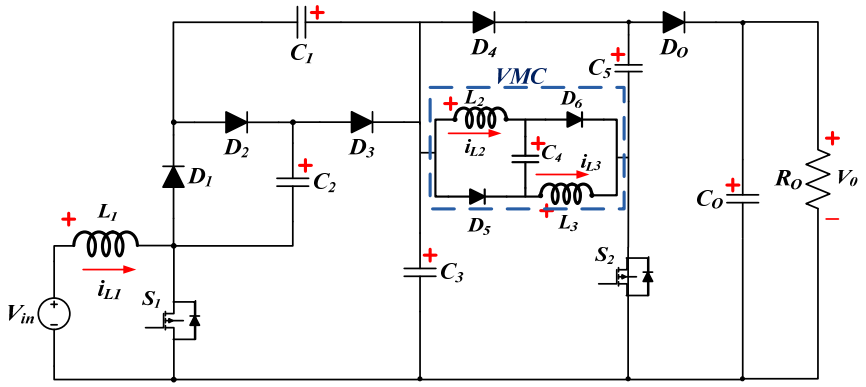


Figure 3. Proposed high-gain dc–dc converter topology.

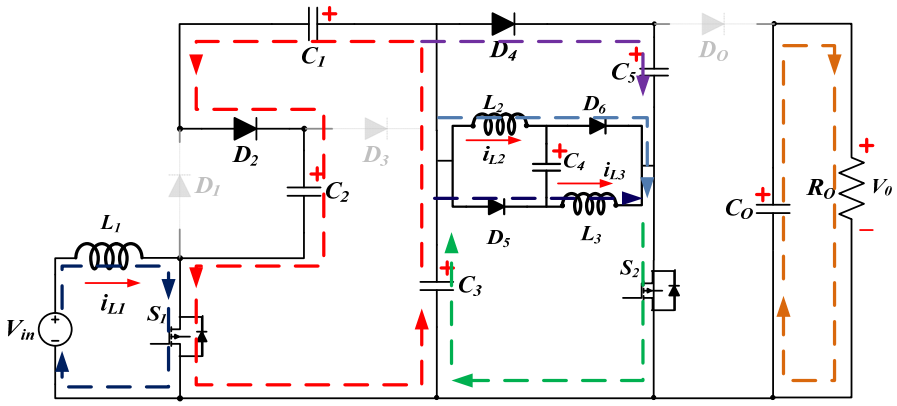


Figure 4. Conduction diagram of the converter in ON-state (Mode 1).

The voltage and current equations across the inductors and capacitors during mode 1 when both switches are ON can be expressed as (1) and (2), respectively.

$$\begin{cases} V_{L1} = V_{in} \\ V_{C0} = V_0 \\ V_{C3} = V_{C1} + V_{C2} \\ V_{L2} = V_{L3} = V_{C3} = V_{C5} = -V_{C4} \end{cases} \tag{1}$$

$$\begin{cases} I_{L_1} = I_{in} \\ I_{C1} = I_{C2} = I_{D2} = I_{S1} - I_{in} \\ I_{S_2} = I_{in} + i_{C3} - I_{s1} = I_{C3} - I_{C1} \\ I_{D4} = I_{C5} \\ I_{CO} = I_O \\ I_{C4} = I_{L2} \end{cases} \tag{2}$$

Mode 2 ($t_O \leq t \leq T$): In mode 2, both switches S_1 and S_2 are turned OFF simultaneously. In Figure 5, it can be seen that diodes D_1, D_3 and D_O are forward-biased, whereas the remainder of diodes D_2, D_4, D_5 and D_6 are reverse-biased. In this mode capacitor, C_3 is charged through capacitors C_1 and C_2. Inductors L_2 and L_3 along with capacitor C_4 transfer power to load and charge, and capacitor C_O maintains a constant voltage V_O about the

load. The voltage and current equations across the inductors and capacitors during Mode 2 when both switches are OFF can be expressed as (3) and (4), respectively.

$$\begin{cases} V_{C1} = V_{C2} \\ V_{L1} = V_{in} + V_{C1} - V_{C3} = V_{in} - V_{C1} \\ V_{C0} = V_0 \\ V_{C3} = V_{L2} + V_{L3} + V_{C4} - V_{C5} + V_{Co} = V_{L2} + V_{L3} + V_{C4} - V_{C5} + V_O \\ V_{L2} = V_{L3} = \frac{1}{2}(3\,V_{C3} - V_0) \end{cases} \tag{3}$$

$$\begin{cases} I_{C1} = I_{C2} = I_{D1} = I_{D2} = \frac{-I_{in}}{2} \\ I_{C4} = I_{C5} = I_{Do} = I_{in} + I_{C3} \\ I_{C0} = I_0 - I_{in} - I_{C3} \\ I_{L2} = I_{C4} \end{cases} \tag{4}$$

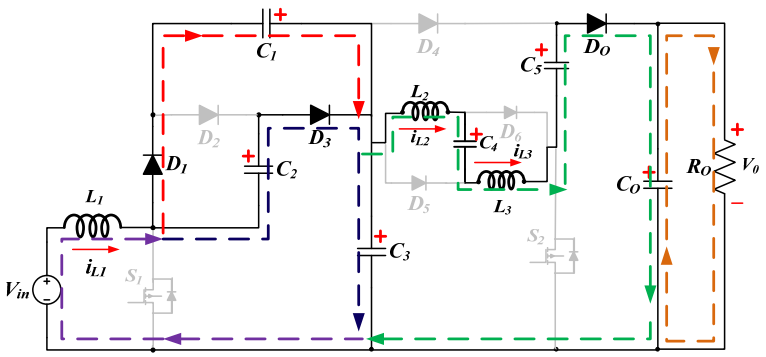


Figure 5. Conduction diagram of the proposed converter in OFF state (Mode 2).

The ideal voltage gain (M) can be calculated by using the volt-sec balance principle in an inductor in CCM operation as per the following relation given in (5),

$$\frac{1}{T}\left(\int_0^{DT} V_{LON}dt + \int_{DT}^{T} V_{LOFF}dt\right) = 0 \tag{5}$$

Applying the volt-sec principle in the inductor L_1

$$\begin{cases} \frac{1}{T}\left(\int_0^{DT} V_{in}dt + \int_{DT}^{T} (V_{in} - V_{C1})dt\right) = 0 \\ V_{C1} = V_{C2} = \frac{V_{in}}{(1-D)} = \frac{V_{C3}}{2} \end{cases} \tag{6}$$

Applying the volt-sec balance principle to L_2

$$\begin{cases} \frac{1}{T}\left(\int_0^{DT} V_{C3}dt + \int_{DT}^{T} \frac{(3V_{C3} - V_O)}{2}dt\right) = 0 \\ V_{C3} = 2V_{C1} = \frac{(1-D)V_O}{(3-D)} \end{cases} \tag{7}$$

Equating Equations (6) and (7)

$$M_{CCM} = \frac{V_0}{V_{in}} = \frac{2(3-D)}{(1-D)^2} \tag{8}$$

where 'D' denotes the duty cycle for switches S_1 and S_2.

The voltages across the capacitors and inductors (shown in Figure 6) are represented in (9) and can be easily evaluated by applying KVL in respective loops as,

$$\begin{cases} V_{C1} = V_{C2} = \frac{(1-D)V_O}{2(3-D)} \\ V_{C3} = 2V_{C1} = \frac{(1-D)V_O}{(3-D)} \\ V_{C4} = -V_{C5} = -V_{C3} = \frac{-(1-D)V_O}{(3-D)} \\ V_{C0} = V_0 \\ V_{L1_{OFF}} = \frac{(-D)V_{in}}{(1-D)} = \frac{-D(1-D)V_O}{2(3-D)} \\ V_{L2_{OFF}} = V_{L3_{OFF}} = \frac{-(1+D)V_{in}}{2(3-D)} = \frac{-(1+D)V_O}{(1-D)^2} \end{cases} \quad (9)$$

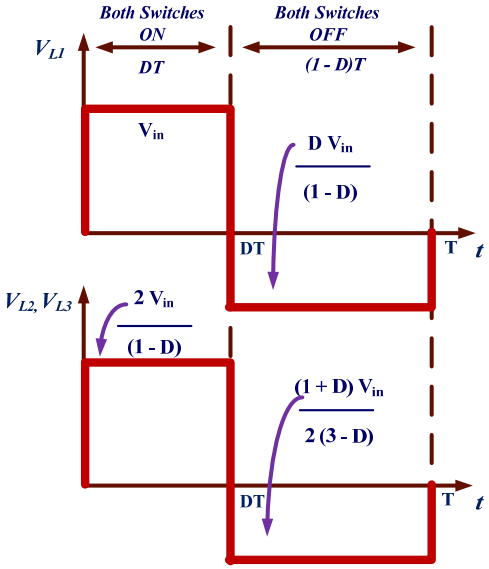


Figure 6. Inductor voltages.

2.1.1. Calculation of Voltage Stress

The voltage stress across the switches as shown in Figure 7 and the diodes shown in Figures 8 and 9 are evaluated at the instance when the switches are not conducting and are in the OFF state. The voltage stress particularly refers to the peak inverse voltage across the switch.

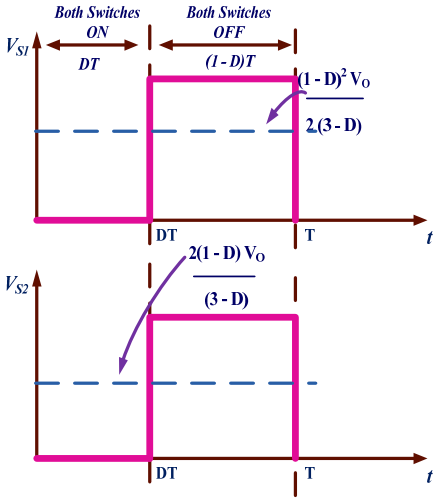


Figure 7. Switch voltages.

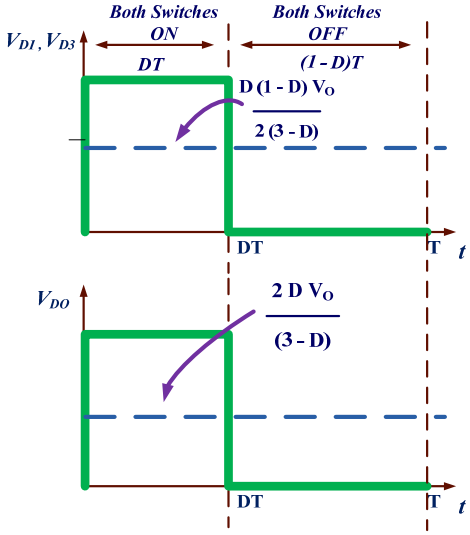


Figure 8. Diode voltages.

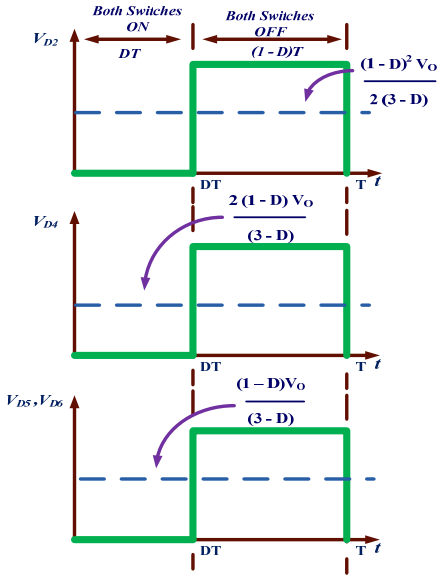


Figure 9. Diode voltages.

The voltage stresses across the switches in the OFF state are given as,

$$\begin{cases} V_{S1} = (1-D)V_{C1} = \frac{(1-D)^2 V_o}{2(3-D)} \\ V_{S2} = (1-D)(V_{C5} - V_o) = \frac{-2(1-D)\ V_o}{(3-D)} \end{cases} \tag{10}$$

The voltage stress across different diodes when they are not conducting can be expressed as in (11):

$$\begin{cases} V_{D1} = V_{D3} = D\ V_{C1} = \frac{D(1-D)V_o}{2(3-D)} \\ V_{D2} = (1-D)V_{C1} = \frac{(1-D)^2 V_o}{2(3-D)} \\ V_{D4} = (1-D)(V_{C3} - V_0) = \frac{-2(1-D)\ V_o}{(3-D)} \\ V_{D5} = V_{D6} = \frac{-(1-D)V_o}{(3-D)} \\ V_{D0} = \frac{-2D\ V_o}{(3-D)} \end{cases} \tag{11}$$

2.1.2. Calculation of Average and RMS Currents

The average currents through the capacitors and switches can be easily determined by applying the current-sec balance principle in capacitors.

$$\frac{1}{T}\left(\int_{0}^{DT} I_{C_{ON}}dt + \int_{DT}^{T} I_{C_{OFF}}dt\right) = 0. \tag{12}$$

The average switch currents (in Figure 10) are given as,

$$\begin{cases} I_{S1_{avg}} = I_{L1} - I_{D1} = \frac{(3-D)(1+D)i_o}{D(1-D)^2} \\ I_{S2_{avg}} = 2I_{L2} = \frac{2i_o}{(1-D)} \end{cases} \tag{13}$$

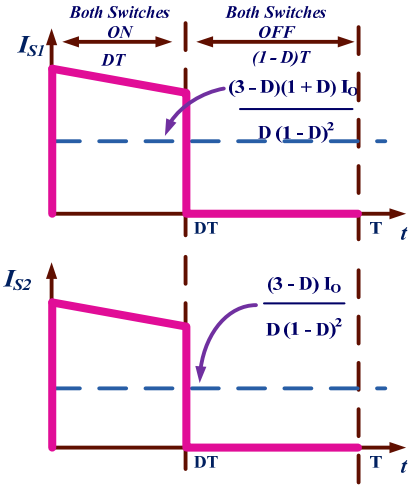


Figure 10. Switch currents.

The average inductor currents (in Figure 11) are given as,

$$\begin{cases} i_{L2_{avg}} = i_{L3_{avg}} = \frac{i_o}{(1-D)} \\ i_{DO_{avg}} = i_{D4_{avg}} = i_o \\ i_{L1_{avg}} = i_{in} = \frac{2(3-D)i_o}{(1-D)^2} \\ i_{D5_{avg}} = i_{D6_{avg}} = 2i_{L2_{avg}} = \frac{2i_o}{(1-D)} \\ i_{D1_{avg}} = i_{D2_{avg}} = i_{D3_{avg}} = \frac{(3-D)i_o}{D(1-D)} \end{cases} \tag{14}$$

The RMS values of the switch currents are given as,

$$\begin{cases} i_{S1_{rms}} = \frac{(3-D)(1+D)i_o}{D\sqrt{D}(1-D)^2} \\ i_{S2_{rms}} = \frac{2i_o}{\sqrt{D}(1-D)} \end{cases} \tag{15}$$

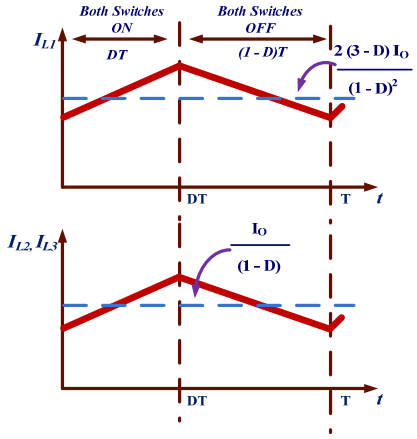


Figure 11. Inductor currents.

The RMS values of the various currents through the components are given as,

$$\begin{cases} i_{L2_{rms}} = i_{L3_{rms}} = \frac{i_o}{(1-D)} \\ i_{DO_{rms}} = i_{D4_{rms}} = \frac{i_o}{\sqrt{D}} \\ i_{L1_{rms}} = i_{in} = \frac{2(3-D)i_o}{(1-D)^2} \\ i_{D5_{rms}} = i_{D6_{rms}} = 2i_{L2_{rms}} = \frac{2i_{io}}{\sqrt{D}(1-D)} \\ i_{D1_{rms}} = i_{D2_{rms}} = i_{D3_{rms}} = \frac{(3-D)i_O}{D\sqrt{D}(1-D)} \\ i_{C1_{rms}} = i_{C2_{rms}} = \frac{3-D}{(1-D)^2}\sqrt{\frac{1-D}{D}}i_o \\ i_{CO_{rms}} = \sqrt{\frac{D}{1-D}}i_o \\ i_{C3_{rms}} = \frac{(5-D)}{(1-D)\sqrt{D\ (1-D)}}i_o \\ i_{C5_{rms}} = i_{C4_{rms}} = \frac{1}{\sqrt{D\ (1-D)}}i_o \end{cases} \quad (16)$$

2.1.3. Design of Inductors and Capacitors

The ripple current in the inductor L_1 can be found as in (17) and rearranged to obtain the critical value of the inductor for CCM operation.

$$\begin{cases} (\Delta i_{L1})_{ON} = \frac{V_{in}}{L_1}DT \\ L_{1_{Cri}} = \frac{V_{in}}{(\Delta i_{L1})_{ON}f_s}D = \frac{D(1-D)^2\ V_O}{2(3-D)\Delta i_{L1}f_s} \end{cases} \quad (17)$$

The ripple current and the critical value of the inductors L_2 and L_3 can be found as

$$\begin{cases} (\Delta i_{L2})_{ON} = \frac{V_{C3}}{L_2}(1-D)T \\ L_{2_{Cri}} = L_{3_{Cri}} = \frac{D(1-D)V_O}{(3-D)\Delta i_{L2}f_s} \end{cases} \quad (18)$$

The peak-to-peak ripple voltages across the capacitors can be given as

$$\begin{cases} \Delta V_{c1} = \Delta V_{c2} = \frac{(3-D)V_0}{(1-D)R_OC_1f_s} \\ \Delta V_{c3} = \frac{(5-D)V_0}{(1-D)R_OC_3f_s} \\ \Delta V_{c4} = \Delta V_{c5} = \frac{V_0}{R_OC_4f_s} \\ \Delta V_{cO} = \frac{DV_0}{R_OC_Of_s} \end{cases} \quad (19)$$

2.2. Operation of Converter in Discontinuous Conduction Mode (DCM)

The proposed converter can also operate in DCM. This mode consists of three different sub-modes of operation, as depicted in Figure 12.

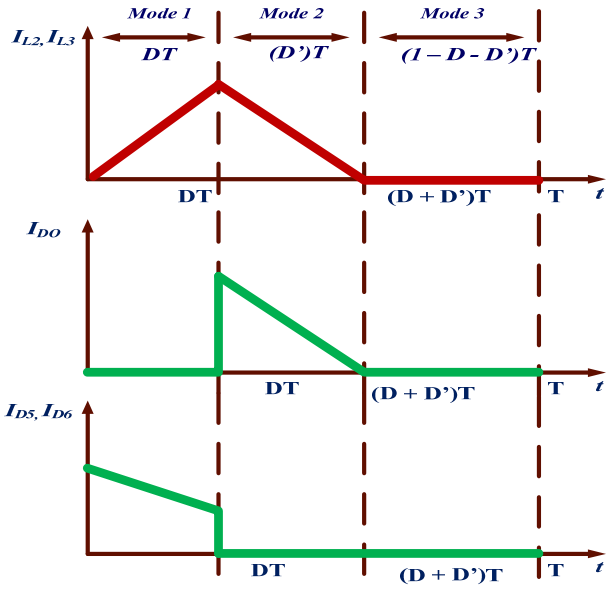


Figure 12. Typical waveforms during DCM.

(i) ***Mode 1***: In this mode, both switches are turned ON for duty cycle D as in the case of CCM.

(ii) ***Mode 2***: In this mode, both switches are turned OFF and the inductors start discharging. The inductors discharge through diodes D_1, D_3, and D_O for a duty cycle D′ and the mode ends at D + D′.

(iii) ***Mode 3***: In this mode, none of the switches or diodes conduct, and the load is fed entirely through the output capacitor C_O. The mode is operated for a duration of 1 − D − D′.

The inductors are charged in Mode 1 (from t = 0 to t = DT) and are discharged in Mode 2 (from t = DT to t = D′T). Hence, by applying volt-sec balance across the inductors, we obtain the voltage gain in DCM.

Applying volt-sec balance in inductor L_1, we obtain,

$$V_{c1} = \frac{(D + D')V_{in}}{D'^2} \tag{20}$$

Applying volt-sec in L_2, we obtain,

$$V_{c1} = \frac{D'V_O}{2(2D + 3D')} \tag{21}$$

From Equating (20) and (21), we obtain,

$$M_{DCM} = \frac{V_O}{V_{in}} = \frac{2(D + D')(2D + 3D')}{D'^2} \tag{22}$$

Rearranging Equation (22), we obtain,

$$D' = \frac{\sqrt{D^2 + 4M_{DCM}} - 5D}{6 - M_{DCM}} \tag{23}$$

Under DCM analysis for inductor L_2, we have,

$$\begin{cases} V_{L2} = L_2 \frac{\Delta i_{L2}}{DT} \\ \Delta i_{L2} = \frac{V_O D' DT}{L_2(2D+3D')} \end{cases} \quad (24)$$

For DCM operation,

$$I_{L2} = \frac{\Delta i_{L2}}{2} = I_O \quad (25)$$

From (24) and (25) we obtain,

$$D' = \frac{4\tau f_s D}{D - 6\tau f_s} \quad (26)$$

where τ is the time constant represented as $\frac{L_2}{R_O}$ and f_s is the switching frequency of the switches.

Equating (25) and (26), we obtain,

$$M_{DCM} = \frac{D(D - 2\tau f_s)}{4\left(\tau f_s\right)^2} \quad (27)$$

Let $K_e = \tau f_s$; then,

$$M_{DCM} = \frac{D(D - 2K_e)}{4\left(K_e\right)^2}. \quad (28)$$

2.3. Converter Operation at Boundary Conditions

The boundary condition represents the critical conduction state of the converter on the boundary of DCM and CCM. The relation for the boundary condition can be easily formulated by equating the voltage gains in the CCM and DCM operations, respectively. The boundary condition is determined by the boundary-normalized time constant of the inductor L_2, is as shown in Figure 13. The variation in the time constant of the inductor as a function of the duty cycle is represented as

$$K_{ec} = \frac{D(1-D)}{8(3-D)}\left(D + \sqrt{25 - 8D} - 1\right) \quad (29)$$

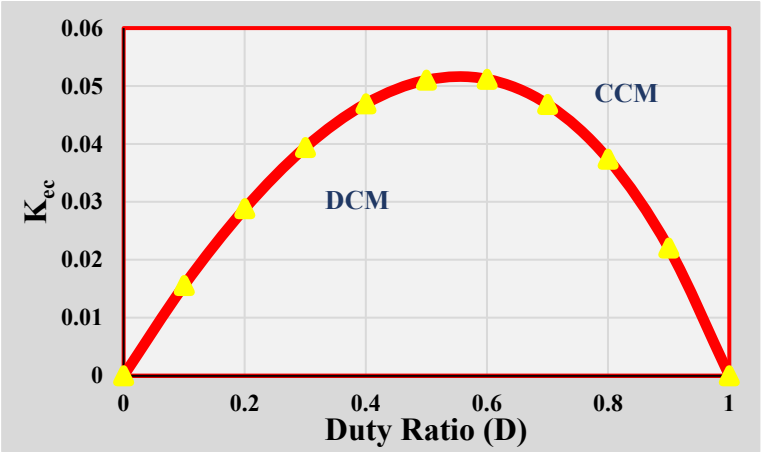


Figure 13. Boundary normalized inductor time constant versus the duty ratio.

The maximum value of K_{ec} is 0.00516 obtained at D = 0.55. The converter operates in DCM mode for a time constant less than K_{ec} and in CCM mode for a time constant more than K_{ec}.

3. Nonideal Analysis

The nonideal analysis of the converter accounts for the power loss analysis of the circuit. Thus far, only the ideal lossless analysis of the converter is being considered in the paper, ignoring the parasitic series resistances of the inductors, equivalent series resistance (ESR) of the capacitors, barrier potential voltage and leakage resistances of the diode, and the ON-state resistance of the switches (MOSFET), as shown in Figure 14. The loss analysis is proceeded by the inclusion of the above-mentioned parameters in the ideal circuit of the proposed topology. The nonidealities of the elements tend to decrease the voltage gain of the converter and also result in an increase in power losses. The total power loss across all the elements is given as,

$$P_{loss_{total}} = \sum_{i=1}^{2} P_{Si_{loss}} + \sum_{i=0}^{6} P_{Di_{loss}} + \sum_{i=0}^{5} P_{Ci_{loss}} + \sum_{i=1}^{3} P_{Li_{loss}} \tag{30}$$

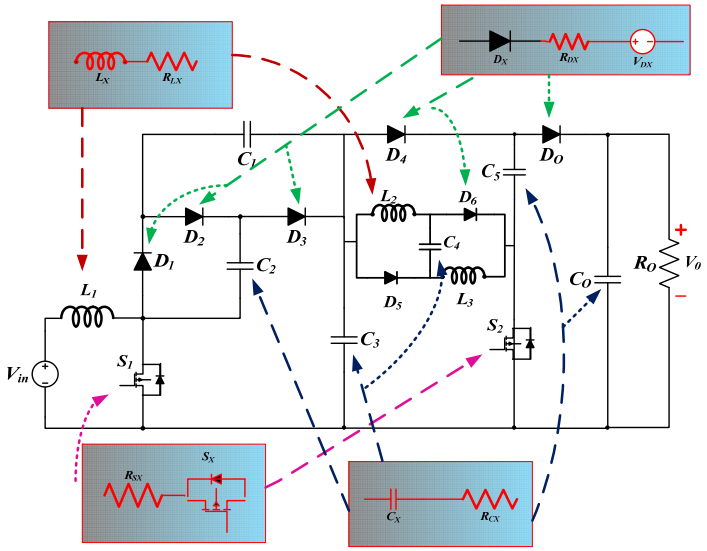


Figure 14. Nonideal realization of the proposed topology.

3.1. Calculation of Losses across Switches

The losses across switches can be either conduction losses that are encountered when the switch is ON and current flows through it, or they may be switching losses that are encountered when the switch is in the transition from the ON state to OFF state or vice-versa.

$$P^{S}_{loss_{total}} = P^{S_{1,2}}_{loss_{conduction}} + P^{S_{1,2}}_{loss_{switching}} \tag{31}$$

For the conduction loss calculations, the resistance of both switches is assumed to be the same, i.e., $r_{S_1} = r_{S_2} = r_s$.

$$\begin{cases} P^{S_{1,2}}_{loss_{conduction}} = i^2_{S1_{rms}} r_{S1} + i^2_{S2_{rms}} r_{S2} \\ P^{S_{1,2}}_{loss_{conduction}} = \left(\frac{(3-D)(3+D)i_o}{D\sqrt{D(1-D)^2}}\right)^2 r_{S1} + \left(\frac{2i_o}{\sqrt{D(1-D)}}\right)^2 r_{S2} \\ P^{S_{1,2}}_{loss_{conduction}} = \frac{1}{(D)^3(1-D)^4}((3-D)^2(1+D)^2 + (D)^2(1-D)^2) P_O \frac{r_s}{R_O} \end{cases} \tag{32}$$

For the calculation of switching losses for a switch operating at a switching frequency of f_s, the rise time (t_r) and fall time (t_f) of the gate pulses are considered. Then, the switching losses can be given as,

$$\begin{cases} P_{loss_{switching}}^{S_{1,2}} = \left(\frac{t_r + t_f}{2}\right) \times \left(i_{S1_{avg}} V_{S1_{avg}} + i_{S2_{avg}} V_{S2_{avg}}\right) f_s \\ P_{loss_{switching}}^{S_{1,2}} = \left(\frac{t_r + t_f}{2}\right) \times \left(\frac{(3-D)(1+D) i_o}{D(3-D)^2} \times \frac{(1-D)V_o}{2(3-D)} + \frac{2i_o}{(1-D)} \times \frac{2V_o}{(3-D)}\right) \times f_s \\ P_{loss_{switching}}^{S_{1,2}} = \left(\frac{t_r + t_f}{2}\right) \times \left(\frac{3 + 2D - D^2}{2D(1-D)(3-D)}\right) P_O \times f_s \end{cases} \quad (33)$$

3.2. Calculation of Losses across Diodes

For the calculation purpose, the cut-in voltage and resistance of all diodes are assumed to be the same, i.e., $V_{DO} = V_{D1} = V_{D2} = V_{D3} = V_{D4} = V_{D5} = V_{D6} = V_D$ and $r_{DO} = r_{D1} = r_{D2} = r_{D3} = r_{D4} = r_{D5} = r_{D6} = r_D$. The losses across different diodes are given as:

$$\begin{cases} P_{DO_{loss}} = i_{DO_{avg}} V_{DO} + i_{DO_{rms}}^2 r_{DO} \\ P_{DO_{loss}} = i_o V_{DO} + \left(\frac{i_o}{\sqrt{D}}\right)^2 r_{DO} \\ P_{DO_{loss}} = \frac{V_D}{V_O} P_o + \left(\frac{1}{\sqrt{D}}\right)^2 \frac{r_D}{R_O} P_O \end{cases} \quad (34)$$

$$\begin{cases} P_{D1_{loss}} = i_{D1_{avg}} V_{D1} + i_{D1_{rms}}^2 r_{D1} \\ P_{D1_{loss}} = \frac{(3-D)}{D(1-D)} \frac{V_D}{V_O} P_o + \left(\frac{(3-D)}{D\sqrt{D}(1-D)}\right)^2 \frac{r_D}{R_O} P_O \end{cases} \quad (35)$$

$$\begin{cases} P_{D2_{loss}} = i_{D2_{avg}} V_{D2} + i_{D2_{rms}}^2 r_{D2} \\ P_{D2_{loss}} = \frac{(3-D)}{D(1-D)} \frac{V_D}{V_O} P_o + \left(\frac{(3-D)}{D\sqrt{D}(1-D)}\right)^2 \frac{r_D}{R_O} P_O \end{cases} \quad (36)$$

$$\begin{cases} P_{D3_{loss}} = i_{D3_{avg}} \times V_{D3} + i_{D3_{rms}}^2 \times r_{D3} \\ P_{D3_{loss}} = \frac{(3-D)}{D(1-D)} \frac{V_D}{V_O} P_o + \left(\frac{(3-D)}{D\sqrt{D}(1-D)}\right)^2 \frac{r_D}{R_O} P_O \end{cases} \quad (37)$$

$$\begin{cases} P_{D4_{loss}} = i_{D4_{avg}} V_{D4} + i_{D4_{rms}}^2 r_{D4} \\ P_{D4_{loss}} = \frac{V_D}{V_O} P_o + \left(\frac{1}{\sqrt{D}}\right)^2 \frac{r_D}{R_O} P_O \end{cases} \quad (38)$$

$$\begin{cases} P_{D5_{loss}} = i_{D5_{avg}} V_{D5} + i_{D5_{rms}}^2 r_{D5} \\ P_{D5_{loss}} = \frac{2}{(1-D)} \frac{V_D}{V_O} P_o + \left(\frac{2}{\sqrt{D}\ (1-D)}\right)^2 \frac{r_D}{R_O} P_O \end{cases} \quad (39)$$

$$\begin{cases} P_{D6_{loss}} = i_{D6_{avg}} V_{D6} + i_{D6_{rms}}^2 r_{D6} \\ P_{D6_{loss}} = \frac{2}{(1-D)} \frac{V_D}{V_O} P_o + \left(\frac{2}{\sqrt{D}\ (1-D)}\right)^2 \frac{r_D}{R_O} P_O \end{cases} \quad (40)$$

$$P_{D_{loss_{total}}} = P_{DO_{loss}} + P_{D1_{loss}} + P_{D2_{loss}} + P_{D3_{loss}} + P_{D4_{loss}} + P_{D5_{loss}} + P_{D6_{loss}} \quad (41)$$

3.3. Calculation of Losses across Capacitors

For the calculation of conduction loss in capacitors, the parasitic resistances of the capacitors r_{C1}, r_{C2}, r_{C3}, r_{C4}, and r_{C5} are assumed to be equal, while the resistance of the capacitor C_O is assumed to be r_{CO}

$$\begin{cases} P_{C_{loss_{total}}} = i_{CO_{rms}}^2 r_{CO} + i_{C1_{rms}}^2 r_{C1} + i_{C2_{rms}}^2 r_{C2} + i_{C3_{rms}}^2 r_{C3} + i_{C4_{rms}}^2 r_{C4} + i_{C5_{rms}}^2 r_{C5} \\ P_{C_{loss_{total}}} = \left(\sqrt{\frac{D}{1-D}}\right)^2 \frac{r_{CO}}{R_O} P_O + 2\left(\frac{3-D}{(1-D)^2}\sqrt{\frac{1-D}{D}}\right)^2 \frac{r_{C1}}{R_O} P_O + \\ \left(\frac{(5-D)}{(1-D)\sqrt{D\ (1-D)}}\right)^2 \frac{r_{C3}}{R_O} P_O + \left(\frac{1}{\sqrt{D\ (1-D)}}\right)^2 \frac{r_{C5}}{R_O} P_O \\ P_{C_{loss_{total}}} = \left(\frac{D}{(1-D)}\right) \frac{r_{CO}}{R_O} P_O + \left(\frac{44 - 24D + 4D^2}{D(1-D)^3}\right) \frac{r_C}{R_O} P_O \end{cases} \quad (42)$$

3.4. Calculation of Losses across Inductors

The loss calculations for inductors are carried out by ignoring the ripple in the inductor current through the leakage resistances r_{L1}, r_{L2}, and r_{L3}. Inductors L_2 and L_3 have the same design values; hence, their parasitic resistances are assumed to be equal.

$$\begin{cases} P_{L_{loss_{total}}} = i^2_{L1_{rms}} r_{L1} + i^2_{L2_{rms}} r_{L2} + i^2_{L3_{rms}} r_{L3} \\ P_{L_{loss_{total}}} = \left(\frac{2(3-D)}{(1-D)^2}\right)^2 \frac{r_{L1}}{R_O} P_O + 2\left(\frac{1}{(1-D)}\right)^2 \frac{r_{L2}}{R_O} P_O \end{cases} \tag{43}$$

3.5. Calculation of Efficiency of the Converter in Nonideal Mode

The efficiency of the converter is given as the ratio of the output power transferred to the total input power fed to the circuit, which can be represented as the sum of the output power and the total losses in the converter. The efficiency (η) is given as

$$\begin{cases} \eta = \frac{P_0}{P_0 + P_{S_{loss}} + P_{D_{loss}} + P_{C_{loss}} + P_{L_{loss}}} \\ \eta = \frac{1}{1 + \frac{P_{S_{loss}} + P_{D_{loss}} + P_{C_{loss}} + P_{L_{loss}}}{P_0}} = \frac{1}{1+K} \end{cases} \tag{44}$$

where K is a constant given simplified as,

$$\begin{cases} K = \left\{ \left[\frac{1}{D^3(1-D)^4} \left((3-D)^2(1+D)^2 + (D)^2(1-D)^2 \right) \frac{r_S}{R_O} \right] \right. \\ \qquad + \left[\frac{(2D+3)(3-D)}{D(1-D)} \frac{V_D}{V_O} \right. \\ \qquad \left. + \frac{27-18D+13D^2-4D^3+2D^4}{D^3(1-D)^2} \frac{r_D}{R_O} \right] \\ \qquad + \left[\frac{D}{1-D} \frac{r_{CO}}{R_O} + \frac{35-18D+3D^2}{D(1-D)^3} \frac{r_C}{R_O} \right] \\ \qquad \left. + \left[\left(\frac{2(3-D)}{(1-D)^2} \right)^2 \frac{r_{L1}}{R_O} + 2\left(\frac{1}{1-D} \right)^2 \frac{r_{L2}}{R_O} \right] \right\} \end{cases} \tag{45}$$

After substituting the value of K obtained in (45) in (44), we obtain,

$$\eta = \frac{D^3(1-D)^4}{D^3(1-D)^4 + \left[a\left(\frac{r_S}{R_O}\right) + b\left(\frac{r_D}{R_O}\right) + c\left(\frac{r_{CO}}{R_O}\right) + d\left(\frac{r_C}{R_O}\right) + e\left(\frac{r_{L1}}{R_O}\right) + f\left(\frac{r_{l2}}{R_O}\right) + g\left(\frac{V_D}{V_O}\right) \right]} \tag{46}$$

where,

$$\begin{cases} a = \left(9 + 12D - D^2 - 6D^3 + 2D^4\right) \\ b = \left(27 - 18D + 13D^2 - 4D^3 + 2D^4\right) \\ c = D^2(1-D)^4 \\ d = D(1-D)^2\left(35 - 18D + 3D^2\right) \\ e = 2D(3-D)^3 \\ f = 2D(1-D)^4 \\ g = D^3(1-D)^4(3-D)(2D+3) \end{cases} \tag{47}$$

3.6. Calculation of Nonideal Voltage Gain

For the derivation of nonideal voltage gain, all the lossy components of the elements such as the ON-state resistance of diodes and switches, ESRs of the inductor, and capacitor are considered for the analysis. Thus far, the input and output powers are equal due to lossless analysis, whereas, considering the above assumptions, the modified relation between the input and output power can be expressed as:

Input Power = Output Power + Losses across elements

3.7. Variation in Nonideal Voltage Gain

The nonideal gain (M_{actual}) of the proposed converter is derived as,

$$\begin{cases} M_{actual} = \frac{1}{1+K}(M_{CCM})_{ideal} = \eta(M_{CCM})_{ideal} \\ M_{\text{actual}} = \dfrac{\frac{2D^3(1-D)^2(3-D)}{D^3(1-D)^4+}}{\left(\left[a\left(\frac{r_S}{R_O}\right)+b\left(\frac{r_D}{R_O}\right)+c\left(\frac{r_{CO}}{R_O}\right)+d\left(\frac{r_C}{R_O}\right)+e\left(\frac{r_{L1}}{R_O}\right)+f\left(\frac{r_{L2}}{R_O}\right)+g\left(\frac{V_D}{V_O}\right)\right]\right)} \end{cases} \quad (48)$$

From the voltage gain comparison of ideal and nonideal voltage gains of the proposed topology in Figure 15, it is observed that both gains have similar values up to the duty ratio of 0.4, and then the nonideal gain increases until D = 0.7 but deviate from the ideal characteristics. Thereafter, it gradually decreases to zero at the unity duty ratio.

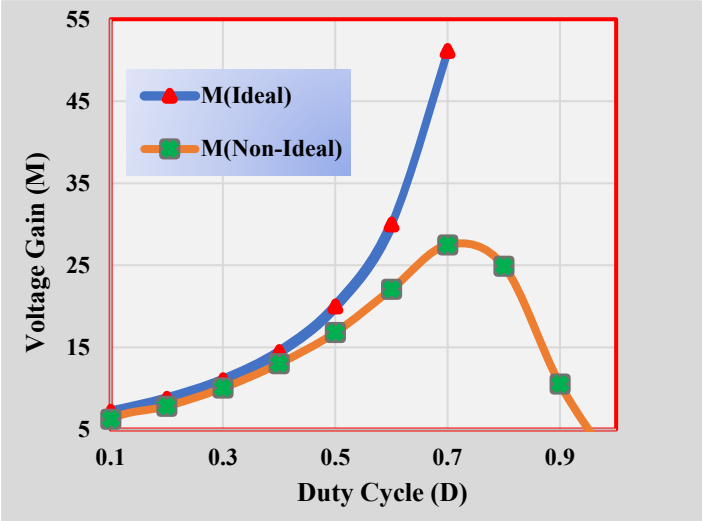


Figure 15. Comparison of calculated ideal and simulated nonideal voltage gain of the proposed converter.

The voltage gain of the converter can be affected by the parasitic resistances of different elements of the converter such as the parasitic resistance of inductors, capacitors, and switches. As the parasitic resistances of different elements increase, the voltage gain of the converter decreases gradually.

From Figure 16, it can be observed that, when the parasitic resistance of the switch is increased while other elements are kept ideal, the voltage gain of the converter decreases. For the parasitic resistance of 0.2% of the load resistance, the maximum gain is at the duty ratio of 0.7 with a gain of 24.18, while it decreases to 15.84 and 11.77 for 4% and 6% of the parasitic resistance, respectively, at D = 0.7.

From Figure 17, it can be observed that, when the parasitic resistance of the inductor is increased while other elements are kept ideal, the voltage gain of the converter decreases. For a parasitic resistance of 0.2% of the load resistance, the maximum gain is at the duty ratio of 0.75 with a gain close to 34, while it decreases to 24.88 and 19.80 for 4% and 6% of the parasitic resistance, respectively, at D = 0.7.

From Figure 18, it can be observed that, when the parasitic resistance of the capacitor is increased while other elements are kept ideal, the voltage gain of the converter decreases. For the parasitic resistance of 0.2% of the load resistance, the maximum gain is at the duty ratio of 0.8 with a gain of 63, while it decreases to around 41 and 21 for 4% and 6% of the parasitic resistance, respectively, at a near-duty ratio of 0.8.

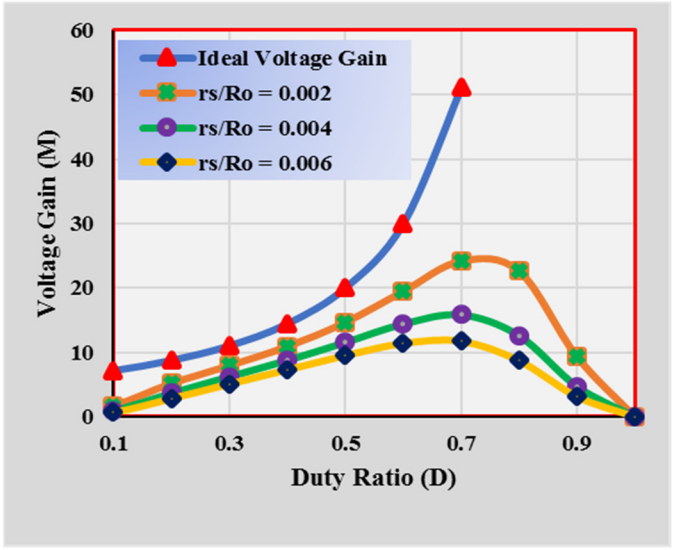


Figure 16. Voltage gain variation as per parasitic resistance of the switch.

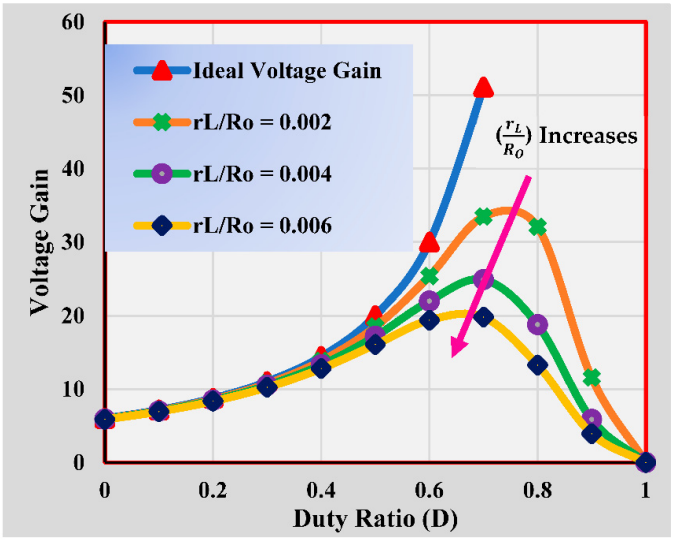


Figure 17. Voltage gain variation as per parasitic resistance of the inductor.

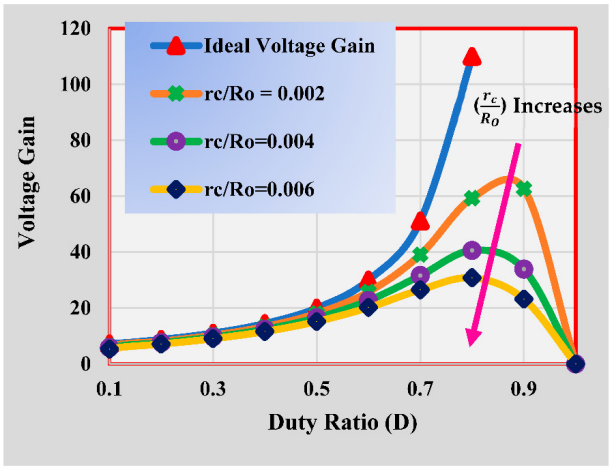
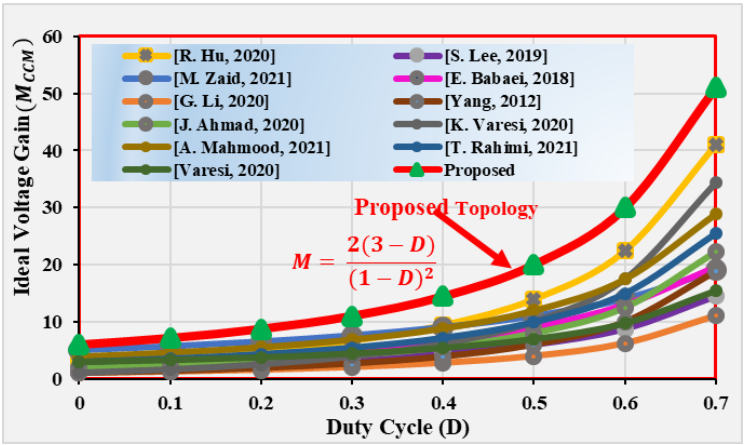


Figure 18. Voltage gain variation as per parasitic resistance of the capacitor.

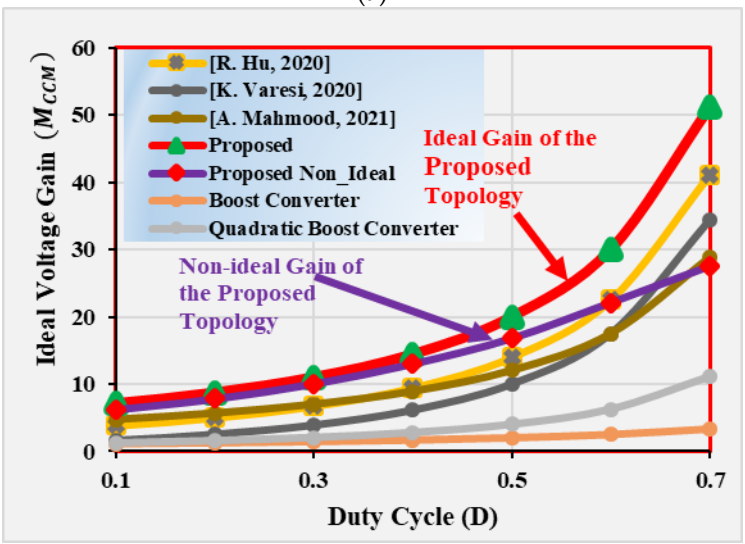
4. Comparison of the Proposed Topology

In this section, a comparison between the proposed topology with two traditional topologies and recent topologies is discussed. The topologies are compared based on their voltage gain (M_{CCM}), number of inductors (N_L), number of capacitors (N_C) and number of diodes (N_D) in the converter. The voltage stress appearing across the switches (V_{si}/V_{in}) is also compared along with the availability of common ground.

For the comparison of the topologies, the graph between the ideal voltage gain and the duty cycle is plotted in Figure 19a. Figure 19b depicts the comparison of the nonideal gain of the converter with the ideal gain of some selected topologies whose gain intersects the nonideal gain plot of the proposed topology. The voltage stress across the switches in the compared converters is shown in Figure 20.



(**a**)



(**b**)

Figure 19. (**a**) Comparison of ideal voltage gain of various similar converters [4,5,16,22,24–30]. (**b**) Comparison of various topologies with the nonideal voltage gain of proposed topology [4,24,27,28].

It can be observed from Figure 19a that the proposed topology has the highest ideal gain among all the high-gain boost converters compared to all converters. An ideal voltage gain of above 14 is achieved by the proposed topology at a duty ratio of 40% and a gain of 20 is achieved at a duty ratio of 50%. The proposed converter also has a higher nonideal gain, as shown in Figure 19b, as compared to the ideal gain of the similar topologies, as presented in Table 1, until the duty ratio of 60%. The switching stress of the converter is very low as compared to the traditional topologies. In converters [4,5], even with the presence of an isolation transformer/coupled inductor operating at a transformation ratio

of one, a lower gain than the proposed topology is produced, which works without a transformer or coupled inductor, hence reducing the overall cost of the topology.

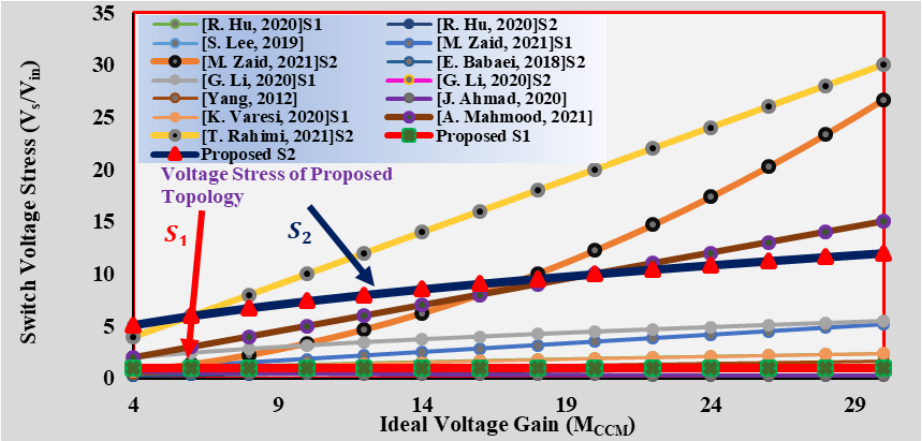


Figure 20. Comparison of calculated switch stress versus voltage gain [4,5,16,22,24–29].

For n = 1, the ideal gain of the converter in [4] when compared with the gain of the proposed converter is found to be half. Moreover, the voltage stress across the switch S_1 in [4] increases significantly as shown in Figure 20.

The topology proposed in [16] also has a VMC and two switches and produces a high gain at lower duty ratios with a lower number of components as compared with the proposed topology, but it decreases as the duty ratio is increased above 40%. The proposed converter despite having fewer inductors, switches and diodes than the converter [22] is capable of producing a much higher voltage gain. Although the switch stress across the converter [22] is very low as compared to the proposed one, the converter lacks a common ground that is available in the proposed topology. The converters in [24,25], despite having 2 and 3 inductors respectively and 2 switches which is the same as used in the proposed topology, produce a lower gain than the proposed topology and, concurrently, the voltage stress across the switch.

In the case of the topology shown in [25], the switch stress increases after a conversion gain ratio of 14. The converters in [26,27] also have three inductors but suffer from a low-voltage gain. The switch S_1 of [27] has high-voltage stress after a voltage gain of 8. The quadratic boost converter in [29] has the same inductors as the proposed converter, but the voltage gain is half as compared to the proposed converter, and it has a single switch only. The topology in [29] exhibits high-voltage stress across switch S_2 amongst all the compared topologies. The topology in [30] has the least voltage stress across its switches but suffers from a low ideal voltage gain, which is much lower than the nonideal voltage gain produced by the proposed converter.

From the comparison, it can be inferred that the topology has the highest voltage gain and the switch voltage gain across S_1 is very low. The switch voltage gain across the switch S_2 is found to be high for low-voltage gains, but it does not increase further as the voltage gain increases beyond 15. Hence, the proposed topology can be used at a voltage gain higher than 14, which is easily achieved at any duty ratio beyond 40%. Moreover, continuous input current and common ground are other advantages of the proposed converter.

Table 1. Comparison of proposed topology with certain similar topologies.

Topology	N_L	N_C	N_{SW}	N_D	M_{CCM}	M_{CCM} at D = 0.5	Common Ground	$S_{CCM} = \frac{V_{S_i}}{V_{in}}$
Boost Converter	1	1	1	1	$\frac{1}{(1-D)}$	2	Yes	$S = \frac{1}{1-D}$
Quadratic Boost Converter	2	2	1	3	$\frac{1}{(1-D)^2}$	4	Yes	$S = \frac{1}{(1-D)^2}$
[4]	1 + 1 coupled inductor	5	2	5	$\frac{2n+1+D}{(1-D)^2}$	14	Yes	$S_1 = \frac{1}{1-D}$ $S_2 = \frac{1+D}{(1-D)^2}$
[5]	1 + 1 coupled inductor	3	1	5	$\frac{1+n-D}{(1-D)^2}$	6	Yes	$S = \frac{2}{1-D}$
[16]	3	4	2	5	$\frac{5+D}{1-D}$	11	No	$S_1 = \frac{1}{1-D}$ $S_2 = \frac{1}{(1-D)^2}$
[22]	8	1	4	17	$\frac{1+7D}{(1-D)}$	9	No	$S_1 = 1$ $S = \frac{1+5D}{1+7D}$
[24]	2	2	2	2	$\frac{1}{(1-D)^2}$	4	Yes	$S_1 = \frac{1}{1-D}$ $S_2 = \frac{1}{(1-D)^2}$
[25]	3	4	1	4	$\frac{1+D}{(1-D)^2}$	6	Yes	$S = \frac{1}{(1-D)^2}$
[26]	3	3	1	5	$\frac{2}{(1-D)^2}$	8	Yes	$S = \frac{2}{(1-D)^2}$
[27]	3	5	2	4	$\frac{1+3D}{(1-D)^2}$	10	Yes	$S_1 = \frac{1}{1-D}$ $S_2 = \frac{1+D}{(1-D)^2}$
[28]	2	5	1	6	$\frac{2(2-D)}{(1-D)^2}$	12	No	$S = \frac{2-D}{(1-D)^2}$
[29]	3	6	1	6	$\frac{(3-D)}{(1-D)^2}$	10	Yes	$S_1 = \frac{3-D}{D^2(1-D)}$. $S_2 = \frac{3-D}{(1-D)^2}$
[30]	2	3	2	3	$\frac{D^2-3D+3}{(1-D)^2}$	7	Yes	$S_1 = \frac{1-D}{D^2-3D+3}$ $S_2 = \frac{1}{D^2-3D+3}$
Proposed Topology	**3**	**6**	**2**	**7**	$\frac{\mathbf{2(3-D)}}{\mathbf{(1-D)^2}}$	**20**	**Yes**	$\mathbf{S_1 = 1}$ $\mathbf{S_2 = \frac{4}{(1-D)}}$

5. Results

In this section, we discuss the simulation results performed on the **P**iecewise **L**inear **E**lectrical **C**ircuit **S**imulation (PLECS) and the experimental results obtained on hardware set-upfor the proposed topology.

5.1. Simulation Results

In this section, the simulation results of the proposed converter are presented. The simulation was carried out in PLECS software at an input voltage of 20 V and switching frequency of 50 kHz. The duty ratio was maintained at 0.4. The value of the inductor was 330 µΩ and its parasitic resistance was maintained at 0.12 Ω, while the value of capacitors was 47 µΩ and its parasitic resistance was kept at 0.1 Ω. The ON-state resistance of the switches was found to be 70 mΩ. With the above parameters, the simulation was performed and the output voltage was found to be $V_O = 248.08$ V at a 40% duty ratio with $V_{in} = 20$ V, which can be seen in Figure 21.

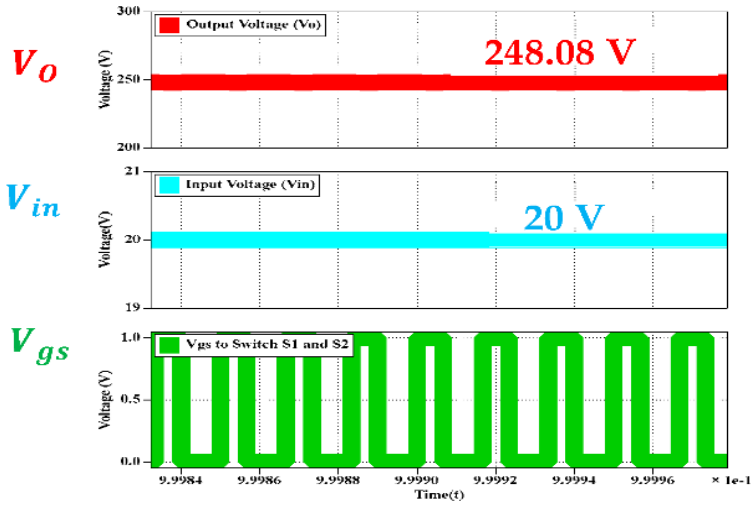


Figure 21. Simulated output voltage (V_O), input voltage (V_{in}), and duty cycle (D).

In Figure 22, the inductor current through inductor L_1 was found to be $I_{L1} = 5.06$ A and $I_{L2} = I_{L3} = 0.58$ A for inductor L_2. The ripple in the current through the inductor was lower and, hence, the average and RMS values were found to be the same.

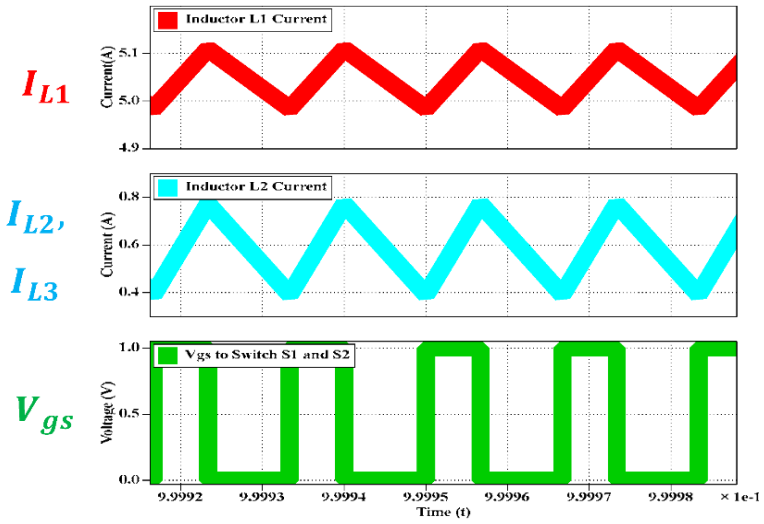


Figure 22. Simulated inductor currents (I_{L1}, I_{L2}, and I_{L3}) and duty cycle (D).

From Figure 23, the peak voltage across switches S_1 and S_2 was found to be $V_{S1(peak)} = 30.687$ V and $V_{S2(peak)} = 155.43$ V, respectively, while the RMS voltage was $V_{S1(rms)} = 23.77$ V. and $V_{S1(rms)} = 120.40$ V, respectively. From Figure 24, the average capacitor voltages in the simulation were found to be $V_{C1} = V_{C2} = 27.5209$ V and $V_{C3} = 58.65$ V, while from Figure 25, the capacitor voltages were $V_{C4} = -56.58$ V, $V_{C5} = 57.16$ V, and $V_{CO} = V_O = 248.08$ V. The ripple in capacitor voltages was negligible and, hence, the RMS and average voltages were found to be the same.

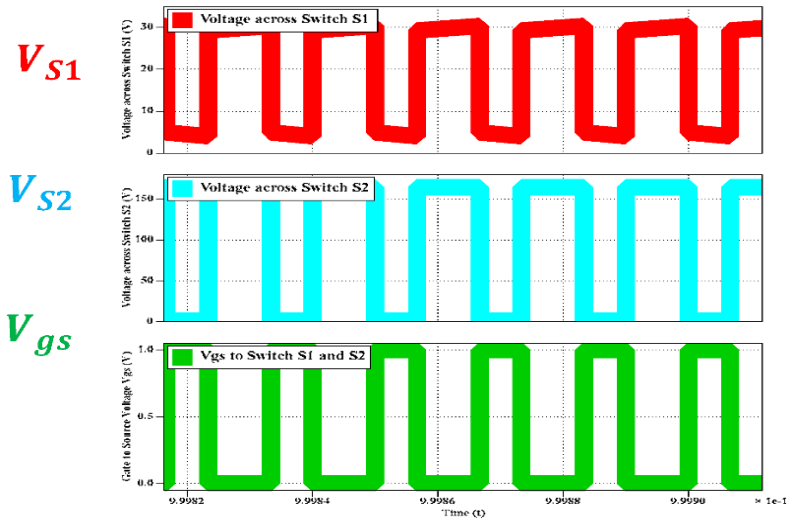


Figure 23. Simulated switch voltages and duty cycle (D).

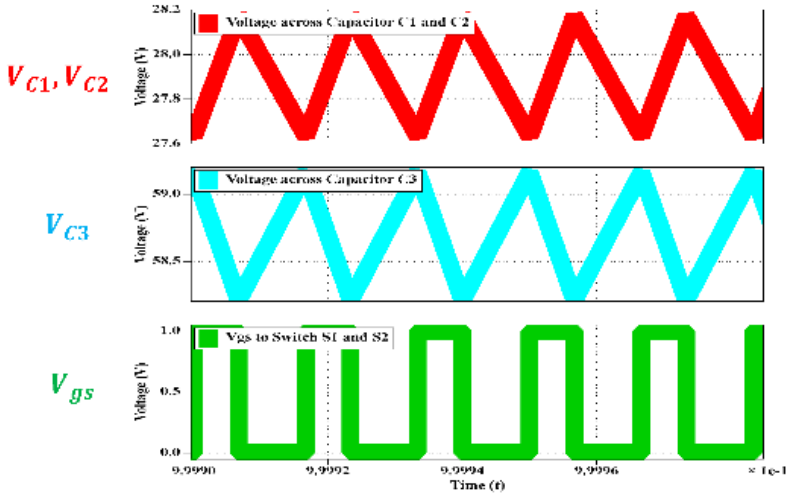


Figure 24. Simulated capacitor voltages and duty cycle (D).

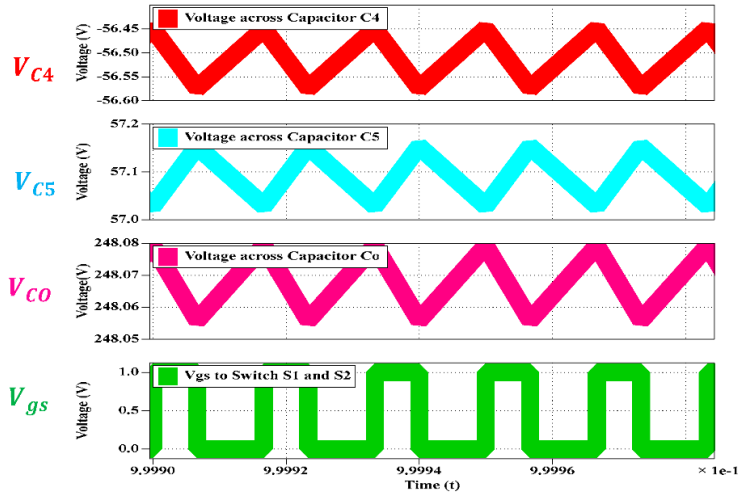


Figure 25. Simulated capacitor voltages and duty cycle (D).

5.2. Experimental Results

The experimental analysis of the proposed converter was carried out on the same parameters as the simulation procedure. To verify the overall voltage boosting, continuous current, and capacitor voltage handling capability of the proposed converter, a hardware prototype of the proposed converter was tested under standard laboratory conditions with the parameters mentioned in Table 2. To demonstrate the working of the topology, a converter with an output power of 200 W at a duty ratio of 40% was implemented with a load resistance of 300 Ω. For switches S_1 and S_2, Power MOSFET with part number SPW52N50C3 provided with a duty cycle (D) of 0.4 operating at a switching frequency (f_s) of 50 kHz was used, whereas diodes ($D_O - D_6$) with part number HER806 were used. From Figure 26, a 20 V DC supply was used at the input side and an output of 240 V was obtained for the same with V_{gs} as the gate drive signal.

Table 2. Hardware values of parameters.

Parameter	Symbol	Value
Input Voltage	V_{in}	20 V
Duty Cycle	D	0.4
Output Power	P_O	67 W
Load Resistance	R_O	850 Ω
Inductors	L_1	330 µH, ESR = 0.12 Ω
	L_2, L_3	0.4 mH ESR = 0.14 Ω
Capacitors	$C_1 - C_5$	47 µF, ESR = 0.1 Ω
	C_O	100 µF, ESR = 0.22 Ω
Diodes	D_O *to* D_6	HER806
Power MOSFETs	S_1, S_2	SPW52N50C3
Driver		TLP250H
Controller		STM32F334R8
Switching Frequency	f_s	50 kHz

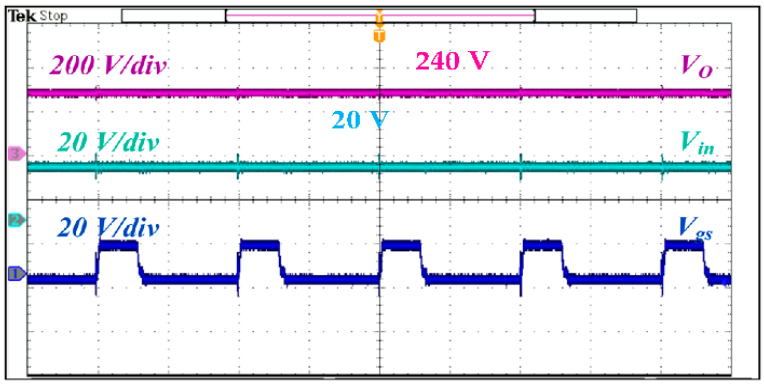


Figure 26. Top to bottom: experimental waveforms of output voltage (V_O), input voltage (V_{in}), and V_{gs} at D = 0.4.

From Figure 27, when the switches are ON, the inductors become charged and the current through them increases. For inductor L_1, it increases from an initial value of 4.8 A to a peak value of 5.2 A and it increases from an initial value of 0.7 A to a peak value of 1.0 A for inductors L_2 and L_3. When the switches are OFF, the inductors release their stored energy, and the currents through them decrease back to their initial values. During the OFF state, the switches are reversed-biased and block a peak voltage of 30 V and 160 V,

respectively, in each cycle, which can be seen in Figure 28. The peak reverse blocking voltage is about 30 V for the switch S_1 and 160 V for switch S_2 for the output voltage of 240 V. Capacitor C_1 has a voltage of 30 V across it, while capacitors C_3 and C_4 have a voltage of 60 V with very-low-voltage ripples as in Figure 29. The experimental setup is shown in Figure 30.

Figure 31 shows the variation in efficiency with the output power as the input voltage is increased. It can be observed that as the input voltage increases, the efficiency of the converter increases. This occurs because with the increase in voltage, the current decreases to conserve the power; hence, the conduction losses across various elements of the converter including switches, diodes, and parasitic resistances of the inductor and capacitor are reduced.

The maximum efficiency of the converter is found as 97.85% at 30 V, 66 W followed by 96.5% for operation at 20 V for the same power. From Figure 32, the majority of the conduction losses i.e., around 39%, occur in the capacitors, out of which 58.5% of the losses in capacitors are due to capacitor C_3 itself. The switches and diodes contribute 40% of the total losses. The losses can be further reduced by using diodes and switches with low parasitic resistance.

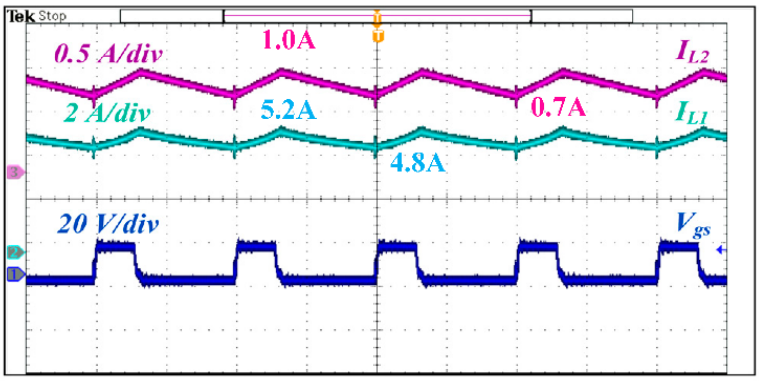


Figure 27. Top to bottom: experimental waveforms of current of inductor L_1 (i_{L1}), inductor L_2 (i_{L2}), and V_{gs} at D = 0.4.

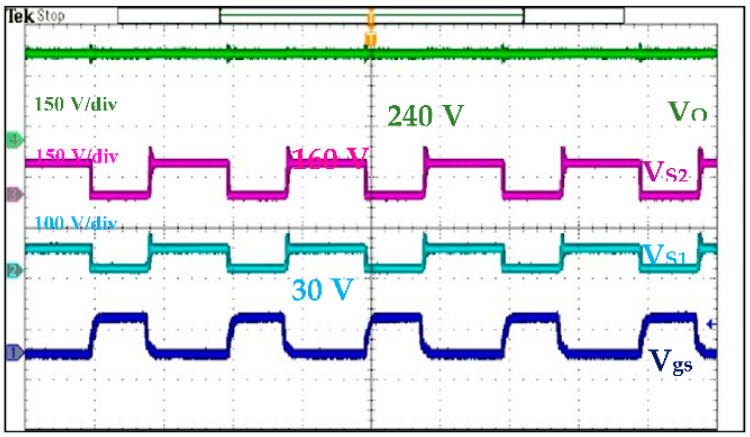


Figure 28. Top to bottom: experimental waveforms of output voltage (V_O), voltage across switch S_2 (V_{S2}), voltage across switch $S_1(V_{S1})$, and V_{gs} at D = 0.4.

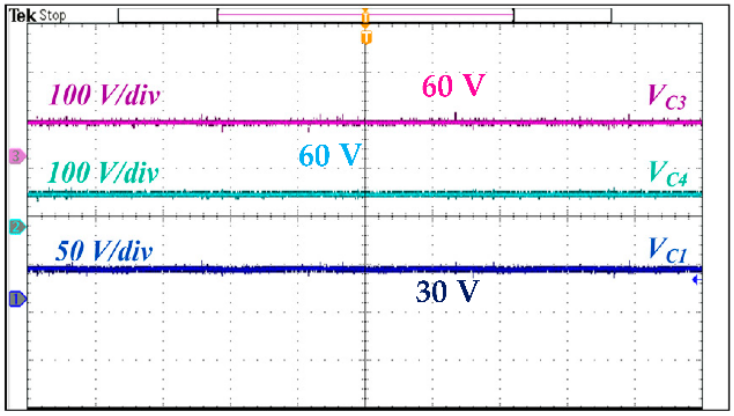


Figure 29. Top to bottom: experimental waveforms of voltage across capacitor C_3 (V_{C3}), the voltage across capacitor C_4 (V_{C4}), and the voltage across capacitor C_1 (V_{C1}) at D = 0.4.

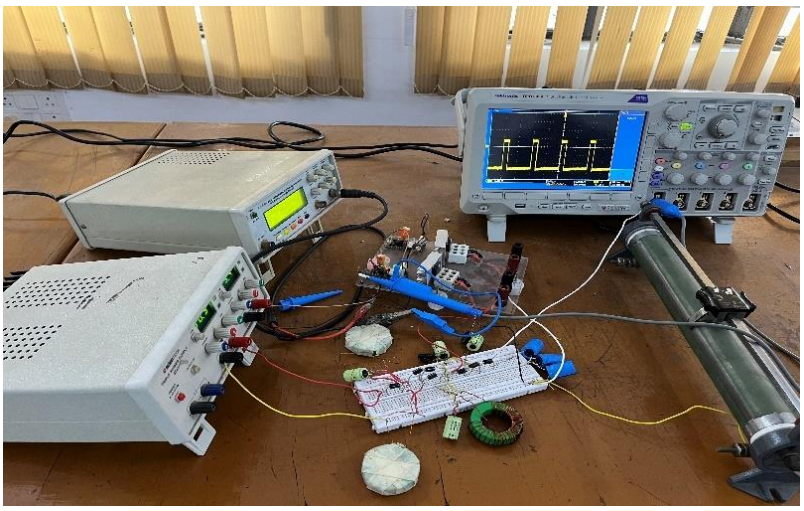


Figure 30. Experimental Set-up.

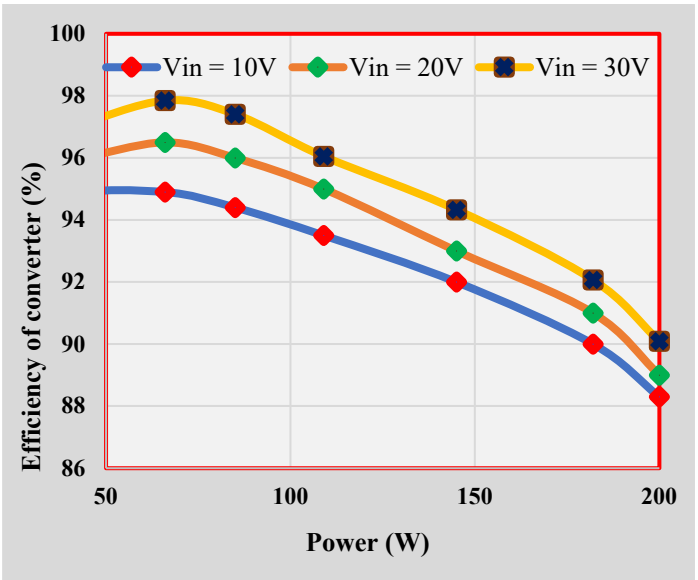


Figure 31. Simulated efficiency vs. output power comparison of the proposed converter at different input voltages.

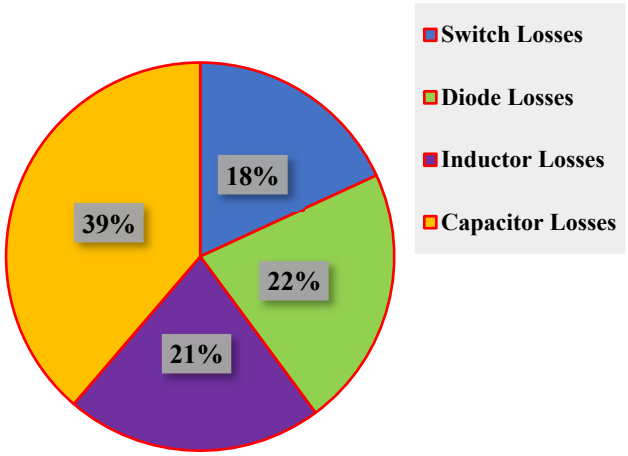


Figure 32. Distribution of losses across various elements of the converter.

6. Conclusions

The converter produces an ideal voltage gain of 11 times at a duty ratio of 30% with an ideal voltage gain of 14.44 at a duty ratio of 40%. The nonideal gain of the proposed converter at a D less than 60% is still found to be higher as compared to the ideal gains of the compared converters. In addition, the voltage stress across the switches is found to be lower than the output voltage and is also much lower than the compared topologies even at higher duty ratios. The voltage stress across S_1 is 6.92% of the V_o and across switch S_2, it is 46.15% of V_o at the duty ratio of 40%. The maximum efficiency of 97.85% is obtained at 66 W when the input voltage is 30 V, while it is 96.44% at a load of 38 W, keeping the input voltage at 20 V. The efficiency of the prototype model decreases with the power level due to the absence of galvanic isolation and parasitic resistances. The voltage and current stresses across the elements are low, which can be observed from the analysis and the hardware results. The converter has a common ground and operates at continuous input current, making it feasible for low- and medium-power solar and renewable energy PV applications.

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