electronics

MDPI

Article

A Multi-Source Co-Simulation Method for the Thermal Stability of GaAs Sub-6G Power Amplifier with Adjustable Bias Current

Yuanbo Ma [1,2,†], Zhaohui Wu [1,3,†] and Bin Li [1,*]

[1] School of Electronics and Information Engineering, South China University of Technology, Guangzhou 510641, China; eeybma@mail.scut.edu.cn (Y.M.); phzhwu@scut.edu.cn (Z.W.)
[2] School of Electrical and Computer Engineering, Nanfang College Guangzhou, Guangzhou 510970, China
[3] China-Singapore International Joint Research Institute, Guangzhou 510700, China
* Correspondence: phlibin@scut.edu.cn
† These authors contributed equally to this work.

Abstract: In this paper, the thermal stability of GaAs heterojunction bipolar transistor (HBT) power amplifier (PA) in a sub-6G band has been improved by a multi-source co-simulation method. To reduce the parameter errors caused by the variations of thermal resistances, a co-simulation method for the multiple heat sources of fully-integrated PA is proposed. Specifically, an adjustable bias circuit is applied on the PA for temperature compensation using a zero-to-absolute-temperature (ZTAT) current. To verify the proposed method, a sub-6G PA is realized in the GaAs HBT process. The experimental results show that the variations in power added efficiency and output power is stabilized due to the 3.5% error ZTAT current. The errors between simulation and measurement are reduced from 6% to 1%. According to the thermal factor defined in co-simulation, the working temperature decreases 10 °C, while the area only increases 27%. The above results prove that that thermal stability and the simulation reliability can be co-designed with the minimal area cost.

Keywords: sub-6G Power amplifier; GaAs HBT; thermal stability; ZTAT current; co-simulation

Citation: Ma, Y.; Wu, Z.; Li, B. A Multi-Source Co-Simulation Method for the Thermal Stability of GaAs Sub-6G Power Amplifier with Adjustable Bias Current. *Electronics* **2022**, *11*, 2000. https://doi.org/10.3390/electronics11132000

Academic Editor: Kai Fu

Received: 29 May 2022
Accepted: 24 June 2022
Published: 26 June 2022

1. Introduction

Benefiting from the high-power density and process yield, GaAs heterojunction bipolar transistor (HBT) process becomes the most promising candidate of power amplifiers (PAs) for mobile terminals [1–4]. With the growth of frequency and integration of sub-6G technology, requirements in thermal stability and electrical-parameter accuracy on PAs keep increasing to guarantee high performance [5–7], making it very challenging for the GaAs HBT PAs. First of all, comparing the temperature characteristics of Si, GaAs and GaN, the thermal conductivity of GaAs is the worst. The narrow bandgap, low material-preparation temperature and insufficient toughness make the thermal conductivity of GaAs only one-third and one-quarter of that of silicon and GaN, respectively. The thermal coupling the inside chip becomes stronger and the operating temperature easily exceeds 80 °C [8,9]. Secondly, at the high temperature, the thermal resistances of HBT are added to simulate the electrical parameters, which are shifted because of the self-heating of GaAs. However, since the simulation accuracy decreases with the increase in temperature, the variations in the thermal resistances of HBT tend to increase the errors between simulation and measurement (ESMs).

To improve the thermal stability, many advanced techniques have been proposed in the current literature [10–13]. The temperature compensation technique is one of the most efficient methods. Figure 1 is a functional diagram of PA in which the bandgap (BG) independent current source is employed. The proportional-to-absolute-temperature (PTAT) current compensates the complementary-to-absolute-temperature (CTAT) current so as to

make the current independent from temperature [14,15]. With the help of an operational amplifier (op-amp), the bias current can be independent from the supply voltage as long as the open-loop gain of op-amp is sufficiently high. In order to make the current adjustable, several trimming bits, which are issued from the digital interface MIPI of mobile terminals, are used [16–18]. However, the complicated schematic, which requires the perfect matching, is still affected by the temperature coefficient (TC) of the resistor. The resistors can be replaced by diode-connected transistors to generate zero TC bias currents [19,20], enabling no-resistor BG schemes to perform quite well in-line regulation. However, the TCs of currents are still large due to the non-linear thermal property voltages of diode-connected transistors. Additionally, as it is limited by the single-npn-device process, the advantage of a BG current source is prominent in the CMOS process [21,22].

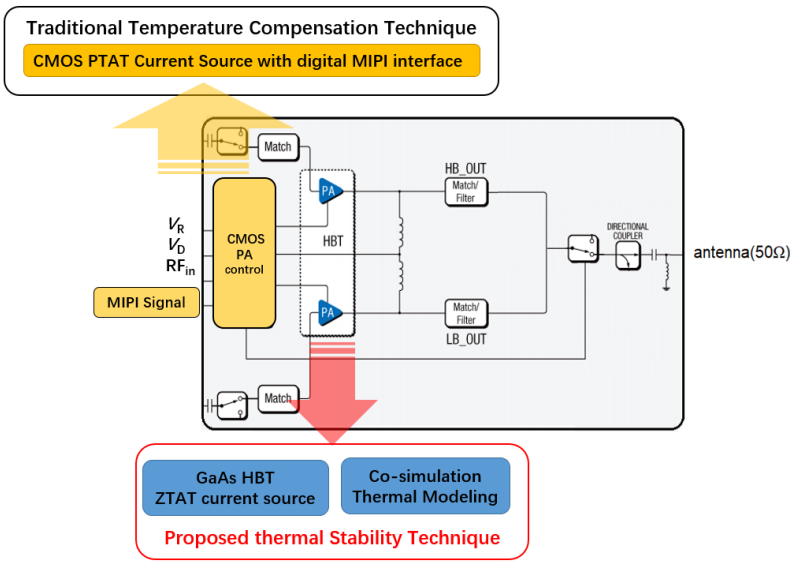


Figure 1. Functional diagram of PA with different temperature compensation techniques.

The thermal stability can also be improved by the accurate thermal modeling [23], which is capable of simulating the parameters as close to the measured results as possible. Several electro-thermal techniques have been proposed to optimize the accuracy of thermal modeling, in terms of the device models [24,25], thermal systems [26,27], simulators [28,29] and algorithms [11,30]. However, even if particular efforts have been made on the thermal analyses, which have been studied quite comprehensively in various HBT devices or CMOS Pas, little attention has been paid in the fully integrated HBT PAs [31]. The ESM, temperature and area cannot be reduced simultaneously in traditional techniques, which do not include the layout and package.

In this paper, an adjustable current bias scheme to bias the PA with a zero-to-absolute-temperature (ZTAT) current for improving the thermal stability is presented, and a co-simulation method for multiple heating sources to minimize the ESM is proposed. In the current bias scheme, the positive TC of HBT current is compensated by the *equal-but-opposite* TC of voltage. The ZTAT current is independent from the temperature as long as the area of diode and HBT are set properly. The proposed bias circuit has no requirement for match and no limitation to the temperature coefficient of resistor. Therefore, it is able to reduce parasitic parameters and process requirements, while applying stable bias current. In the co-simulation method, with the feedback of exact thermal resistances of each amplifier cells, the ESM and the temperatures of amplifier cells can be reduced with an area-saving layout. Differing from the existing methods, the proposed method, which focuses on the circuit and layout of fully integrated HBT PA, solves the problem that thermal simulation and electrical simulation cannot effectively feedback parameters to each other. Moreover, the multi-heat source temperature distribution and chip area are specially introduced to improve the accuracy and practicality of co-simulation. In the design and pre-simulation

stage, the electrical parameters under real working conditions can be obtained. The ZTAT current source and co-simulation thermal modeling are presented in Sections 2 and 3, respectively. The experimental results of an implementation of a class-AB PA in the sub-6G band fabricated in the GaAs HBT process are analyzed in Section 4.

2. Principle of the Proposed Bias Circuit for ZTAT Current

In a typical independent current source, resistors are used to convert the supply voltage to current, which is then mirrored to amplifier cells by a current mirror (CM). However, because of that resistor, the current is proportional to the temperature and unable to suppress the variation in supply voltage. Although this problem can be solved by BG by generating the PTAT current and the CTAT current from a pair of substrate BJTs, the complexity of the circuit significantly increases the footprint. Therefore, this work proposes the bias circuit that is able to address the above problems by employing a diode and HBT to generate the equal-but-opposite TC of voltage to compensate the TC of current. As shown in Figure 2, the proposed bias circuit is composed of a DRH scheme and a CM scheme.

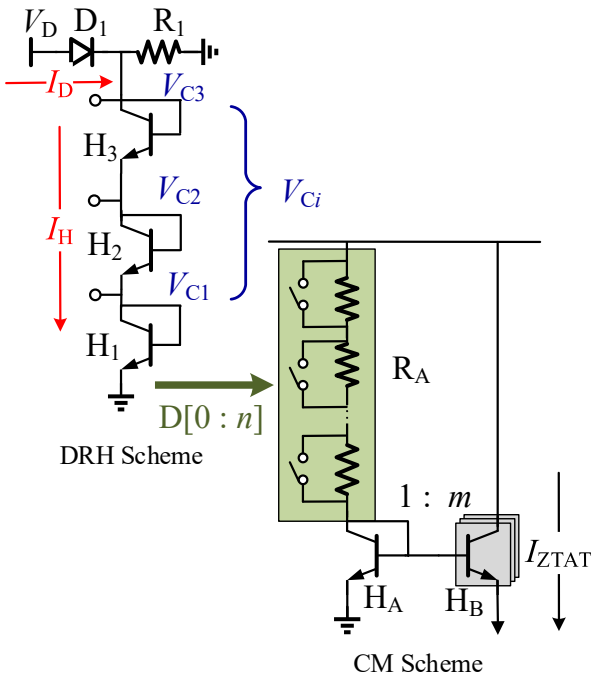


Figure 2. Simplified scheme of the proposed adjustable ZTAT bias circuit.

The DRH scheme, which consists of a diode D_1, a resistor R_1 and a branch of HBTs, generates a set of temperature-sensing voltages V_{Ci} with different TCs. Assuming the currents of the diode and HBTs are I_D and I_H, respectively, the collector voltage V_{C3} of the top HBT is given by

$$V_{C3} = (I_D - I_H)R_1 \tag{1}$$

Since the diode and diode-connected HBT have the similar PN junction structure, the TCs of I_D and I_H can be calculated by the same equation. Under forward bias, the diode current can be written as [32]

$$I_D = I_s \exp(\frac{V}{V_T}) \tag{2}$$

The effect of temperature on I_D is produced mainly through the reverse saturation current I_S and the thermal voltage V_T. The I_S is given by

$$I_s = qA_D(\frac{D_p}{L_p N_d} + \frac{D_n}{L_n N_a})n_i^2 \tag{3}$$

where A_D is the junction area and n_i is the intrinsic carrier concentration. The parameters in parentheses have little relationship with temperature, so the effect of temperature is produced mainly through ${n_i}^2$, which can be estimated as

$$I_s \propto A_D n_i^2 \propto A_D T^3 \exp(-\frac{E_{g0}}{kT}) \tag{4}$$

where T is the ambient temperature, k is the Boltzmann constant, q is the electron charge and E_{g0} is the band gap at 0 K of GaAs. Taking the derivative of Equation (4), the TC of I_S is estimated by

$$\mathrm{TC}_{I_S} \propto qA_D \frac{E_{g0}}{kT^2} \tag{5}$$

Substituted $V_T = kT/q$ and Equation (5) into the derivative of Equation (2), the TC of I_D is estimated as

$$\left.\frac{dI_D}{dT}\right|_{V_D} \propto q\left(\frac{A_D E_{g0} - V_D}{kT^2}\right) \tag{6}$$

According to Equation (6), the TC of I_D is only related to A_D at a certain voltage V_D of diode. The TC of the current of diode-connected HBT is similar to that of the diode. At a certain base-to-emitter voltage V_{be} of HBT, the TC of I_H can be deduced from Equation (6) with the HBT area A_H. Combining Equation (1) and Equation (6), the TC of V_{C3} can be simply estimated as

$$\begin{aligned} \mathrm{TC}_{V_{C3}} &\propto \left(\mathrm{TC}_{I_D}\big|_{V_D} - \mathrm{TC}_{I_H}\big|_{V_{be}}\right) \times \mathrm{TC}_{R_1} \\ &\propto \left(I_D A_D \frac{E_{g0}}{kT^2}\Big|_{V_D} - I_H A_H \frac{E_{g0}}{kT^2}\Big|_{V_{be}}\right) \times \mathrm{TC}_{R_1} \end{aligned} \tag{7}$$

Since the resistor R_1 in the circuit is single GaAs resistor, the TC of R_1 is a positive constant. Based on Equation (7), the TC of V_{C3} is only related to the TC of the current I_D-I_H, which is proportional to the area A_D and A_H under the certain voltage V_D and V_{be}. Setting the value of A_D and A_H so that the TC of I_D is less than the TC of I_H, the TC of V_{C3} is inversely proportional to temperature. The other collector voltages V_{Ci} are calculated based on resistances as

$$V_{Ci} = \frac{\sum_{i=1}^{i} R_{H_i}}{R_{H_1} + R_{H_2} + R_{H_3}} V_{C3} \tag{8}$$

Then, the TCs of V_{Ci} can be expressed as

$$\begin{aligned} \mathrm{TC}_{V_{Ci}} &= \tfrac{d}{dT}\left(\tfrac{\sum_{i=1}^{i} R_{H_i}}{R_{H_1}+R_{H_2}+R_{H_3}} V_{C3}\right) \\ &= \mathrm{TC}\left(\tfrac{\sum_{i=1}^{i} R_{H_i}}{R_{H_1}+R_{H_2}+R_{H_3}}\right) V_{C3} + \tfrac{\sum_{i=1}^{i} R_{H_i}}{R_{H_1}+R_{H_2}+R_{H_3}} \mathrm{TC}_{V_{C3}} \end{aligned} \tag{9}$$

In the first part of Equation (9), the TCs of the ratio of resistances are constant, so it has little effect on the TC of V_{Ci}. The second part of Equation (9) is proportional to V_{C3} with different slopes. The slopes decreasing from top to bottom provide multiple TCs of voltages to compensate different currents in multistage-PAs or stack-PAs. Furthermore, considering the accuracy and availability, the adjustable resistor R_A is designed to be modified by the trimming bits D [0: n].

In the CM scheme, the ZTAT current calculated by V_{C3} and R_A is mirrored to the amplifier cells through a pair of HBTs with a 1: m ratio. When the temperature increases, the quiescent currents of HBTs have a positive slope. The compensation for the positive TCs can be gained by the V_{Ci} with the *equal-but-opposite* TCs. Thus, the ZTAT current is as independent from temperature as possible.

3. Principle of Co-Simulation Method for Differential Heat Sources

The thermal simulation plays an important role in correcting the parameter variations over temperature. With the help of electrical and thermal co-simulation, the ESM can be corrected as accurately as possible. However, the temperature variations of different heat sources make the results of traditional co-simulations unreliable. In addition, the thermal modeling without concerning the area cost will hardly be adopted. Figure 3 is the procedure of the proposed co-simulation method. The parameters of the electrical and thermal simulations are employed to improve the accuracy and reduce the ESM.

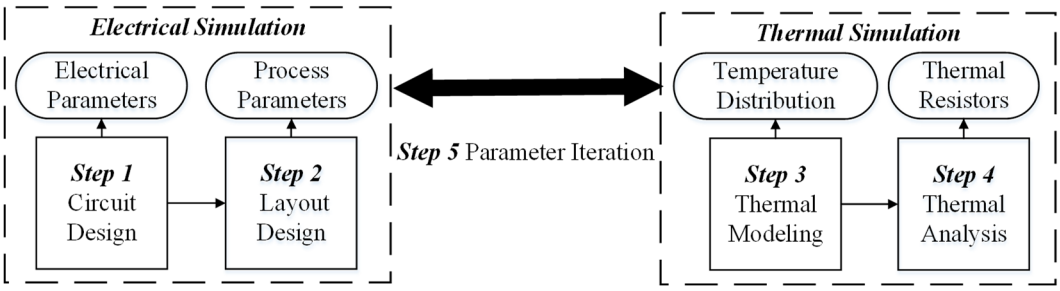


Figure 3. Procedure of proposed co-simulation method.

3.1. Circuit Design

The HBT PA is designed for sub-6G handset products with the parameters of the output power P_O, power added efficiency (PAE), power gain (PG) and supply voltage V_D. The PA is functionally divided into three schemes: impedance matching, bias control and HBT amplifier cells. In practice, the impedance matching with passive devices is normally off-chip for flexibility. The bias control, which consists of the bias circuit and switch array, has little effect on the thermal consumption. Therefore, the HBT amplifier cells release most of the thermal power H_0 as follows,

$$H_0 = V_D I_Z - P_O = V_D I_Z (1 - \text{PAE}) \tag{10}$$

3.2. Layout Design

Considering the area of HBT amplifier cells, the layout is optimized following the principle: the amplifier cells are divided into an $I \times j$ amplifier-cell array with the individual area $S_{i,j}$, separated by a distance $D(x, y)$ from cell to cell, and marginalized to the edge of chip. The simplified layout is shown in Figure 4.

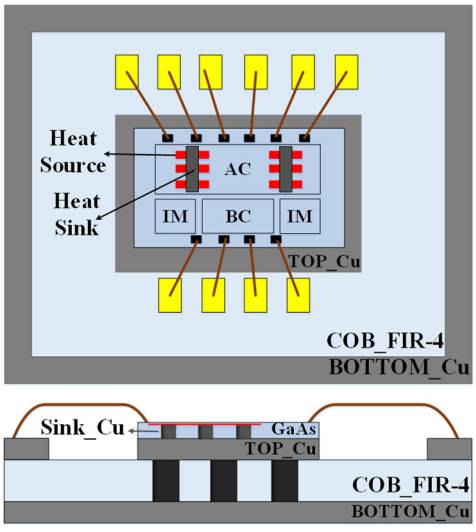


Figure 4. Simplified modeling topology of proposed method.

3.3. Thermal Modeling

The modeling focused on the heat sources and dissipations can be built by the following the steps.

1. Modeling the heat sources as plates. Because the heat sources are thinner, the heat dissipation is concentrated on the upper surface.
2. Modeling two primary materials for heat dissipating differently. One is the copper heat sinks at the bottom of chip, which connect the emitter of HBTs with the COB substrate. Those copper sinks release the majority of heat because of the good thermal conductivity. The other is the bonding wires at the top of chip, which can be simplified due to the limited area.

3.4. Thermal Analysis

In thermal analysis, to guarantee the effective convergence of meshing, parameters such as the material definitions, boundary conditions and thermal parameters are used. The temperature distribution $T_{i,j}$ can be calculated as

$$F_{i,j} = \frac{H_{i,j}}{S_{i,j}} = h(T_{i,j} - T_0) \tag{11}$$

where h is heat convection, T_0 is initial temperature, $F_{i,j}$ and $H_{i,j}$ are the heat flux and the heat power of each amplifier cell, respectively.

3.5. Parameter Iteration

The thermal resistances $r_{i,j}$ calculated by the temperature distribution $T_{i,j}$ are fed back into the electrical simulation. The parameter errors of the electrical simulation caused by the temperature variations will be corrected after several iterations. The $r_{i,j}$ is calculated as

$$T_{i,j} = T_0 + r_{i,j} \times H_{i,j} \tag{12}$$

The co-simulation also illustrates the relationship between the chip area and the temperature distribution. With the help of a thermal factor K, the layout can be optimized to improve the thermal stability with minimal area cost.

4. Experimental Results and Analysis Conclusions

In this section, a PA working at 3.5 GHz is fabricated in GaAs HBT process to verify the proposed method. The schematic and die photo are shown in Figures 5 and 6, respectively. To minimize the influence of other components on thermal power, the PA is designed as the single-stage and the impedance matching is out of the chip. In the bias control, the R_A is controlled by three trimming bits D [0:2]. The resistance can be adjusted from 0.8 kΩ to 0.98 kΩ with a 3.5% error to improve the accuracy and flexibility. Usually, the resistance is adjusted by the trimming bits provided by the interface MIPI in handsets. In the proposed PA, the combined resistors are simply shorted to obtain a 0.85 kΩ R_A for the required current. In the HBT amplifier cells, a ballast resistor R_B is added at the base of HBT to prevent current collapse.

4.1. The Experimental Results of PAs

To satisfy the 30 dBm P_O and 50% PAE of the PA for the sub-6G handsets, the bias circuit needs to generate 1.4×10^{-3} A current to the HBT amplifier cells with an area of 3840 μm^2 under a 5 V supply at 25 °C. The parameters of the bias control scheme are listed in Figure 5 and Table 1. The TCs of R_1, I_D-I_H and V_{C3} of the bias circuit are shown in Figure 7. The TC of R_1 and differential current I_D-I_H are 5.65 Ω/°C and −8.03 μA/°C, respectively. They generate the −2.68 mV/°C V_{C3} with 4.02 V to supply the current mirror. The simulated and measured ZTAT currents from −15 °C to 85 °C are compared in Figure 8. At 25 °C, the measured current 1.38×10^{-3} A meets the design requirement

with a 1.4% error due to the over-ideal simulation model. When the temperature changes, the current error is stabilized within 3.5% over a 100-degree range. The comparison of current references is presented in Table 1. The implement area of 0.035 mm^2 is acceptable based on the 0.5 µm GaAs HBT process. As a well-designed product of Maxim, the current error of [18] is the best, but the number of pins and area are considerable. Compared with other complicated current bias circuits whose areas are 1~2 times larger, the current error of the proposed circuit is still competitive, even smaller than the errors of other adjustable references.

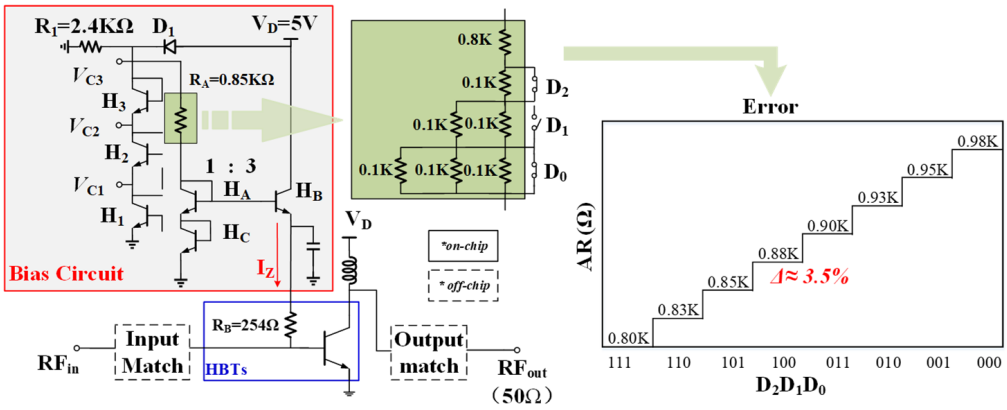


Figure 5. Schematic of PA with the proposed ZTAT current.

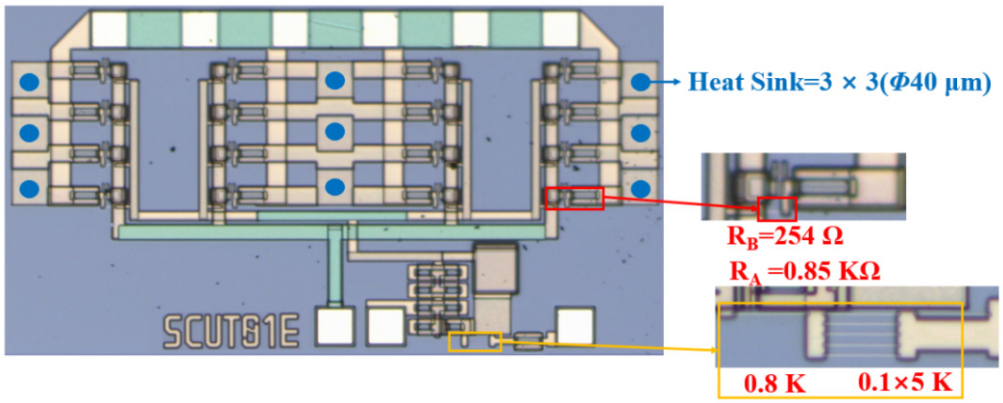


Figure 6. Die photo of PA with the proposed ZTAT current.

Table 1. Comparison of the proposed bias circuit with current references.

	This Work	[14]	[15]	[16]	[17]	[18]
Current (A)	**1.4 m**	99.7 µ	0.338 µ	20 µ	16.6 µ	2.5
ΔT (°C)	**−15~85**	−40~125	0~80	−40~80	−20~100	−20~70
Accuracy (%)	**3.5%**	3.5%	3.1%	10%	4%	2%
Process	**0.5µm GaAs**	65 nm CMOS	0.18 µm CMOS	0.35 µm CMOS	0.35 µm CMOS	N/A CMOS
Area (mm^2)	**0.035**	0.04	0.00075	0.139	0.0576	9(package)
Trimming bits	**3**	No	No	5	18	7
Devices (µm)	**D_1:2 × 4; HBT:2 × 20 × 2**					

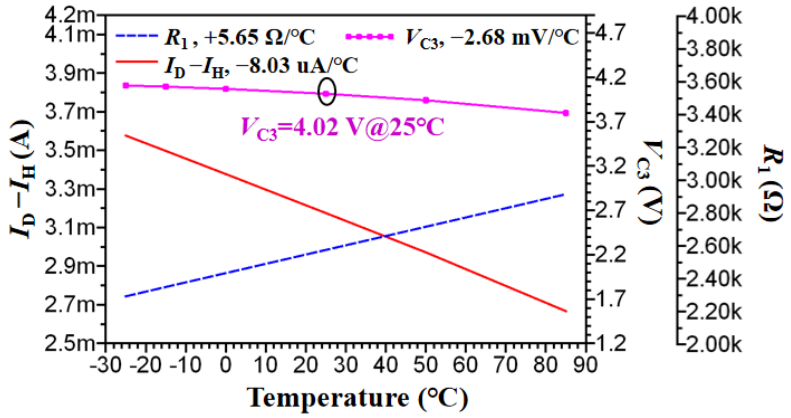


Figure 7. Simulated R_1, I_D, I_H and V_{C3} over temperature.

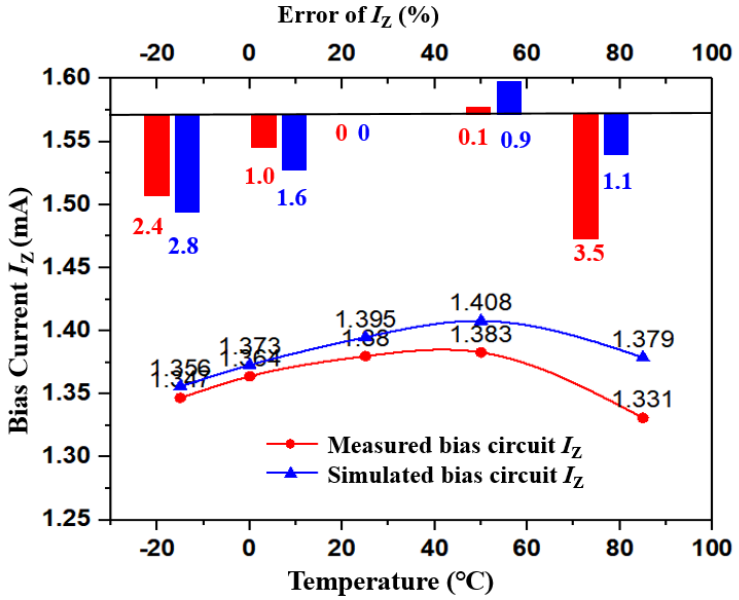


Figure 8. Measured and simulated ZTAT currents over temperature.

The measured PAE, P_O and PG at −15 °C, 25 °C and 85 °C from 14 dBm to 23 dBm RFin are compared in Figure 9. It is demonstrated that the variations between 25 and 85 °C are much smaller than the variations between −15 and 25 °C. Moreover, it is seen that the higher temperature has greater influence on the parameters. The variations between 25 and 85 °C at each input power are also shown at the top of the figures. The error of PAE between 25 °C and 85 °C is 7% when RFin is small and becomes stable at 3.7% after FRin larger than 19 dBm. The error of P_O between 25 °C and 85 °C is 0.7 dBm at beginning and then stabilized at 0.1 dBm after RFin larger than 19 dBm. The error of PG between 25 °C and 85 °C starts at 1dB and then stabilized at 0.2 dB. Since the PAE represents the heat loss of the PA, the increase in temperature results in the decrease in PAE and P_O. However, the variations of PAE and P_O cannot increase continuously with the temperature when RFin is larger than 19 dBm. Different from PAE and P_O, the PG decreases with the increasing input power. The variations of PG are also much smaller and tend to be stable after 19 dB. However, the stabilizing effect of the proposed bias circuit on PG is not as good as the effect on PAE and P_O. The reason is that the PG is closely related to the impedance matching and thermal performance of devices. In summary, the designed PA can be stabilized by the proposed circuit when the heat loss goes higher.

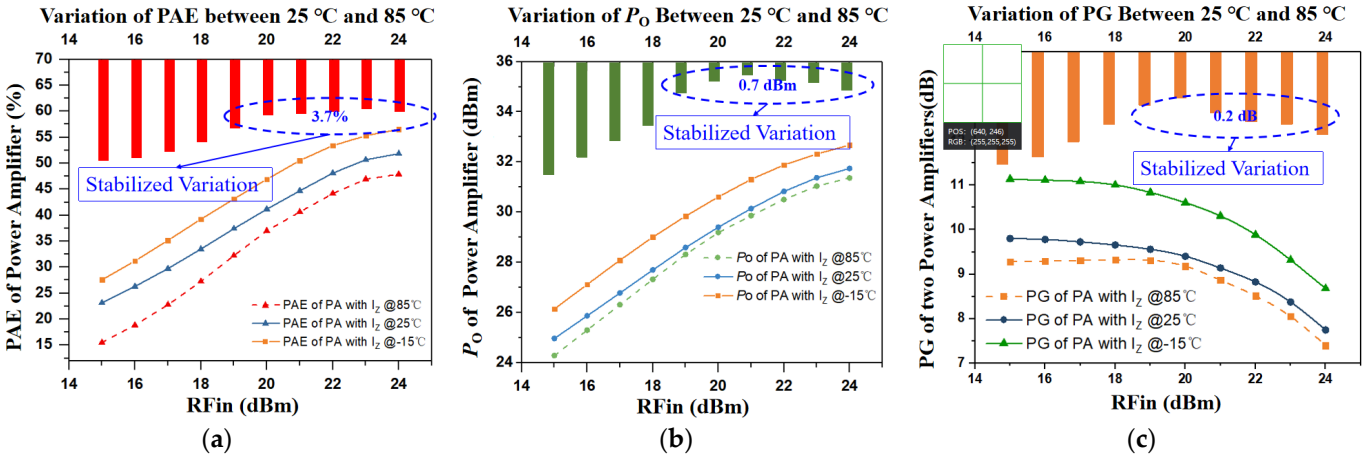


Figure 9. (**a**) Measured PAE of proposed bias PA; (**b**) Measured *P*o of proposed bias PA; (**c**) Measured PG of the proposed bias PA over input power at −15 °C, 25 °C and 85 °C.

The measured ACPR and EVM at different temperatures are summarized in Table 2. At 25 °C, the lower ACPR and upper ACPR are −50.28 dBc and −51.07 dBc, respectively. The results become better by 5 dBc at −15 °C and become worse by 4 dBc at 85 °C. The EVM is about 3.1% at 25 °C. It increases about 0.5% at −15 °C and decrease 0.4% at 85 °C, respectively. The variations in ACPR and EVM are mainly caused by the thermal parameters of devices. It is verified that the designed PA can perform well to meet the requirements of mobile terminals over the temperature range of −15 to 85 °C.

Table 2. Comparison of the measured ACPR and EVM results over temperature.

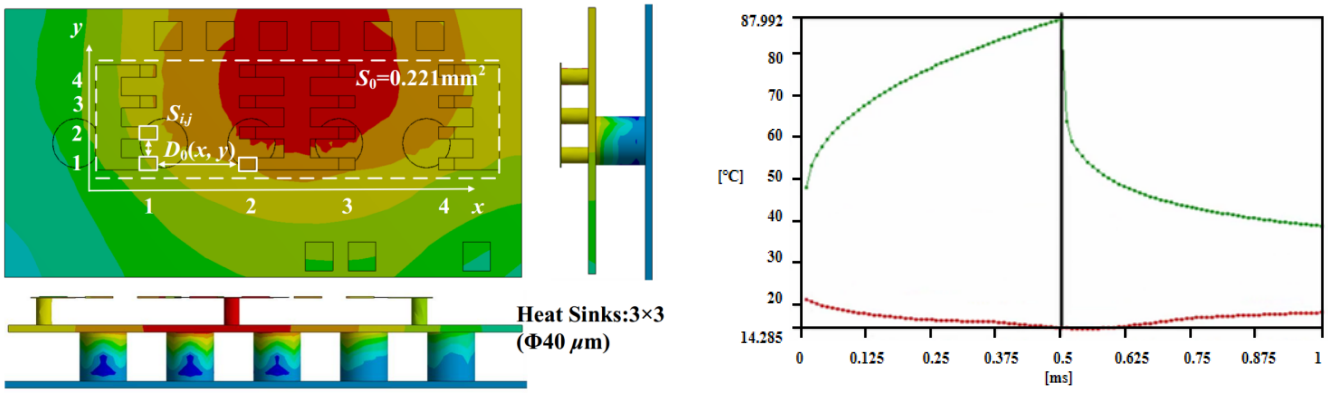
Parameters	Measured Condition		
	−15 °C	**25 °C**	**85 °C**
−ACPR (dBc)	−55.01	−50.28	−46.12
+ACPR (dBc)	−56.13	−51.07	−46.90
EVM (%)	2.6	3.1	3.7

4.2. The Experimental Results of Co-Simulation

The model of the PA in Figure 10 is built strictly following the layout. Figure 10a presents the temperature distribution of each part of the chip, while Figure 10b presents the trend of temperature over time of Figure 10a. The HBT amplifier cells are divided into 4 × 4 cells with equal heat area $\{S_{i,j}\}_{i=1}^{4}\}_{j=1}^{4} = 40 \times 30\ \mu m^2$, separated each other with equal distance $\{D_0(x,y)\}_{x=1}^{3}\}_{y=1}^{3} = (200, 75)\ \mu m$, and marginalized to the upper edge of chip. The 3 × 3 copper cylinders (Φ40 μm) are the thermal sinks to dissipate heat power through two-layer substrates. In this model, some unimportant structures are simplified because they have little contribution to the thermal analysis.

The thermal power H_0 = 1.303 W is released at the surface of HBTs, and the heat flux F_0 = 2.5 × 108 W/m^2 is then assigned to each amplifier cell. After the thermal analysis, the temperature distribution and the thermal resistances are shown in Figure 11. The temperatures range from $T_0(3, 2)$ = 88 °C to $T_0(1, 1)$ = 70 °C. It is worthy of concern that the maximum temperature T_{0max} = 88 °C is beyond the recommended operating temperature (85 °C) and the temperature variation ΔT_0 = 17 °C is considerable enough to affect simulation. The thermal resistances $r_0(i, j)$ calculated by $T_0(i, j)$ are subject to a variation of 217 °C/W. Table 3 is the comparison of the experimental results with different thermal resistances. In the electrical simulation without thermal modeling, the values of $r_0(i, j)$ for all the amplifier cells are 0 at 25 °C and 740 Ω/W at 85 °C, respectively. The ESMs are up to 6%. In the co-simulation, the exact $r_0(i, j)$ are assigned to the amplifier cells and

the ESMs decrease to 1%. Taking the advantage of co-simulation, the simulation errors can be eliminated effectively before tapeout.



(**a**) (**b**)

Figure 10. (**a**)Thermal modeling of proposed bias PA; (**b**)Temperature distribution of thermal simulation.

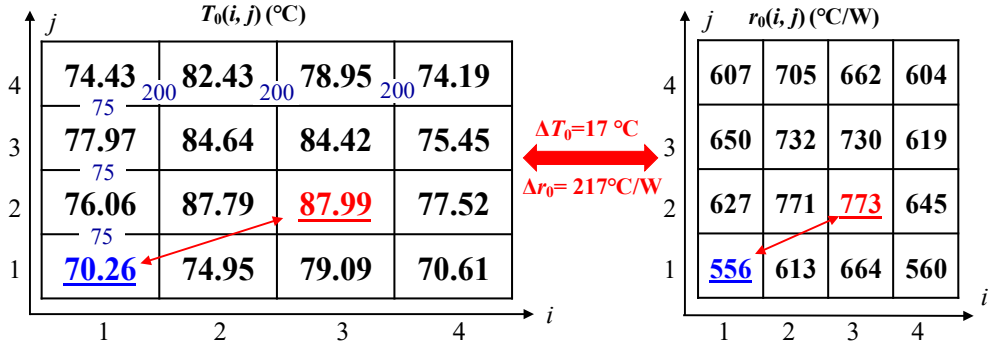


Figure 11. Temperature distribution and thermal resistances of amplifier cells.

Table 3. Comparison of the measured results and simulated results.

	No.	Condition	PG (dB)	PAE (%)	P_O (dBm)	Error(%)
Measured results	1	−15 °C	9.735	51.017	31.73	
	2	25 °C	8. 83	48.10	30.85	
	3	85 °C	8.45	44.38	30.45	
Simulation results without thermal model	4	−15 °C, r = 491 Ω/W	9.96	53.53	31.96	
	5	25 °C, r = 0	9.30	50.73	31.39	
	6	85 °C, r = 740 Ω/W	7.95	43.75	29.95	
			5.91%	1.45%	1.64%	(3−6)/3
Co-simulation results	7	85 °C, $r_0(i, j)$	8.46	44.41	30.46	
			0.73%	**0.97%**	**0.20%**	**(3–7)/3**

The proposed co-simulation cannot only improve the simulation accuracy, but also optimize the heat distribution, so as to reduce the temperature variations in the chip. Usually, increasing the distance between the heat sources is the preferred solution to reduce the temperature. Once the area cost is considered, increasing distance may not be acceptable. With the help of co-simulation, the temperature can be reduced with minimal area. To find the relationship between temperature and area, the proposed method defines the thermal factor K that consists of three normalized indicators as

$$K = \frac{S_n}{S_0} \times \frac{T_{\max\, n}}{T_{\max\, 0}} \times \frac{\Delta T_n}{\Delta T_0} \tag{13}$$

where S_n, T_{maxn} and ΔT_n are area, maximal temperature and temperature variation of the n-th modeling. The smaller the K, the better the performance. Figure 12 shows the results of eight models when gradually increasing the distance. The details of the program are:

1. The temperatures of upper-central amplifier cells are higher than that of the lower-outer ones, so the $D(x)$ and $D(y)$ are gradually increased by 25 μm from center to outside and by 50 μm from top to bottom, respectively.
2. The $K_6 = 0.62$ is minimal in the 6th modeling where $T_{max6} = 76.5$ °C and $\Delta T_6 = 9$ °C. The area is $S_6 = 0.31$ mm^2 with a 40% increase. Figure 13 is the results of the 6th modeling.
3. The maximal temperature T_{max} stops falling after the 6th modeling. Continuing to increase the distance will be useless to reduce the temperature. There are two reasons: no matter how wide the spacing is, there must be 50% thermal power according to PAE; the heat dissipation is limited by the thermal conductivity of the heat sinks.
4. Using the thermal factor K, the PA can be customized according to the specific requirements. For example, if the area cost is the first priority, the $K_3 = 0.68$ is a considerable result in the 3rd modeling where $T_{max3} = 79.4$ °C $\Delta T_3 = 10.7$ °C and $S_3 = 0.28$ mm^2 with only 27% increase.
5. For every 27% increases in area, the temperature reduces 10 °C and temperature variation reduces 7 °C.

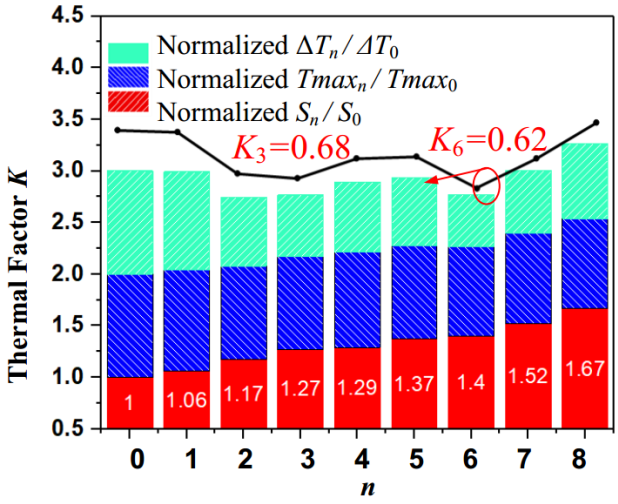
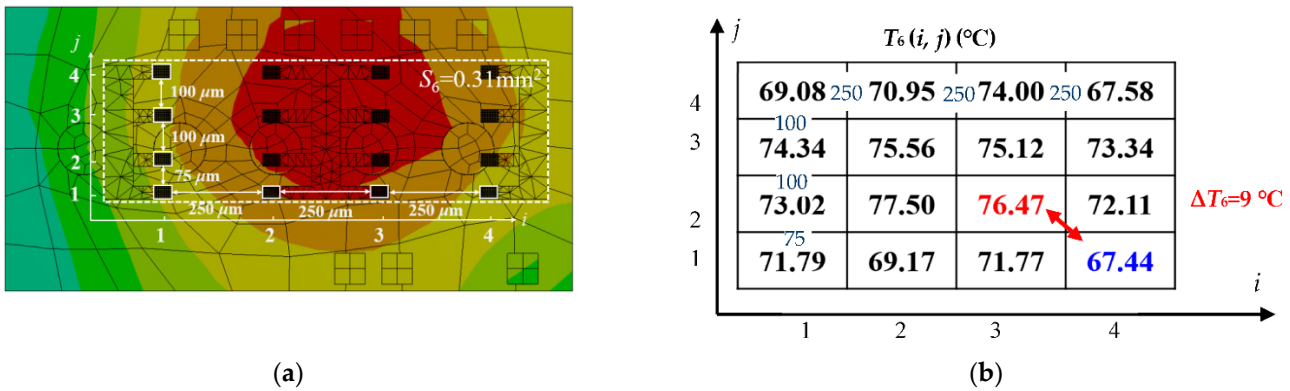


Figure 12. Variation in thermal Factor K in 8 models.



(**a**) (**b**)

Figure 13. (**a**) 6th thermal model; (**b**) Temperature distribution of 6th thermal model.

It is seen that the proposed co-simulation provides a "design-simulation-modeling" optimization method that can improve the performance of electrical parameters and thermal performance of the PA at the same time. The working temperature and temperature

difference between multi-heat sources on the chip can be uniformly reduced with minimum area cost. Compared to the existing electro-thermal co-simulation methods, the proposed method can provide an effective link to different co-optimization methods by feeding back parameters from thermal simulation to electrical simulation.

5. Conclusions

The techniques for the thermal stability of GaAs HBT PA operating in a sub-6G band are illustrated to improve the performance in high temperature. For the PA with the proposed adjustable bias circuit, the error of the PAE and P_O decrease to 3.1% and 0.6 dBm since the temperature is compensated by the 3.5% error ZTAT current. With the multi-source co-simulation, the errors between simulation and measurement decrease to 1% since the thermal resistance of amplifier cells can be calculated accurately. More importantly, a thermal factor K is defined to help reducing the temperature, while saving the area cost. According to the results of iterative modeling, the internal working temperature can be reduced by 10 °C with an increase of 27% in area. It is verified that the proposed methods form an effective co-design model for improving the thermal stability of sub-6G PA.

Author Contributions: Conceptualization, Y.M. and B.L.; methodology, Y.M.; validation, Y.M. and Z.W.; formal analysis, Y.M.; investigation, Y.M. and B.L.; data curation, Y.M. and Z.W.; writing—original draft preparation, Y.M.; writing—review and editing, B.L. and Z.W.; supervision, B.L.; project administration, B.L.; funding acquisition, Z.W. All authors have read and agreed to the published version of the manuscript.

Funding: This work was supported by Key-Area Research and Development Program of Guangdong Province (2019B010143003) and Young Innovation Project of Guangdong Province (2020KQNCX127).

Data Availability Statement: All data included in this study are available upon request by contact with the corresponding author.

Conflicts of Interest: The authors declare no conflict of interest. The funders had no role in the design of the study; in the collection, analyses, or interpretation of data; in the writing of the manuscript, or in the decision to publish the results.

References

1. Chen, K.; Wang, X.; Cheng, X.; Han, J.; Chen, F.; Deng, X. An S-Band GaAs Multifunction Chip for Transmit/Receive Modules. *IEEE Trans. Microw. Theory Tech.* **2020**, *68*, 398–404. [CrossRef]
2. Ozan, S.; Nair, M.; Cappello, T.; Beach, M.A. Low-Noise Amplifier with Wideband Feedforward Linearisation for Mid-Band 5G Receivers. In Proceedings of the IEEE Asia Pacific Conference on Circuits and Systems (APCCAS), Ha Long, Vietnam, 8–10 December 2020; pp. 125–126.
3. Ahn, C.H.; Kim, Y.; Oh, S.; Noh, Y.; Lee, D.H.; Lee, S.; Cho, K.; Kim, J. Design and Realization of Low-Cost 10 W Power Amplifier Module at 7.9–8.4 GHz. *IEICE Electron. Express* **2018**, *15*, 770–775. [CrossRef]
4. Hao, R.; Zhang, X.; Wang, F.; Gao, H.; Cheng, J.; Li, G.P. A fully Integrated Broadband, High-Gain, High-Power and High-Efficiency UHF Amplifier Using GaAs HBT and GaN HEMT. *IEICE Electron. Express* **2017**, *14*, 639. [CrossRef]
5. Li, J.; Qi, Y.; Yu, W.; Li, F.; Shen, P. Temperature Effects in OTA MIMO Measurement. *IEEE Trans. Instrum. Meas.* **2021**, *70*, 1–9. [CrossRef]
6. Huang, A.; Lin, K.H.; Wei, H.Y. Thermal Performance Enhancement with DRX in 5G Millimeter Wave Communication System. *IEEE Access* **2021**, *9*, 34692–34707. [CrossRef]
7. Wang, T.H.; Chen, Y.H.; Chang, C.W.; Li, K.M.; Chen, J.H.; Staudinger, J. On the Thermal Memory Effect Reduction of Power Amplifiers Using Pulse Modulation. *IEEE Microw. Wirel. Compon. Lett.* **2019**, *29*, 285–287. [CrossRef]
8. Alim, M.A.; Chowdhury, A.Z.; Islam, S.; Gaquiere, C.; Crupi, G. Temperature-Sensitivity of Two Microwave HEMT Devices: AlGaAs/GaAs vs. AlGaN/GaN Heterostructures. *Electronics* **2021**, *10*, 1115. [CrossRef]
9. Ma, Y.; Li, B.; Wu, Z.; Wu, H.; Chen, Z. A Co-simulation Method of Power Amplifier for Reliability Optimization. In Proceedings of the IEEE International Conference on Electron Devices and Solid State Circuits (EDSSC), Shenzhen, China, 6–8 June 2018; pp. 1–2.
10. Lai, S.F.; Tam, W.S.; Kok, C.W.; Ng, L.T.; Wong, H. Quiescent Current Control for Low Distortion Linear Power Amplifier. In Proceedings of the IEEE Region 10 Conference, Macao, China, 1–4 November 2015; pp. 1–2.
11. Hassan, Z.; Allec, N.; Fan, Y.; Li, S.; Xuan, Z. Full-Spectrum Spatial–Temporal Dynamic Thermal Analysis for Nanometer-Scale Integrated Circuits. *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.* **2011**, *19*, 2276–2289. [CrossRef]

12. Sun, X.; Gao, H.; Li, G.P.; Sun, W. Peripheral Adaption Power Cell Network for High Efficiency and High Linearity Power Amplifier. *IEEE Microw. Wirel. Compon. Lett.* **2014**, *24*, 799–801. [CrossRef]
13. Tam, W.S.; Wong, O.Y.; Kok, C.W.; Wong, H. A Low Power Temperature Insensitive Voltage Supervisory Circuit in Metal Gate Technology. In Proceedings of the IEEE International Conference of Electron Devices and Solid-State Circuits (EDSSC), Xi'an, China, 25–27 December 2009; pp. 437–438.
14. Souliotis, G.; Plessas, F.; Vlassis, S. A High Accuracy Voltage Reference Generator. *Microelectron. J.* **2018**, *75*, 61–67. [CrossRef]
15. Crupi, F.; Rose, D.R.; Paliy, M.; Lanuzza, M.; Perna, M.; Iannaccone, G. A Portable Class of 3-Transistor Current References with Low-Power Sub-0.5 V Operation. *Int. J. Circuit Theory Appl.* **2018**, *46*, 779–795. [CrossRef]
16. Ramos, F.R.; Mussolini, T.P.; Moreno, R.L.; Pimenta, T.C. A CMOS Temperature-independent Current Reference Optimized for Mixed-Signal Applications. *Integration* **2019**, *66*, 88–95. [CrossRef]
17. Yang, B.D.; Shin, Y.K.; Lee, J.S.; Lee, Y.K.; Ryu, K.C. An Accurate Current Reference Using Temperature and Process Compensation Current Mirror. In Proceedings of the IEEE Asian Solid-State Circuits Conference, Taipei, China, 16–18 November 2009; pp. 241–242.
18. Maxim Integrated. DS2741, Current Monitor and Accumulator with Integrated Sense Resistor Datasheet. 2009. Available online: http://datasheets.maximintegrated.com/en/ds/DS2741.pdf (accessed on 1 July 2009).
19. Tetsuya, H.; Toshimasa, M.; Kenji, T.; Tetsuya, A.; Yoshihito, A. Ultralow-Power Current Reference Circuit with Low Temperature Dependence. *IEICE Trans. Electron.* **2005**, *88*, 1142–1147.
20. Tam, W.S.; Wong, O.Y.; Kok, C.W.; Wong, H. Generating Sub-1V Reference Voltages from a Resistorless CMOS Bandgap Reference Circuit by Using a Piecewise Curvature Temperature Compensation Technique. *Microelectron. Reliab.* **2010**, *50*, 1054–1061. [CrossRef]
21. Perpina, X.; Reverter, F.; Leon, J.; Barajas, E.; Vellvehi, M.; Jorda, X.; Altet, J. Output Power and Gain Monitoring in RF CMOS Class A Power Amplifiers by Thermal Imaging. *IEEE Trans. Instrum. Meas.* **2019**, *68*, 2861–2870. [CrossRef]
22. Jia, L.; Lin, Q.; Wu, H.; Wang, X. Performance Degradation Investigation for a GaAs PHEMT High Gain MMIC PA Taking into Account the Temperature. *Electronics* **2022**, *11*, 1669. [CrossRef]
23. Hollstein, K.; Yang, X.; Weide-Zaage, K. Thermal Analysis of the Design Parameters of a QFN Package Soldered on a PCB Using a Simulation Approach. *Microelectron. Reliab.* **2021**, *120*, 114–118. [CrossRef]
24. Lu, T.; Jin, J. Electrical-Thermal Co-Simulation for Analysis of High-Power RF/Microwave Components. *IEEE Trans. Electromagn. Compat.* **2016**, *59*, 93–102. [CrossRef]
25. Kone, G.A.; Grandchamp, B.; Hainaut, C.; Marc, F.; Maneux, C.; Labat, N.; Zimmer, T.; Nodjiadjim, V.; Riet, M.; Godin, J. Reliability of Submicron InGaAs/InP DHBT Under Thermal and Electrical Stresses. *Microelectron. Reliab.* **2011**, *51*, 1730–1738. [CrossRef]
26. Filippis, S.D.; Kosel, V.; Dibra, D.; Decker, S.; Koeck, H.; Irace, A. ANSYS Based 3D Electro-Thermal Simulations for the Evaluation of Power MOSFETs Robustness. *Microelectron. Reliab.* **2011**, *51*, 1954–1958. [CrossRef]
27. Ozalas, M.T. The Impact of Electro-Thermal Coupling on HBT Power Amplifiers. In Proceedings of the IEEE Compound Semiconductor Integrated Circuit Symposium (CSICS), La Jolla, CA, USA, 19–22 October 2014; pp. 1–2.
28. Korndorfer, F.; Datsuk, A.; Kaynak, M. Layout Based Electro-Thermal Simulation Setup. In Proceedings of the IEEE Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems (SiRF), Anaheim, CA, USA, 14–17 January 2018; pp. 68–69.
29. Mehta, K.; Liu, Y.S.; Wang, J.; Jeong, H.; Yoder, P.D. Thermal Design Considerations for III-N Vertical-Cavity Surface-Emitting Lasers Using Electro-Opto-Thermal Numerical Simulations. *IEEE J. Quantum Electron.* **2019**, *55*, 1. [CrossRef]
30. Yu, W.; Zhuang, H.; Zhang, C.; Hu, G.; Liu, Z. RWCap: A Floating Random Walk Solver for 3-D Capacitance Extraction of Very-Large-Scale Integration Interconnects. *IEEE Trans. Comput. Aided Des. Integr. Circuits Syst.* **2013**, *32*, 353–366. [CrossRef]
31. Chen, Z.; Wong, H.; Yan, H.; Dong, S.; Yang, B.L. Temperature Dependences of Threshold Voltage and Drain-Induced Barrier Lowering in 60 nm Gate Length MOS Transistors. *Microelectron. Reliab.* **2014**, *54*, 1109–1114. [CrossRef]
32. D'Alessandro, V.; Catalano, A.P.; Scognamillo, C.; Codecasa, L.; Zampardi, P. Analysis of Electrothermal Effects in Devices and Arrays in InGaP/GaAs HBT Technology. *Electronics* **2021**, *10*, 757. [CrossRef]