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Design of an Efficient 24–30 GHz GaN MMIC Power Amplifier Using Filter-Based Matching Networks

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Abstract: A broadband GaN MMIC power amplifier (PA) with compact dimensions of 1.94 × 0.83 mm^2 is presented for 5G millimeter-wave communication. To guarantee output capability at the operating band edges where serious performance degradation is likely to occur, the appropriate large-signal matching model and optimal impedance domain need to be carefully determined through load-pull analysis. Broadband matching networks (MNs) in the lowpass form are thereafter developed based on the Chebyshev filter synthesis theory. Using high-pass interstage MN in conjunction with parallel RC lossy circuits to compensate for the transistor's negative gain roll-off slope ensures a flat frequency response. The input MN is designed as a band-pass filter due to the reactance extracted from the input side of the stabilized device exhibiting series LC resonance characteristics. Measured on-wafer pulsed results for the proposed three-stage PA demonstrate up to 30.9 dBm of output power, more than 28.6 dB of small-signal gain, and a peak power-added efficiency (PAE) of 35.6% at 27 GHz. Both uniform gain and saturated output power (P_{sat}) are achieved across 24–30 GHz with fluctuations of less than 0.8 dB.

Keywords: broadband power amplifier; GaN HEMT; high efficiency; load-pull; network synthesis

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1. Introduction

The rapid development of smart cities and the popularity of IoT applications have promoted the widespread deployment of commercial 5G networks, which now mainly operate in sub-6 GHz to provide wide-area signal coverage. However, as new standards and advanced services continue to roll out, sub-6 5G will no longer meet future needs because of its limited low-band resources. In contrast, millimeter-wave (mmW) bands not only possess an abundant spectrum to carry massive wireless connections and deliver huge speed improvements but also feature short wavelengths, which are in line with the trends of telecommunication systems toward large bandwidth, low latency, and miniaturization. The 24–30 GHz frequency range covering the overlapping bands n257, n258, and n261 has been the world's most-utilized 5G mmW spectrum range to date and is attracting extensive attention from researchers. In this context, as a critical building block of the RF front-end, the power amplifier (PA) should have a fractional bandwidth (FBW) of 22% to be compatible with these three bands in order to enhance the integration and reliability of the 5G system while also maintaining good efficiency.

Constrained by the gain–bandwidth product of active devices, proper design strategies need to be adopted to realize a flat gain response and reach a fair compromise between efficiency and output power (P_{out}) over the expected frequency range. According to the target level, the mainstream broadband schemes for PAs reported in the most recent literature can be roughly divided into three categories. In the architecture aspect, the major ones are distributed, balanced, and differential amplifiers that are capable of achieving more than a

one-octave bandwidth via artificial transmission lines, 3 dB couplers, and balun transformers, respectively [1–3]. However, they generally have the evident drawback of bulky size, and some of them could suffer from significant losses or poor efficiency, restricting their use to certain scenarios. Circuit-level methods can be summarized as the parameter solution for matching networks (MNs), among which the simplified real frequency technique (SRFT), based on numerical analysis, utilizes a programmed optimization algorithm to find the network with maximum transducer power gain [4,5]; however, this necessitates the iterative modification of the independent variables to attain global convergence. An analytical approach to filter synthesis allows the construction of MNs with specified bandwidths and suitable passband types depending on the load composition; moreover, complete closed-form solutions can be obtained for simple loads such as RC, RL, or RLC [6–10], making them more flexible and easier to apply compared to the computationally intensive SRFT. As for the device level, negative feedback and reactive/resistive matching effectively alleviate the gain roll-off characteristics of transistors, which offer considerable advantages in terms of cost, space, and complexity [11–14]. From another perspective, reducing the impedance transformation ratio (ITR) of MN is also a valid way to extend the bandwidth. As a representative of third-generation wide-bandgap semiconductors, gallium nitride (GaN) has a higher breakdown electric field, saturated electron drift velocity, and thermal conductivity than Si and GaAs materials; thus, GaN-based devices have outstanding performance in power density, cutoff frequency (f_T), and temperature resistance [15–17]. Meanwhile, their inherent large output resistance, along with small parasitic capacitance, helps to lower ITR without the need for a cascode or stacked configuration, commonly used in CMOS technology [18]. There is no doubt that a GaN high-electron-mobility transistor (HEMT) is the ideal candidate for broadband high-efficiency mmW PA design.

This paper presents a comprehensive procedure for developing a small-scale 1-watt GaN MMIC PA covering the range of 24–30 GHz. On the basis of the derived optimal load impedance and large-signal matching model, two Chebyshev low-pass networks were synthesized for matching at the last stage to yield a balanced P_{out} and reasonable efficiency. Parallel RC lossy networks were employed to stabilize the transistors together with a high-pass MN at every stage to equalize the overall frequency response without sacrificing too much gain. A band-pass filter was designed using closed-form solutions to improve the input return loss over broadband. The proposed PA was fabricated in OMMIC's 0.1 μm GaN-on-Si process, known as D01GH [19]. The experimental results are summarized and compared to those from previously published studies.

2. Circuit Design Considerations

2.1. Choice of Amplifier Topology and Transistor Size

In consideration of the mismatch, transmission loss, process variation, and maximum available gain (MAG) of transistors, a cascaded, three-stage, common-source architecture was employed to achieve a small-signal gain above 26 dB. Next, the unit cell periphery needed to be chosen carefully. Although the larger transistor delivers a higher P_{out}, the lower optimal impedance complicates broadband matching, resulting in higher loss. Moreover, additional parasitics will decrease both the f_T and the maximum oscillation frequency (f_{max}), leading to elevated energy consumption and a deteriorated PAE. Therefore, the total gate width (TGW) of the output stage cell should be set to be smaller under the premise of fulfilling 1 W P_{sat}, which is estimated to be 370 μm when given a 1.25 dBm trade-off margin with a moderate RF power density of 3.6 W/mm. There are three combinations for power cell implementation according to a unit gate width (UGW) $\leq$ 100 μm and a number of gate fingers (NGF) $\leq$ 8 being recommended in the foundry design manual for model accuracy reasons. Since the signal travels along the gate with a steady rise in attenuation and phase shift, and on account of phase differences between the gate fingers, excessive UGW and NGF will both cause a reduction in the forward gain. Table 1 reveals that cells with a minor UGW have better frequency response characteristics for similar TGWs, and the terminal impedances of these cells at the center frequency (f_0) are fairly close to one another. As a

result, the eight-finger HEMT was chosen, and the former ones were subsequently settled following a conservative staging ratio of 1:2. Regarding the soft compression phenomena of GaN-based devices, the first stage cell was slightly enlarged to 50 × 2 µm to enhance the linear driving capability, which seldom impacts the final PAE. The overall class-AB amplifier topology is shown in Figure 1.

Table 1. Simulated f_T, f_{max}, and the terminal impedances of three unit cells with different fingers but similar TGWs (around 370 µm) at the nominal bias conditions of V_{ds} = 12 V and V_{gs} = −1 V, where the maximum device DC and AC transconductance appear.

Transistor Size (µm)	f_T (GHz)	f_{max} (GHz)	Z_{in} @ 27 GHz (Ω)	Z_{out} @ 27 GHz (Ω)
92 × 4	92.8	112	6.6 + j0.6	16.3 − j5
62 × 6	96.3	129.7	5.5 − j1	15.4 − j5.2
46 × 8	100	139.3	5.1 − j1.8	15.1 − j5.3

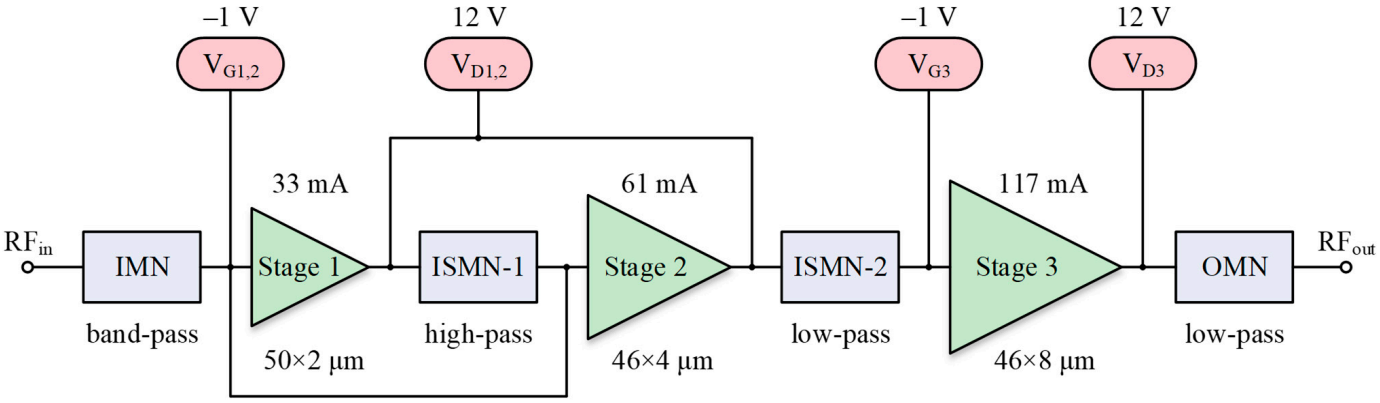

Figure 1. Block diagram of the proposed multistage power amplifier.

2.2. Stability

Due to the high intrinsic gain, active GaN devices are more prone to self-oscillation and can cause circuit failures. Hence, all selected power cells must be adequately stabilized at the very beginning. Figure 2 presents two typical stabilization measures applied at the transistor's input to avoid any power loss, where the reactive/resistive lossy MN in the form of parallel RC ensures in-band stability, whereas the series connection of the stabilizing resistor, R_p, and choke inductor, L_p (or microstrip line, TL_p), merged into the gate bias branch aims to improve the low-frequency stability, and it behaves similarly to an open circuit for the amplification chain, which can be freely connected to point *A* or *B* depending on layout needs. Special attention should be paid to whether the self-resonant frequency (f_{SR}) of the MIM capacitor, C_s, falls within or below the operating band, as the resulting RF short circuit may trigger potential instability, leading the parallel RC network to lose its role in both stabilization and gain equalization. Furthermore, the inevitable electromagnetic (EM) coupling from the surrounding environment will shift the f_{SR} of the C_s to lower frequencies [2], for which we can split the C_s into two identical square-shaped capacitors connected on both sides of the R_s in parallel so that the parasitic inductance of the capacitor plates can be minimized. In addition, the symmetrical layout contributes to the signal transmission consistency and realizes the input balance of the transistor.

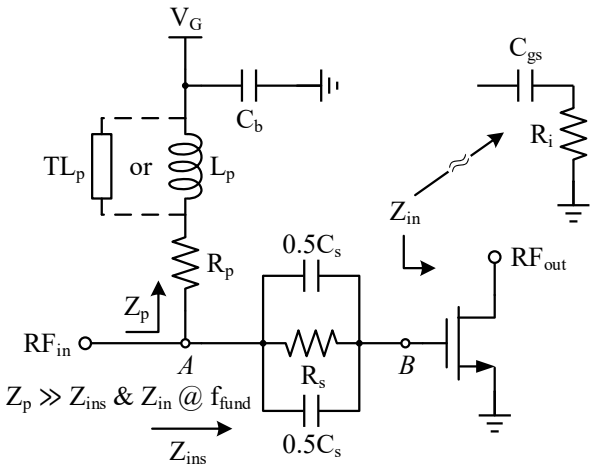

Figure 2. Schematic of the stabilized transistor.

To quantify the impact of the RC stabilization network on the matching bandwidth, using Equations (1) and (2), the channel resistance, R_i, and the depletion capacitance, C_{gs}, of the 46 × 8 µm cell are found to be 5.3 Ω and 0.655 pF, respectively, extracted from the S-parameter simulation at f_0 (27 GHz) based on the simplified hybrid-π model of a FET [13].

$$R_i = \mathrm{Re}\left(\frac{1}{y_{11}+y_{12}}\right) \tag{1}$$

$$C_{gs} = \left[-\omega \mathrm{Im}\left(\frac{1}{y_{11}+y_{12}}\right)\right]^{-1} \tag{2}$$

Omitting the negligible C_{gd} for simplicity, the individual cell is treated as a unilateral two-port network whose input impedance, Z_{in}, translates into a series combination of R_i and C_{gs}, as depicted in Figure 2. Suppose the input impedance of a HEMT after stabilization viewed from point A is Z_{ins}, then:

$$Z_{ins} = \frac{1}{1/R_s + j\omega C_s} + Z_{in} \tag{3}$$

$$Q_{ins} = \left(\frac{1}{\omega R_i C_{gs}}\right)\left[\frac{1+\omega^2 R_s^2 C_s\left(C_s+C_{gs}\right)}{1+\left(\omega R_s C_s\right)^2 + R_s/R_i}\right] \tag{4}$$

$$Q_{in} = \frac{1}{\omega R_i C_{gs}} \tag{5}$$

$$\frac{Q_{ins}}{Q_{in}} = \frac{1+\omega^2 R_s^2 C_s\left(C_s+C_{gs}\right)}{1+\left(\omega R_s C_s\right)^2 + R_s/R_i} \tag{6}$$

From Equations (5) and (6), at f_0, the quality factor Q of Z_{in} (i.e., Q_{in}) is 1.7, and the Q of Z_{ins} (i.e., Q_{ins}) will be larger than Q_{in} when $(R_sC_s) > 10^{-11}$, meaning that the maximum attainable bandwidth will be reduced after the insertion of a parallel RC network, which may be true for gain concerns. Fortunately, the upper limit of Q is 2.7 according to $Q = f_0/\mathrm{BW}$, with a conservatively designed bandwidth of 10 GHz. In fact, there is enough room for us to achieve the desired compromise between stability, bandwidth, and gain under the obtained boundary condition. We finally chose a stabilization network consisting of two identical 0.68 pF capacitors in parallel with a 30 Ω resistor for the output stage cell, with a Q_{ins} of 2.24 determined by Equation (4). In addition, by substituting the reactance X slopes of the two curves in Figure 3 at f_{SR} into Equation (7), it is found that

the series parasitic inductance represented by the C-R-C structure is reduced by half, from 21.2–9.6 pH, compared to the conventional R-C one, thereby boosting the f_{SR} to 44.6 GHz.

$$\left.\frac{\partial X}{\partial f}\right|_{f_{SR}} = 2\pi \frac{\partial}{\partial \omega}\left(\omega L - \frac{1}{\omega C}\right)\Bigg|_{\omega_{SR}} = 4\pi L \tag{7}$$

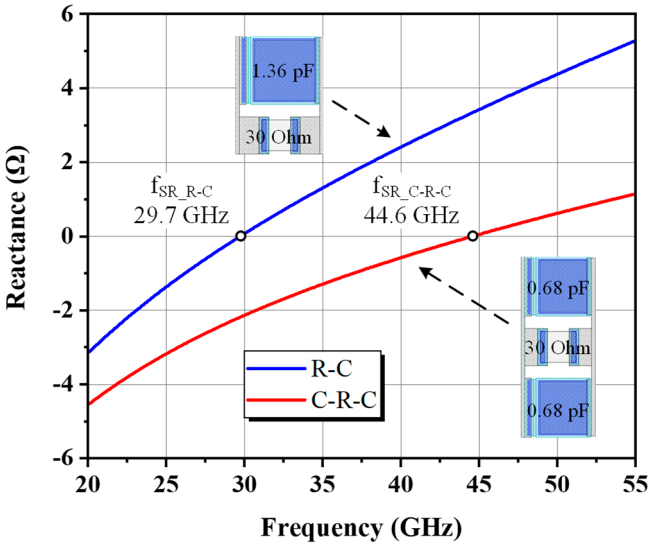

Figure 3. The reactance of a parallel RC stabilization network.

Figure 4 shows that the Rollett stability factor (K) > 1 is achieved throughout nearly the whole band at the expense of less than 0.9 dB of gain loss. Despite the instability still existing at frequencies below 1 GHz, this problem is solved naturally when considering the losses and filtering functions of all passive networks.

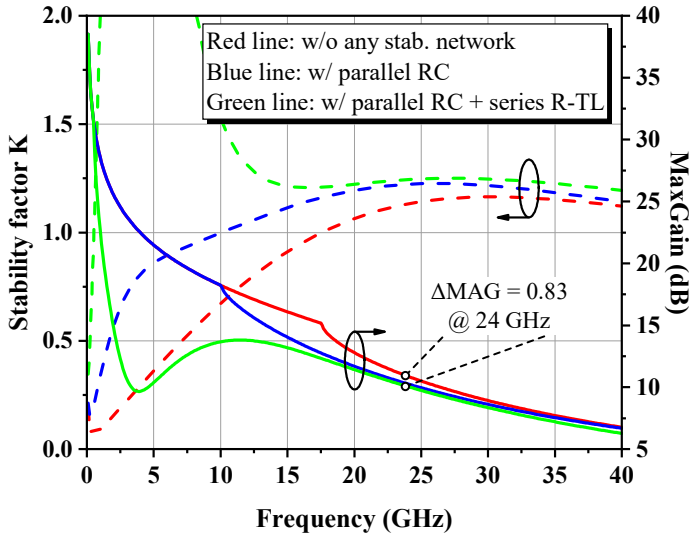

Figure 4. Simulated K-factor and MAG of the 46 × 8 µm GaN transistor, with and without stabilization networks.

2.3. Load-Pull Analysis and Optimal Impedances Selection

Achieving the continuous and accurate matching of frequency-dependent impedance over broadband is a challenge. On top of that, the designed band usually deviates from evaluation to a lower frequency after implementation, and severe performance degradation tends to happen near the operating band edges, especially at the upper-frequency corner,

where gain roll-off issues are highlighted. Therefore, the single-tone load-pull procedures of the stabilized 46 × 8 µm cell were carried out at 24 GHz, 28 GHz, and the extended corner of 32 GHz, while the input was terminated on the conjugate matching condition to determine the tolerance zone, satisfying the preset goal of PAE ≥ 40% and P_{1dB} ≥ 31 dBm to secure the specifications safely. Harmonic control was deliberately neglected since it complicates the MN, and the higher-order harmonic components are far from a passband that can be readily filtered out. From Figure 5a, we can observe that, due to the nonlinear output capacitance, C_{out}, both the PAE and P_{1dB} contours for load impedances move counterclockwise and narrow with increasing frequency, with the PAE contour shrinking more dramatically, indicating that C_{out}'s effect on PAE is significant at high frequencies and that the optimal impedance domain defined by the overlapping portion (shaded) of the three sets of contours is primarily bounded by the contours at 32 GHz. Consequently, we chose 11 + j13 Ω as the optimal center load impedance, $Z_{L,opt}$, close to the impedance points with maximum PAE at high fundamentals. In this way, a wider bandwidth can be produced by intentionally introducing a certain degree of mismatch on the low-frequency side while the high-frequency performance is strengthened.

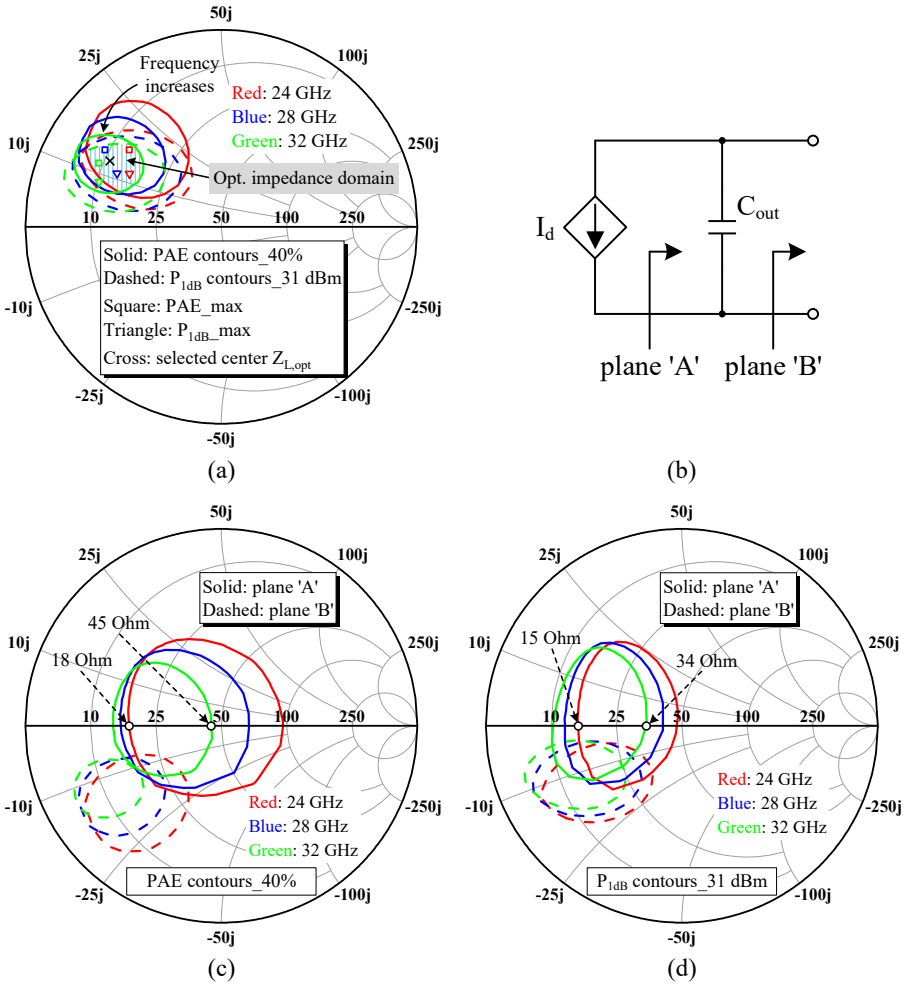

Figure 5. (**a**) Load-pull simulations at 1 dB gain compression. (**b**) Reference planes for the equivalent circuit of the transistor. (**c**,**d**) Extracted PAE and P_{1dB} contours at plane 'A.'

For subsequent analyses and the design of broadband MNs, we needed to derive the parallel $R_{out}C_{out}$ model for the large-signal output impedance of the cell, in which the extraction of C_{out} is particularly vital. Assume that the load-pull simulation is performed at the transistor's internal current source, i.e., reference plane 'A' in Figure 5b; the resulting contour will become frequency-independent regardless of any parasitic reactance, and its

center will fall on the real axis of the Smith chart, implying that the ideal closed contour will be bisected by the real axis [20]. Based on this conclusion, we can use Equation (8) to calculate the shunt capacitance, C_p, corresponding to the conjugate of $Z_{L,opt}$ and take it as an initial guess for C_{out} (0.26 pF @ 28 GHz); then, we can try de-embedding different C_{out} values from the load-pull contours derived at plane 'B' one by one in steps of 0.01 pF. When the extracted efficiency and power contours are shifted back to the position symmetrical to the real axis [18], as illustrated in Figure 5c,d, the C_{out} is identified to be 0.27 pF. Additionally, the acceptable load resistance R_L ranges between 18 and 34 Ω.

$$Y^*_{L,opt} = \frac{1}{Z^*_{L,opt}} = \frac{1}{R_p} + j\omega C_p \tag{8}$$

Since impedance matching must comply with the Bode–Fano criterion and R_L is much smaller than the HEMT's output resistance $1/G_{ds}$, we have

$$\Delta\omega \ln\left|\frac{1}{\Gamma_m}\right| \le \frac{\pi}{R_{out}C_{out}} = \frac{\pi}{\left(\frac{R_L}{1+R_L G_{ds}}\right)C_{out}} \approx \frac{\pi}{R_L C_{out}} \tag{9}$$

Under a known bandwidth, $\Delta\omega$, and C_{out}, the chosen R_L should be as small as possible to minimize the reflection coefficient, $|\Gamma_m|$, but this will increase the ITR and is not beneficial for achieving uniform broadband output performance; thus, we compromised by setting R_L to the range's median value: 26 Ω.

For the input stage device, the priority of which is to provide sufficient driving power, the preferred $Z_{L,opt}$ was selected through a simultaneous conjugate matching simulation so that the device could obtain excellent power gain within the target band. Table 2 lists the optimal load impedance of each stage as well as the output parallel RC model parameters extracted from the load-pull simulations.

Table 2. Optimal load impedances and the values of large-signal output matching models.

HEMT (μm)	$Z_{L,opt}$ (Ω)	R_L (Ω)	C_{out} (pF)
46 × 8	11 + j13	26	0.27
46 × 4	21 + j31	75	0.13
50 × 2	36 + j57	/	/

3. Design and Implementation of Matching Networks

3.1. Low-Pass OMN Synthesis and Mixed-Element Implementation

Designing a wideband output matching network (OMN) should consider not only in-band matters but also suppress harmonic distortion. Herein, we adopted a low-pass filter structure that provides a Chebyshev impedance match. On the other hand, bearing in mind that the discontinuity interaction and mutual coupling between adjacent elements will obviously affect the frequency response of compact MNs at mmW, while rigorous EM simulation is extremely time-consuming yet essential, the schematic design was alternated with layout replacement to lessen the risk of unmitigated performance deviations and laborious adjustments when cascading all of them into a complete amplifier.

To start with, the influence of the L-type MN composed of a 1.8 pF DC-block capacitor and the parasitic shunt capacitor of the RF signal pad on an external 50 Ω load at both the input and output terminations was compensated by a high-impedance microstrip line to 48 Ω at 27 GHz. At least two sections of the LC ladder are needed for the Chebyshev filter-based OMN to achieve a transformation ratio of 4.4:1 throughout the target band with a passband ripple less than 0.1 dB, as expressed theoretically in [6]. To facilitate the determination of the normalized g elements through the look-up table, we set the impedance transformation ratio, r, as 4 and the FBW as 0.4 to ensure a sufficient design margin. The

generated fourth-order low-pass prototype shown in Figure 6a can be converted into a specific network by inverse normalization Equations (10) and (11).

$$L_n = \frac{g_{2n-1}}{\omega_0}\frac{R_{load}}{r} \tag{10}$$

$$C_n = \frac{g_{2n}}{\omega_0}\frac{r}{R_{load}} \tag{11}$$

where R_{load} and ω_0 refer to the desired terminal resistance and center angular frequency, respectively. The preliminarily obtained real-to-real network scaled from 48 Ω to an intermediate impedance of 12 Ω was then turned into a real-to-complex network to finalize the broadband matching to our desired $Z_{L,opt}$ with the automatic optimizer in Advanced Design System (ADS) [8]. Figure 6b shows the resulting MN with the element values listed in Table 3.

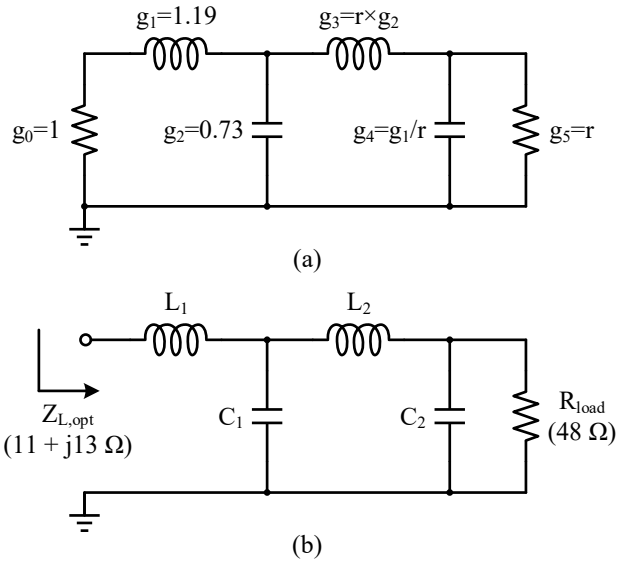

Figure 6. Two-section low-pass MN: (**a**) normalized prototype; (**b**) real-to-complex impedance transformer.

Table 3. Design parameters for the low-pass OMN.

Elements	*g* (*r* = 4, FBW = 0.4)	Real-to-Real (48 Ω to 12 Ω)	Real-to-Complex (48 Ω to 11 + j13 Ω)
L_1	1.19	84 pH	157 pH
C_1	0.73	0.36 pF	0.4 pF
L_2	2.92	206 pH	203 pH
C_2	0.3	0.15 pF	0.17 pF

Considering the feasibility of physical implementation and layout convenience, we directly employed MIM capacitors instead of low-impedance stubs or fan-shaped branches paired with microstrip lines to approximate the ideal lumped elements in the synthesized circuit to construct a mixed-element network. The inductors were replaced by transmission-line sections with a high characteristic impedance, Z_0, and a short electrical length, θ, the equivalent series reactance, X, of which is roughly linear to ω, that is:

$$X = Z_0 \sin\theta \approx \omega L \tag{12}$$

Narrow microstrip lines were applied in the design to reduce the footprint. Except for the line width in OMN, which is 15 μm, the rest are 10 μm. The supply traces of drain bias and OMN used a double-layer metal to sustain higher current densities and reduce

ohmic loss, respectively. In addition, to prevent discontinuity during bending, 45-degree microstrip lines with perpendicular access lines were adopted at the corners.

Figure 7 shows that the input reflection coefficient of OMN rotates clockwise with increasing frequency in the previously determined optimal impedance domain and forms a knot at 24–31.5 GHz, while the second harmonic impedance varies along the periphery of the Smith chart. Moreover, the impedance at 32 GHz highly coincides with $Z_{L,opt}$, which guarantees the PAE level at high frequencies.

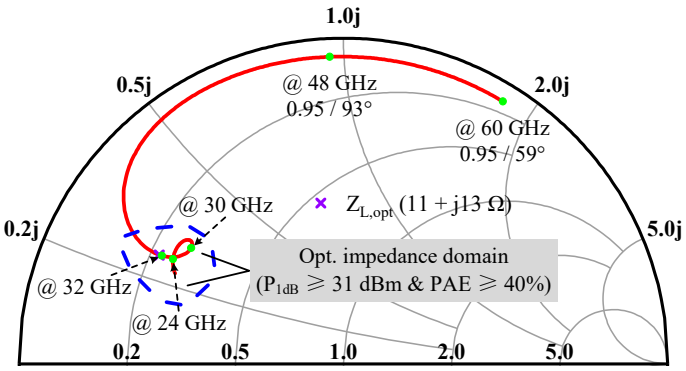

Figure 7. Simulated S_{11} of OMN in EM layout format.

3.2. Source-Pull Analysis and Low-Pass ISMN-2 Synthesis

Since the input and output impedances of the cell are somewhat correlated, reacquiring the optimal source impedance, $Z_{S,opt}$, when loaded with the established OMN allows the cell to run in a better state. It should be mentioned that an even-order harmonic short circuit composed of open and shorted $\lambda/8$ stubs with the same characteristic impedance, Z_1, in parallel was used as the gate bias for the 46×8 µm cell described in Figure 8. The equivalent input impedance, $Z_{\lambda/8-stubs}$, at the central node, a, can be expressed as Equation (13), which indicates that the present structure not only has the same function of the conventional quarter-wave short-circuit stub but also greatly improves layout utilization by dividing the lengthy $\lambda/4$ line in half and arranging them on the upper and lower sides of the chip.

$$Z_{\lambda/8-stubs}(f) = \frac{1}{2} j Z_1 \tan\left(\frac{\pi}{2} \cdot \frac{f}{f_{fund}}\right) \tag{13}$$

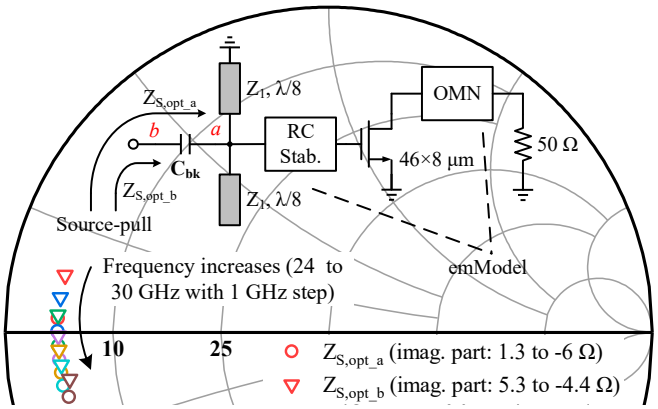

Figure 8. Optimal input impedances extracted from source-pull simulations.

The source-pull simulations performed at P_{1dB} were repeated within the band of interest at node a to determine the trajectory of Z_{S,opt_a}, as shown in Figure 8, and we noticed they spread across the upper and lower half-planes of the Smith chart. After adding the series 0.73 pF capacitor, C_{bk}, an updated trajectory with axisymmetric attributes was

obtained at node *b*. The real and imaginary parts of the resulting Z_{S,opt_b} vary within a small range, from 4.4 to 5.2 Ω and from 5.3 to −4.4 Ω, respectively. Hence, the interstage matching network between the second and third stages (ISMN-2) can be regarded as a real impedance transformation from 5 to 75 Ω. Unlike the OMN, where the effect of C_{out} needs to be canceled out, here, C_{out} will be exploited to participate in matching, which helps to tackle the design challenge of achieving broadband matching with a large ITR. Likewise, we also referred to the data tabulated in [6], and the Chebyshev low-pass prototype of a 15:1 impedance transformer with 40% FBW was applied and scaled to the 50 Ω system and 27 GHz center frequency in an analogous manner, as illustrated in Figure 9.

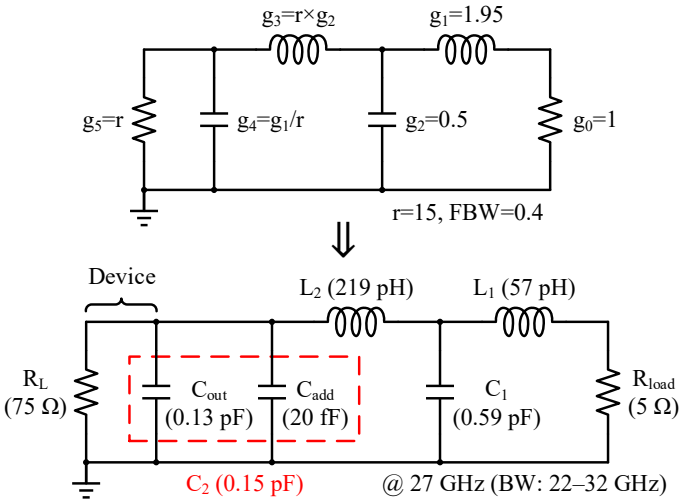

Figure 9. Conversion from a 0.1 dB equal-ripple low-pass filter prototype to a denormalized network.

After replacing the ISMN-2 into a layout and cascading it with corresponding cells and OMN, we evaluated the total losses associated with each MN, including mismatch and dissipative loss, by injecting a fixed low-power stimulus signal to the interstage cell and calculating the power difference between their input and output ports. The simulation results are displayed in Figure 10. OMN loss increases monotonically in the designed band, with the maximum value not exceeding 1 dB, while the loss curve of ISMN-2 follows a decreasing and then increasing trend, with the valley point located at 29 GHz, and the sum of all losses introduced by both is controlled within the range of 2–2.4 dB. Since the design of the latter two MNs emphasizes achieving better P_{out} and PAE metrics, compensation for the transistor's gain roll-off is very limited.

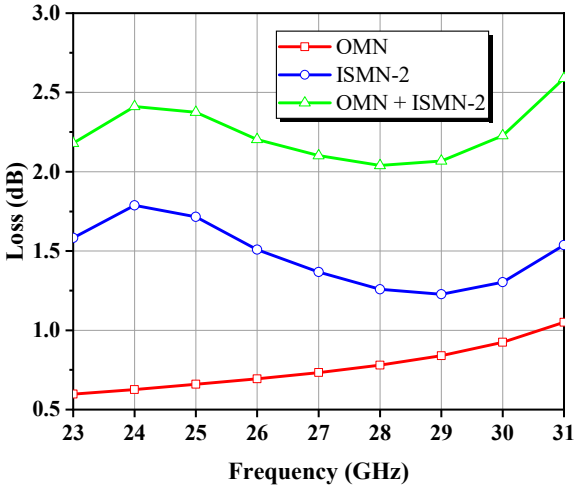

Figure 10. Estimated total losses for the MNs.

3.3. Compact High-Pass ISMN-1 Design

To dampen the strong low-frequency gain while compensating for the high-frequency response, a two-section high-pass structure was adopted for the interstage matching network between the first and second stages (ISMN-1), and the entire course of impedance transformation was visually proceeded by means of the Smith chart with a constant-Q circle without the extra consideration of DC blocking. The drain feeder was involved in matching to save area. As shown in Figure 11a, Z_n ($n = 0, 1, \ldots, 5$) denotes the impedance looking toward the output end after adding the nth element in sequence. This was determined by Equation (14), where Γ_n is the simulated reflection coefficient at the terminated 50 Ω reference load connected to the corresponding node, n (blue square). As can be clearly seen from Figure 11b, the impedance profile (Z_2–Z_5) is rather sensitive to each matching piece, and because of the tight layout of the high-pass network, these elements' placements and parameters were decided after careful 2.5D EM simulations (ADS Momentum) and comparisons. It is worth mentioning that the value of 4.5 that was chosen to represent the maximum Q is basically defined by the initial Z_0, which is equal to the center frequency divided by the required bandwidth. The final curved trajectory, Z_5, sandwiches $Z_{L,opt}$ in the middle, creating a knot with a broadband matching nature.

$$Z_n = 50\frac{1+\Gamma_n}{1-\Gamma_n} \tag{14}$$

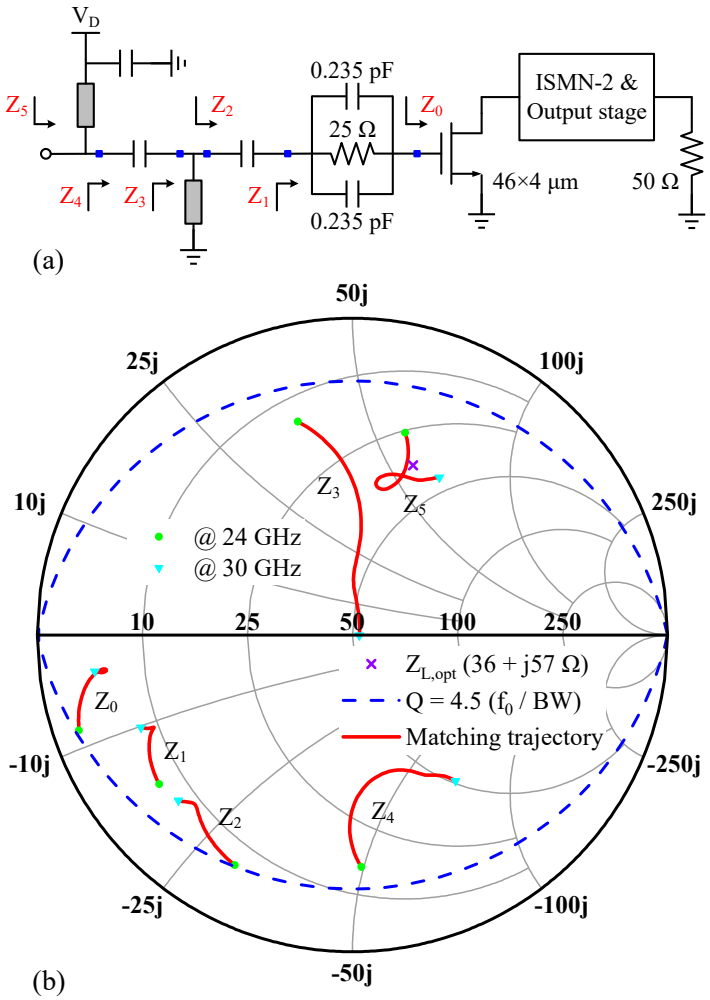

Figure 11. (**a**) Schematic of the ISMN-1. (**b**) Matching trajectory along the ISMN-1 within the 24–30 GHz bandwidth.

3.4. Input Impedance Model and Band-Pass IMN Synthesis

The input impedance, Z_{in}, of the first stage cell with stabilization circuits is plotted in Figure 12a and is represented by the red line. As the frequency increases, Z_{in} moves up along the resistance circle of 12.4 Ω within the range of 26–30 GHz, which can be considered as a series RLC resonant circuit, where the inductance and capacitance values were determined to be 275 pH and 82 fF, respectively. Although this model does not fit well with the variation trends observed in Z_{in} at lower frequencies, owing to irregular changes in the real part of Z_{in} over the band revealed in Figure 12b, it is in good agreement with the imaginary part of Z_{in}, and, as such, we can conclude that LC resonance is the most dominant form of Z_{in}'s reactance.

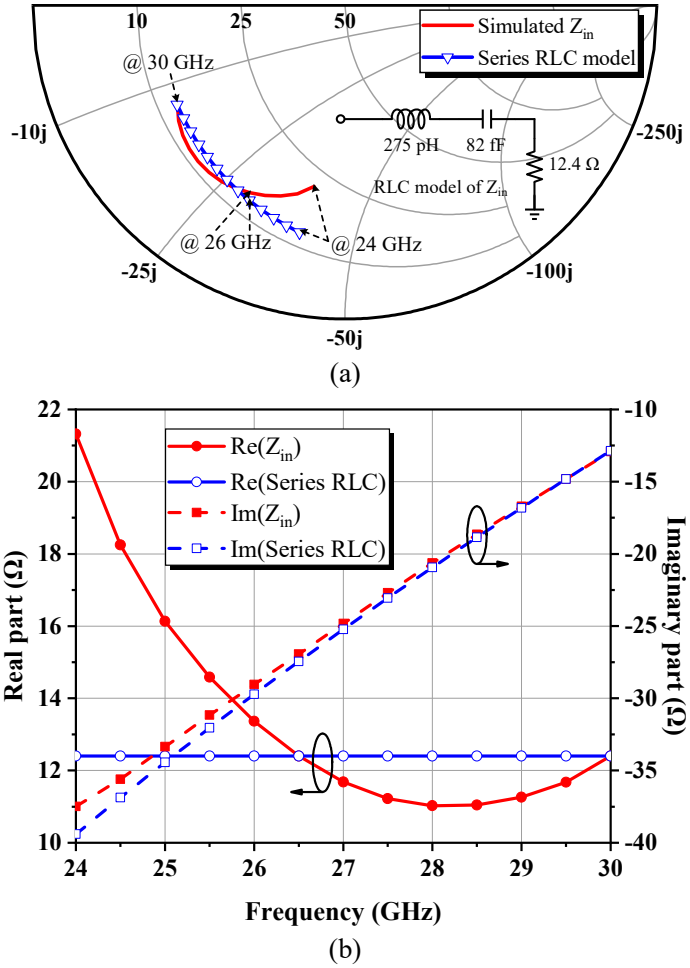

Figure 12. (**a**) Simulated S_{11} of the stabilized 50 × 2 μm cell and series RLC equivalent circuit. (**b**) Comparison of the real and imaginary parts of Z_{in} and RLC model circuit impedance.

Because the primary objective of the input matching network (IMN) is to improve the return loss in broadband, as long as the reactive component is fully absorbed, the transformation from a designated input impedance to the standard 50 Ω can be achieved precisely, indicating that the best matching topology is the band-pass structure; thus, we adopted closed-form solutions [7] to accomplish the design. Nevertheless, the band-pass network requires twice the number of elements as the low-pass form, a second-order band-pass filter with a target band of 22 to 32 GHz was therefore built to accommodate the practical 6 GHz bandwidth demand. The quality factor, Q, of IMN depends on the series RLC model circuit, which can be obtained from the formula $\omega_0 L/R$ or $1/(\omega_0 RC)$, where the larger solution result, i.e., Q = 5.9, was taken as the design parameter, and ω_0 is the geometric mean angular frequency. The detailed IMN design steps are shown in Figure 13.

After the low-pass prototype is derived, each series or shunt element is converted into a band-pass network via resonation at ω_0, and L_{add} complements the resonant inductance in the model circuit. The Norton transformation acts as an ideal transformer, enabling the up-conversion of R_L from 30.3 to 48 Ω without altering the bandwidth. It should be noted that the frequency response represented by Z_{in} and its equivalent model in the low-frequency range of 24–26 GHz demonstrates a relatively large divergence. Hence, the synthesized band-pass network needs to be further tweaked for actual Z_{in} with some sort of compromise.

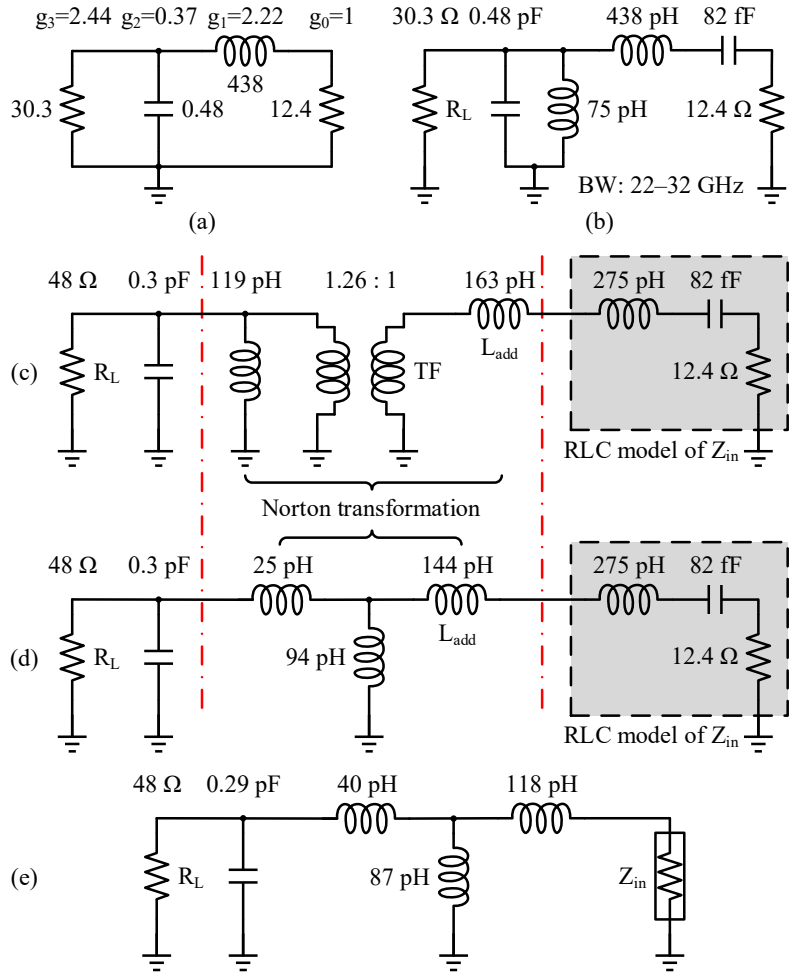

Figure 13. IMN design flow: (**a**) low-pass prototype; (**b**) band-pass version; (**c**) upward impedance transformation of R_L to 48 Ω; (**d**) Norton transformation to remove the ideal transformer; (**e**) optimized band-pass network.

Afterward, the stagger-tuning technique was undertaken to optimize the insertion loss of each MN according to their passband properties; the broadband gain response was able to be achieved eventually. To thoroughly check the overall stability of the PA before tape-out, we conducted a series of EM/circuit co-simulations in the wide frequency region from DC to 100 GHz for various possible situations, including different bias voltages and power excitation. The case encountered that μ was less than unity in the 4.9–6.2 GHz range, as shown in Figure 14. Even though the stability of all unit cells was well assured in advance, the shared unilateral supplies, parasitic feedback loops, and coupling effects caused by the compact layout still triggered the formation of new potential instability in the cascaded circuit. Because of this, a 30 Ω resistor, R_b, was added in series with the 3 pF bypass capacitor in both the gate and drain bias paths of the driver stage to eliminate unfavorable oscillations. Figure 15 presents the final schematic of the designed broadband PA.

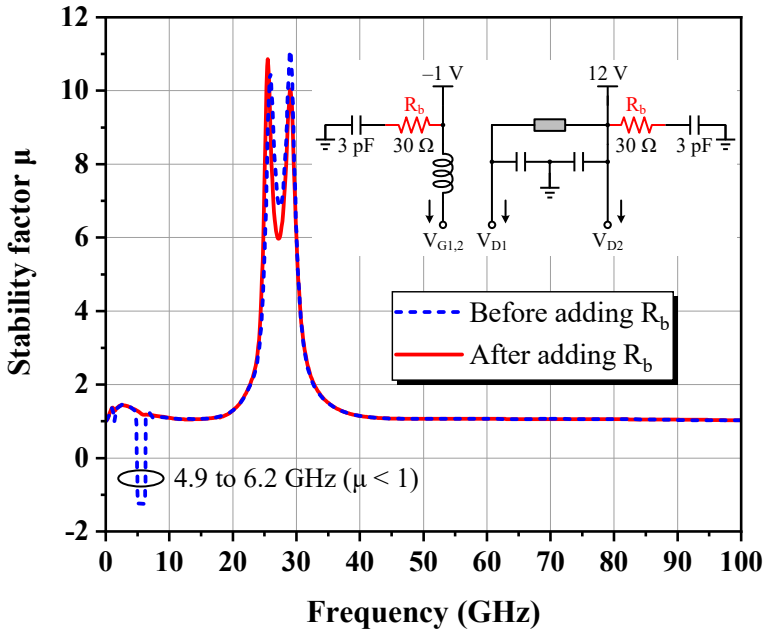

Figure 14. Stability factor μ before and after adding the R_b.

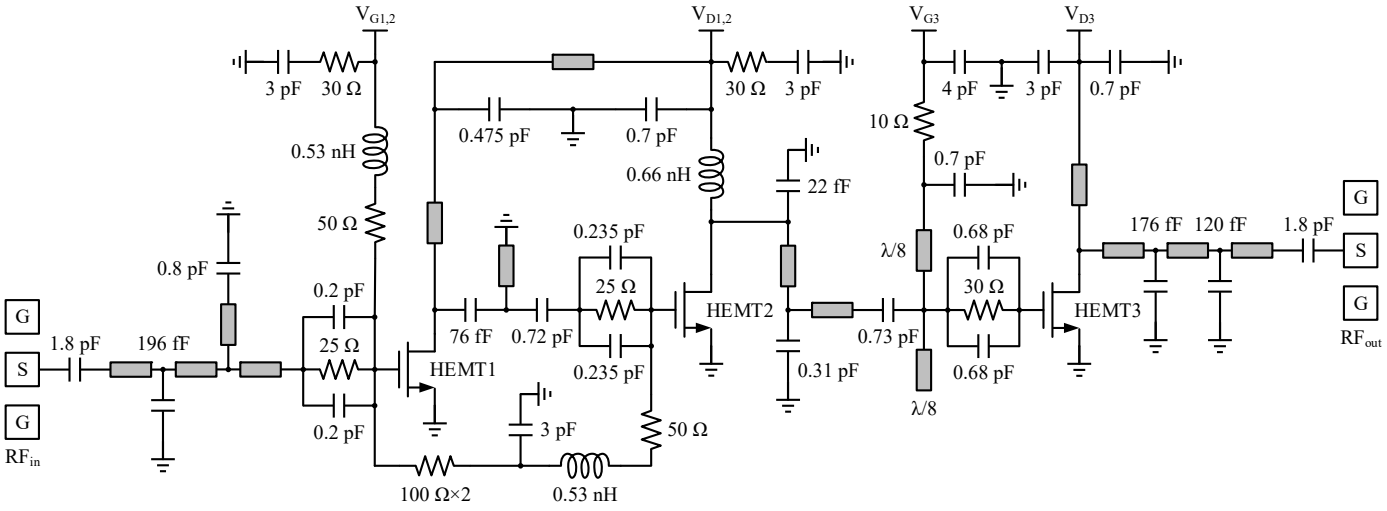

Figure 15. Complete schematic of the three-stage PA.

4. Measurement Results

Figure 16 shows the proposed MMIC PA fabricated with the industrial 100 nm double heterojunction AlN/GaN/AlGaN HEMT process on a high-resistivity (5 kΩ/cm), 100-μm-thick silicon substrate. Under a 12 V pulsed supply with a 5% duty cycle (200 μs pulse width, 4 ms period) for drains of all stages to avoid overheating during continuous on-wafer testing, as the thermal contact of the chip's backside on the heat sink is poor, the gate bias voltage was slowly raised from the −1.5 V threshold level until the quiescent current draw reached 211 mA, consistent with the simulation environment.

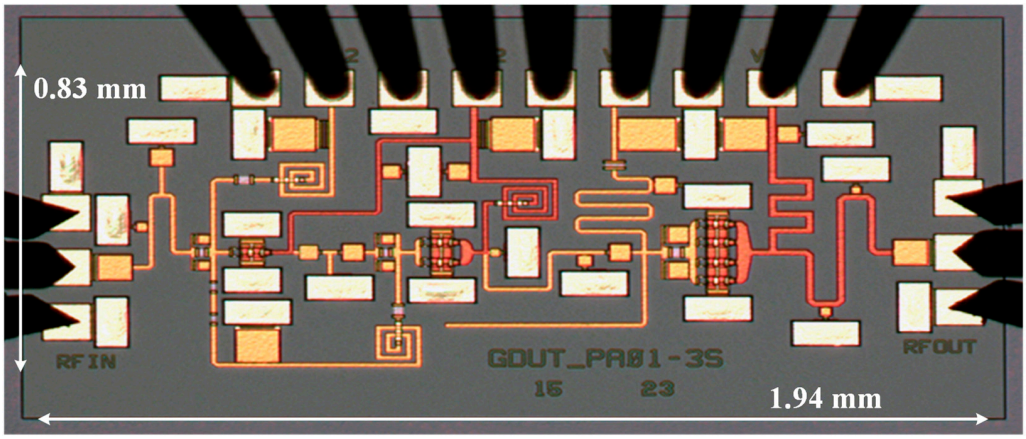

Figure 16. Die microphotograph of the 24–30 GHz GaN MMIC PA.

4.1. Small-Signal Characterization

After calibrating out the losses of coax cables and GSG probes (150 µm pitch), Figure 17 exhibits that the measured input and output return loss are both greater than 10.5 dB, as well as a linear gain exceeding 28.6 dB over 24–30 GHz with 0.8 dB total variation. The pulsed test outcomes recorded by a vector network analyzer (Keysight N5245A PNA-X) agree nicely with simulations in continuous-wave (CW) mode, with the exception of S_{21}, which is higher than predicted from 23.5 GHz onwards. Moreover, no oscillations arise, and the out-of-band gain drops substantially as intended thanks to the filter-based MNs; such band selectivity eases the later transmitter build-up.

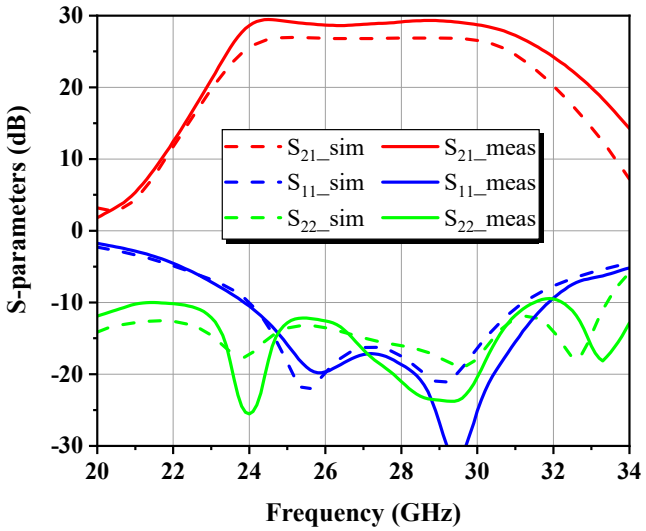

Figure 17. S-parameters of the proposed PA.

4.2. Large-Signal Characterization

Figures 18 and 19 show that P_{4dB} is beyond 30 dBm, P_{sat} ranges from 30.5–30.9 dBm, and the PAE at P_{4dB} reaches 30.6%–34.7% across the band of interest at room temperature. Power sweep characteristic curves at three discrete frequencies are plotted in Figure 20, where the maximum PAE approaches 35.6% found in the vicinity of P_{6dB} at 27 GHz, and PAE peaks at other frequency points occur at around 4 dB of gain compression. The total current consumption grows to about 288–320 mA when the PA is driven into saturation.

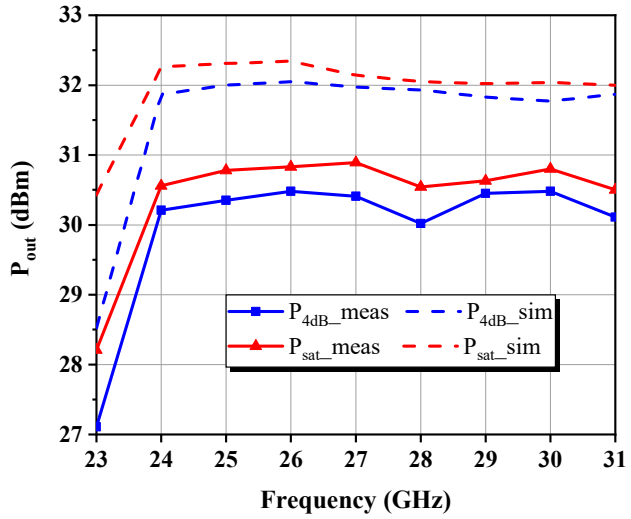

Figure 18. Measured and simulated P_{out} at 4 dB gain compression and in the saturation state.

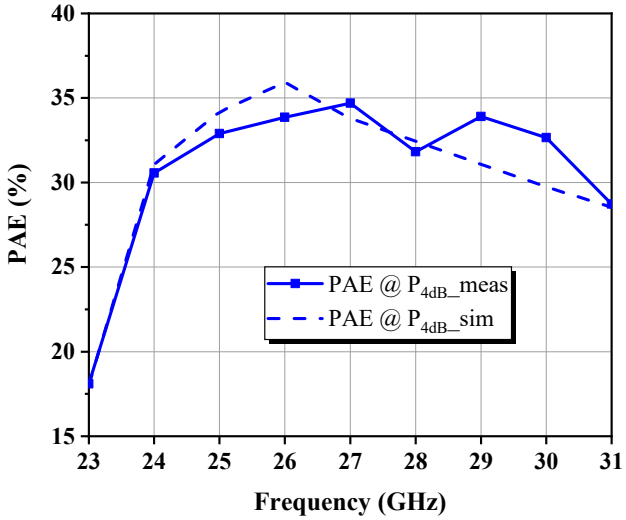

Figure 19. Measured and simulated PAE at P_{4dB} versus frequency.

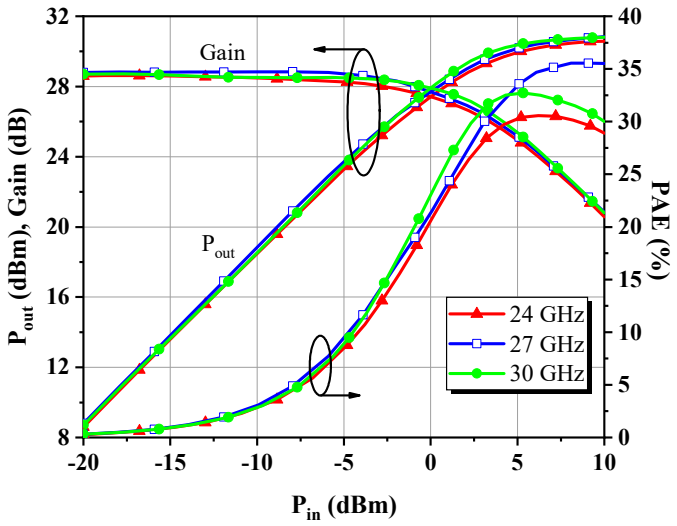

Figure 20. Measured P_{out}, PAE, and gain behaviors with respect to input power at 24, 27, and 30 GHz.

The discrepancies between the measured and simulated data mainly come from the accuracy of the transistor nonlinear electro-thermal model, self-heating from the finger dissipation, manufacturing errors in MIM capacitors, and the quality of the probe card contact. The experimental performances are summarized and compared to previously reported GaN PAs with similar frequency bands in Table 4.

Table 4. Performance summary and comparisons with previous works.

Ref.	[13]	[16]	[17]	[19]	TGA2594 [21]	APN244 [22]	This Work
Process	0.1 μm GaN/Si	0.1 μm GaN/SiC	0.15 μm GaN/SiC	0.1 μm GaN/Si	0.15 μm GaN/SiC	0.2 μm GaN/SiC	0.1 μm GaN/Si
V_D (V)	12	15	20	12	20	28	12
Meas. mode	Pulsed	Pulsed	CW	Pulsed	CW	Pulsed	Pulsed
Freq. (GHz) (FBW)	22–27 (20.4%)	27–34 (23%)	32–38 (17.1%)	24–30 (22.2%)	27–31 (13.8%)	24–28 (15.4%)	24–30 (22.2%)
Gain (dB)	24 ± 0.5	20.5 ± 1.5	17 ± 0.5	17.9 ± 1.5	23.6 ± 1.9	20 ± 0.5	29 ± 0.4
P_{out} (dBm)	31 ± 0.7	38.7 ± 0.4	36.7 ± 0.5	39.9 ± 1	37 ± 0.4	38.6 ± 0.5	30.7 ± 0.2
PAE (%)	30.5–36.9 [a]	24.5–30.5 [b]	25–34 [c]	24–37 [a]	26.5–30.3 [c]	30.8–32.6 [a]	30.6–34.7 [b]
Size (mm^2)	1.8 × 0.87	4.5 × 3.5	2.22 × 1.6	3.7 × 3.2	3.24 × 1.74	3.3 × 1.95	1.94 × 0.83

[a] PAE @ saturated output power. [b] PAE @ specific gain compression point. [c] PAE @ specific input drive.

5. Conclusions

This paper demonstrates a fully integrated 1-watt GaN MMIC PA for the 24–30 GHz band. Key design considerations related to cell selection, stability issues, and optimal impedance extraction are discussed. The output MN, designed using a network synthesis approach incorporating CAD-based post-optimization, caused the transformed trajectory to rotate around the target load in the optimal impedance domain to ensure broadband output performance. The introduction of lossy matching in the form of parallel RC at each stage, combined with a high-pass interstage MN, largely compensated for the transistor's gain roll-off. A band-pass filter was adopted for the input MN to absorb the reactive component of the input impedance, thus producing a wideband frequency response. Benefiting from the arrangement of two interstage MNs with opposite passband properties, the joint-tuning freedom for smooth gain is greatly enhanced. The implemented three-stage PA occupies a small area of 1.61 mm^2 and exhibits good gain flatness and output power uniformity, with a PAE of up to 35.6% in the operating band. The measurement results indicate the suitability of the proposed compact broadband PA for 5G mmW applications.

Author Contributions: Conceptualization, L.P.; methodology, L.P.; software, L.P.; validation, L.P.; data curation, L.P. and J.C.; writing—original draft preparation, L.P.; writing—review and editing, Z.Z.; visualization, L.P.; supervision, G.Z.; project administration, Z.Z. and G.Z.; funding acquisition, G.Z. All authors have read and agreed to the published version of the manuscript.

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Conflicts of Interest: The authors declare no conflict of interest.

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