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The Impact of an Extended Gate Field Plate on the DC and RF Characteristics of a Junctionless Thin-Film Transistor

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Abstract: In this work, conventional and drain offset junctionless (JL) finlike thin-film transistors (FinTFTs) with and without extended gate field plate (E-GFP) are fabricated. Drain offset JL FinTFTs showed a higher breakdown voltage than that of the conventional one. By extending the GFP over the drain offset region, holes were generated on the surface of the drain offset region that reduce drain resistance. Therefore, the drain offset JL FinTFT with E-GFP exhibited better on-current, breakdown, and high-frequency characteristics than the one without E-GFP. Results also show that all the noise spectral densities of various JL FinTFTs follow a $1/f$ trend and were similar in the studied frequency range.

Keywords: drain offset; gate field plate; junctionless FinTFT; RF; system-on panel

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1. Introduction

Polycrystalline silicon thin-film transistors (poly-Si TFTs) are possible candidates for radio frequency (RF) applications owing to their higher electron mobility and driving current than those of amorphous silicon TFTs [1–3]. In recent years, the RF integrated circuit (IC) has been embedded in display panels as, for example, a frequency divider [4], phase-locked loop (PLL) [5], and amplitude-shift-keying demodulator for RF identification tags (RFID) [6], to realize system-on-panels (SOPs). To overcome the short-channel effects (SCEs) caused by the shrinking of the conventional MOSFET, junctionless (JL) field-effect transistors without metallurgical junction were adopted. In this study, we present the drain offset JL poly-Si finlike thin-film transistors (FinTFTs) with and without an extended gate field plate (E-GFP) in comparison with the conventional one. The effect of drain offset and E-GFP on the DC, breakdown, and RF characteristics of JL poly-Si FinTFT are investigated. In addition, the low-frequency noise (LFN) of JL FinTFTs with various structures is compared. The DC and RF characteristics of various JL poly-Si FinTFTs after postmetal annealing (PMA) in forming gas (FG) are discussed.

2. Experiments

JL FinTFTs were fabricated on a 6-silicon wafer with a 1 μm thick silicon dioxide layer as the substrate. First, a 50 nm thick undoped amorphous silicon layer was deposited and then crystallized by solid-phase crystallization at 600 °C for 24 h. The silicon layer was implanted by $^{49}BF^{+2}$ at 15 keV at doses of 1×10^{14} cm^{-2}. The trench structure with 30 nm channel thickness and the active region with multiple nanowires were defined by electron-beam lithography and anisotropic etched by reactive ion etching, respectively. After the active region had been defined, a 10 nm Al_2O_3 layer was deposited by atomic layer deposition as a gate insulator, and a 50 nm TiN was deposited and patterned to form a gate electrode. Subsequently, the source and drain were implanted with $^{49}BF^{+2}$ at 8 keV at doses of 1×10^{15} cm^{-2}, and then subjected to 300 s of low-temperature microwave annealing at a power of 2400 W. For the drain offset sample, a mask was used, so that on

the right side of the gate, part of the drain area remained p^-. Lastly, a 300 nm thick TEOS oxide was deposited, followed by Al–Si–Cu metallization. For the device with E-GFP, the Al–Si–Cu metal above the gate extended towards the drain region and covered the p^-/p^+ junctions as a GFP. Figure 1 shows the process flow of JL FinTFTs.

On-wafer two-port measurements were taken using an Agilent N5245A Network Analyzer and then de-embedded by subtracting the OPEN dummy. Various control biases were applied using an HP 4142B source measure unit.

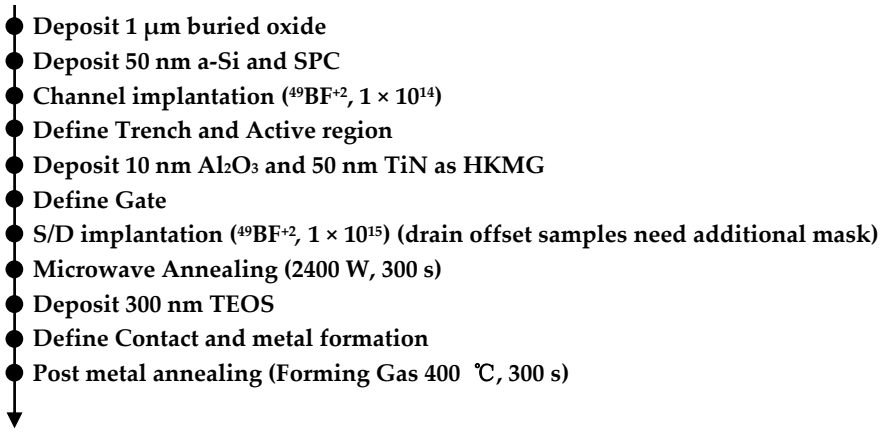


Figure 1. Process flow of JL FinTFTs.

3. Results

Figure 2a,c present the schematic top view of conventional and drain offset JL FinTFTs with and without an extended GFP (E-GFP). The trench length (L_g) for all devices was 200 nm. Figure 2a shows a conventional structure with a drain offset length (L_P^-) of 0 μm. Only the poly-Si under the gate electrode was p^-, and the rest was p^+. Figure 2b shows the drain offset JL FinTFT without E-GFP. When applying ion implantation doping to S/D, a mask is used, and a part of the area next to the drain remains p^-, so that the uncovered part of the gate electrode also retains a small region as p^-. This drain offset length (L_P^-) is 0.25 μm. Figure 2c shows the drain offset JL FinTFT with E-GFP. A GFP extends towards the drain region and covers the p^-/p^+ junctions. The cross-section for drain offset JL FinTFT with E-GFP along B–B′ direction is shown in Figure 2d. Table 1 lists structures and notations for the sample JL FinTFTs used in this study.

Figure 3a presents a top-view scanning electron microscope (SEM) image of the JL FinTFT, and shows the gated raised S/D structure. The multiple nanowire structure was adopted to improve gate controllability and suppress the short channel effects. Figure 3b depicts the cross-sectional transmission electron microscopy (TEM) image of a single nanowire (NW) along with the A–A′ direction in Figure 2a. The bottom side of each channel wire (W_0) was 50 nm, and the measured width of each channel wire (W_{nw}) was approximately 100 nm. In this work, the total fin number was 160, and the effective channel width (W_{eff}) was 16 μm.

Table 1. JL FinTFT structures and notations.

JL FinTFTs	Notations
Conventional JL FinTFTs	Conv.
Drain offset JL FinTFT with E-GFP	Drain offset w/E-GFP
Drain offset JL FinTFT without E-GFP	Drain offset w/o E-GFP

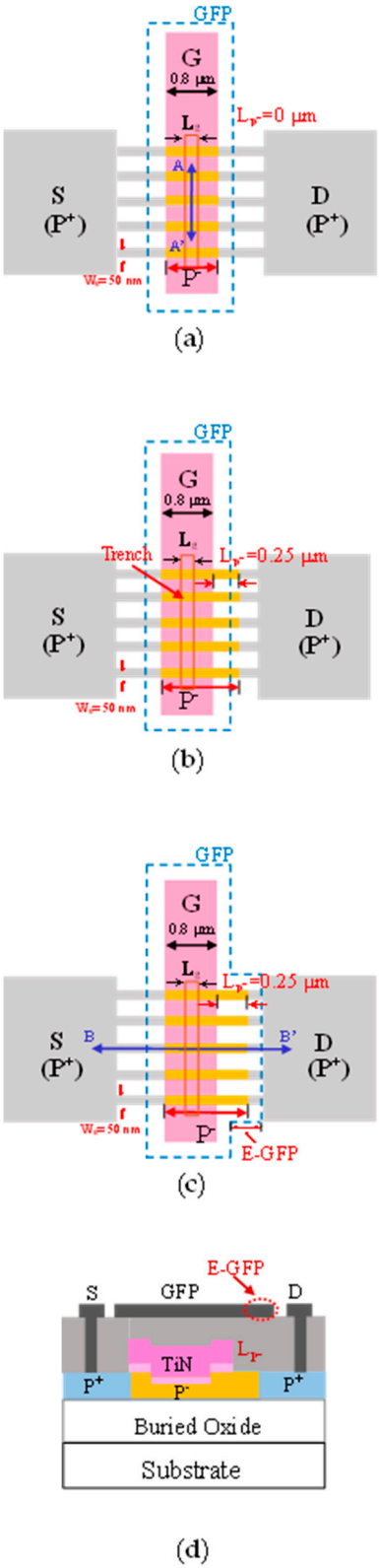
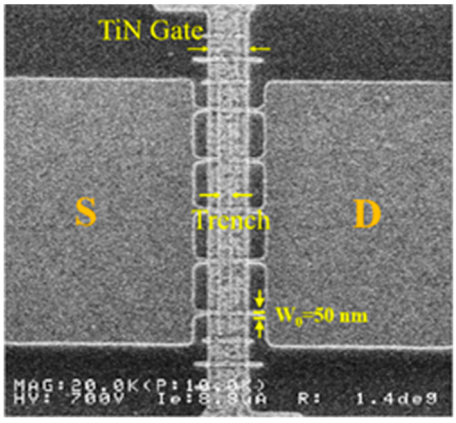
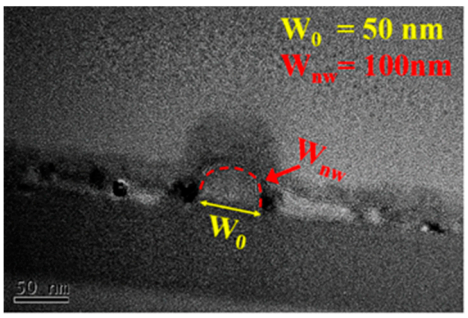


Figure 2. Schematic top view of JL FinTFT for (**a**) conventional structure with drain offset length (L_P^-) of 0 μm. (**b**) Drain offset JL FinTFT without E–GFP and (**c**) drain offset JL FinTFT with E–GFP. (**d**) Cross–sectional view of drain offset JL FinTFT with E–GFP along B–B′ direction.



(**a**)



(**b**)

Figure 3. (**a**) Top-view SEM images of the JL FinTFT with L_g = 200 nm. (**b**) TEM image of a single NW along A–A′ direction.

3.1. DC and Breakdown Characteristics

Figure 4 shows the transfer characteristic curves of JL FinTFTs with various structures. Drain offset JL FinTFTs without E-GFP have a lower on-state current compared to that of others due to its lower drain offset doping concentration. When negative voltage applies to the gate, and the GFP extends towards the drain region and covers the p^-/p^+ junctions, a hole accumulation layer is induced at the surface of the drain offset under the GFP. This hole accumulation layer increases the on-state current. Table 2 lists the electrical parameters of the JL FinTFTs with various structures. V_{th} is defined as the gate voltage required to achieve a normalized drain current of $I_d = (W/L) \times 10^{-8}$ A at V_d = 2 V. DIBL is defined as $\Delta V_g/\Delta V_d$ at $I_d = 10^{-7}$ A. The subthreshold swing (SS) values of the conventional one, drain offset without E-GFP, and drain offset with E-GFP were 397, 403, and 405 mv/dec, respectively. The on-current at $V_{GS} = -3$ V and $V_{DS} = -2$ V, and the I_{on}/I_{off} ratio of the drain offset JL FinTFTs with E-GFP were improved compared to those of the one without E-GFP due to the hole accumulation layer induced at the surface of the drain offset region under the E-GFP.

Table 2. Electrical parameters of the JL FinTFTs with various structures.

Device	V_{th} (V)	DIBL (mV/V)	SS (mV/dec)	I_{on}/I_{off} (A/A)	I_{ON} (mA/mm)
Conventional	0.96	352	397	2.84×10^4	23.4
Drain offset w/o E-GFP	0.86	388	403	3.22×10^3	14.5
Drain offset w/E-GFP	0.95	370	405	6.27×10^3	17.8

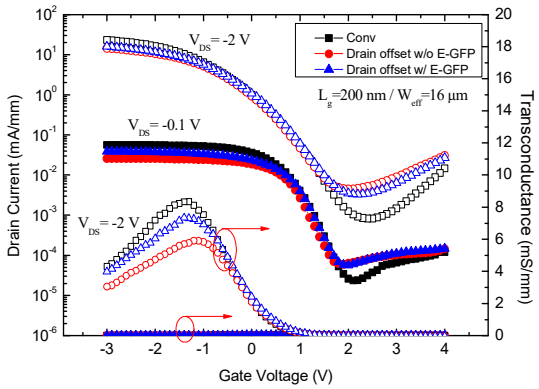
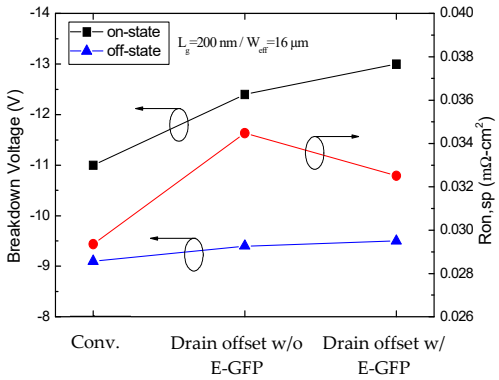


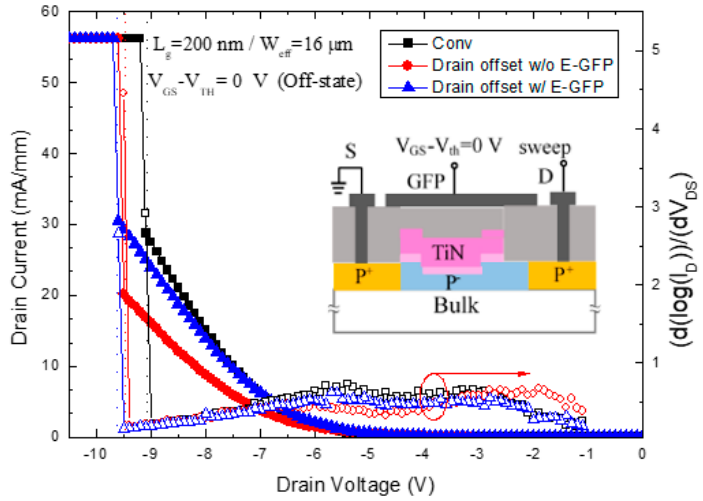
Figure 4. Transfer curves of JL FinTFT for conventional JL FinTFT, drain offset JL FinTFT without E−GFP, and drain offset JL FinTFT with E−GFP.

Figure 5a plots the off-state and on-state breakdown voltage of JL FinTFTs. The off-state and on-state breakdown characteristics were measured with $V_{GS} - V_{th} = 0$ V and $V_{GS} - V_{th} = -2$ V, respectively. To define V_{BD} more precisely, we plotted d (log (I_D))/dV_{DS} as a function of the drain voltage (Figure 5b,c) and obtained the breakdown voltage from the peak value [7]. Drain offset JL FinTFTs with E-GFP had a larger breakdown voltage than that of the conventional one. To clearly understand the effect of structure on breakdown voltage, the electric field distribution of various JL FinTFTs before breakdown was analyzed and is shown in Figure 5d. For the conventional JL FinTFT, a high electric field peak was observed at the right edge of the gate and the p^-/p^+ junction. When the $L_P{}^-$ was 0.25, the p^-/p^+ junction moved to the right and suppressed the electric field peak at the p^-/p^+ junction, resulting in gradual field distribution. Therefore, the JL FinTFT with drain offset rendered the electric field distribution more uniform and increased the device breakdown voltage. However, the light doping concentration of the drain offset region increased the specific-on resistance ($R_{on,sp}$) as shown in Figure 5. Drain offset JL FinTFTs without the E-GFP had the largest $R_{on,sp}$ value among all structures. Adding the E-GFP structure could further increase the breakdown voltage and induce holes at the surface of the drain offset under the E-GFP, thereby reducing the $R_{on,sp}$ value for the drain offset JL FinTFT. This result shows that drain offset JL FinTFTs with E-GFP can solve the tradeoff between specific-on resistance and breakdown voltage.



(**a**)

Figure 5. *Cont.*



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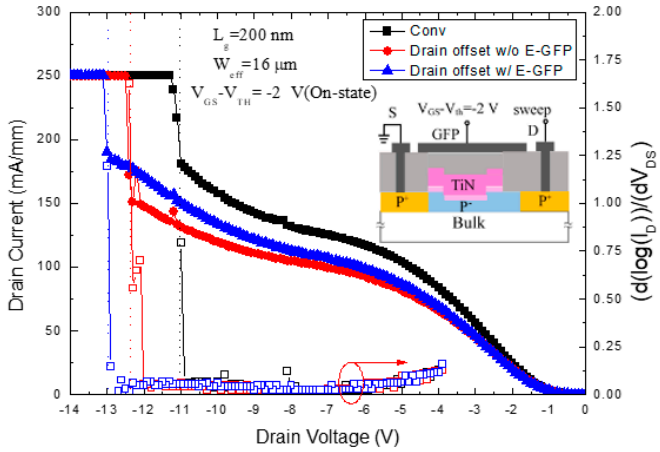

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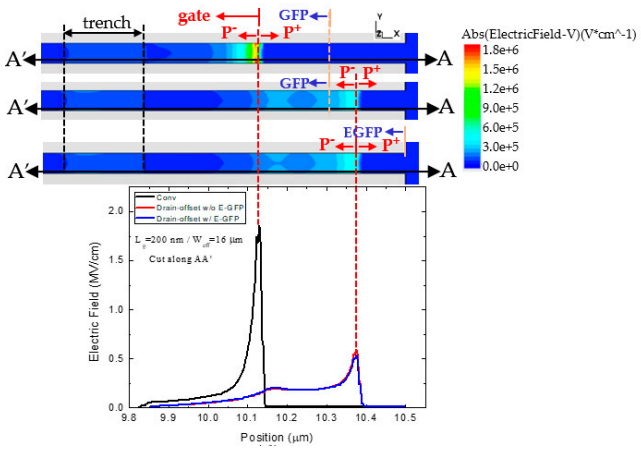
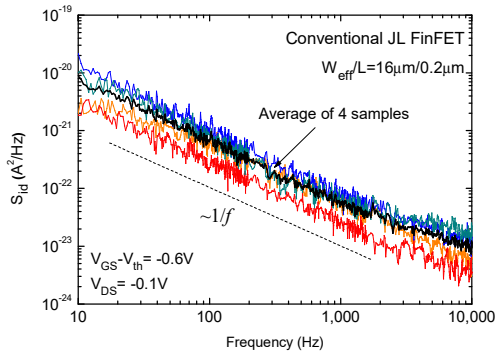


(**d**)

Figure 5. (**a**) Off-state and on−state breakdown voltage, and specific−on resistance of JL FinTFTs. Output characteristics and extraction of breakdown voltage by the derivative method for JL FinTFTs at (**b**) off−state and (**c**) on−state. (**d**) Surface electric field distribution of JL FinTFTs before breakdown.

3.2. Low-Frequency Noise Characteristics

The conduction mechanism of JL field-effect transistors is bulk conduction instead of surface channel conduction, which is different from the conduction mechanism of inversion mode (IM) counterparts. Recent studies show that the LFN of JL nanowire transistors is lower than that of IM nanowire transistors and LFN power spectral density also increases with the dimensions shrinking [8,9]. In this part, the LFN of JL FinTFTs with various structures are compared. The drain current noise spectral density (S_{Id}) of four samples of the conventional JL FinTFT with $V_{DS} = -0.1$ V and $V_{-S} - V_{th} = -0.6$ V is shown in Figure 6a. For the smallest transistors, the dispersion of noise spectra must be considered; in this case, it was within one decade. The average over four samples, displayed as the bold line, showed a typical $1/f$ trend. In the following discussion, we used the average noise spectrum to analyze low-frequency noise. Figure 6b shows the average value of S_{Id} for various JL FinTFTs. All noise spectral densities followed a $1/f$ trend and were similar in the studied frequency range.



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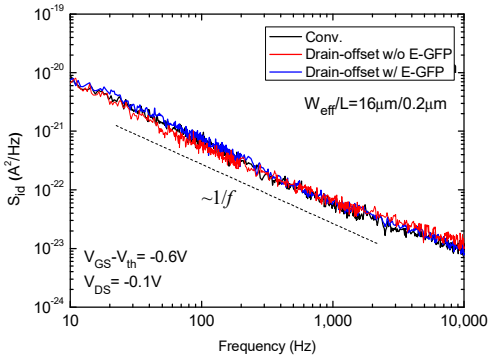


(**b**)

Figure 6. (**a**) Drain current noise spectral density of four samples of conventional JL FinTFT with $V_{DS} = -0.1$ V and $V_{GS} - V_{th} = -0.6$ V. The average shows a typical $1/f$ trend. (**b**) Average value of S_{Id} of various JL FinTFTs.

3.3. AC Characteristics

Figure 7a plots the cutoff frequency (f_T) and maximal oscillation frequency (f_{max}) versus drain current for the JL FinTFTs with various structures. After de-embedding, f_T and f_{max} were determined by extrapolating the short circuit current gain ($|H_{21}|^2$) and the unilateral power gain (U), respectively, to 0 dB along a line with a slope of 20 dB/decade. The difference between the f_T and f_{max} values of various structures increased with the increase in gate voltage and drain current. As the gate voltage increased, the hole accumulation layer induced by the E-GFP was formed in the offset region, thereby reducing

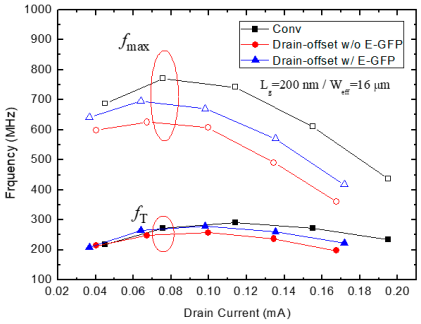
S/D resistance and boosting the drain current. For further analysis of the high-frequency characteristics, the parameters of the small-signal equivalent circuit were extracted using the method of Lovelace et al. [10]. Figure 7b,d plot the extracted small-signal parameters as functions of the drain current. In this work, the effect of drain series resistance is very important. The approximate for f_T that takes drain series resistance can be expressed as follows [11]:

$$f_T \approx \frac{g_m}{2\pi[C_{gs} + C_{gd}(1 + g_m R_d)]} \quad (1)$$

where g_m is the transconductance, C_{gs} is the gate-to-source capacitance, C_{gd} is the gate-to-drain capacitance, and R_d represents the drain series resistance. The approximate expression for $f_{\max}$ is given by [12].

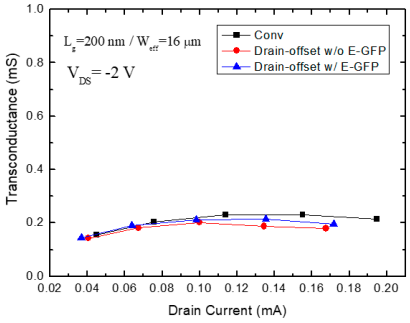
$$f_{\max} \sim \frac{f_T}{\sqrt{4g_{ds}R_g + 8\pi f_T C_{gd}(R_g + \alpha R_d)}} \quad (2)$$

where g_{ds} is the output conductance, Rg is the gate series resistance, and Rd is the drain series resistance. The transconductances of JL FinTFTs with various structures were similar, with only a slight deviation in the transconductance values between the different structures at high gate voltage (Figure 7b). Adding an E-GFP above the drain offset region could increase the on-current, but it increased the parasitic capacitance at the drain side due to a large overlap between E-GFP and the drain offset region (Figure 7c). As the structure on the source side of these three JL FinTFTs remained unchanged, the values of C_{gs}, and R_s (not shown here) were similar. Extracted R_d values are shown in Figure 7d. When the L_P^- length increased to 0.25 µm, because the doping concentration of the offset region was lighter, the drain offset JL FinTFTs without E-GFP had the largest R_d value among the three transistors. The R_d value of the drain offset JL FinTFTs with E-GFP was significantly lower than that of the one without E-GFP. An induced hole accumulation layer at the surface of the drain offset region under the E-GFP effectively decreased the R_d value. Hence, the better f_T and $f_{\max}$ of the drain offset JL FinTFTs with E-GFP than those of the one without E-GFP were mainly attributed to the change in R_d.



(a)

Figure 7. *Cont.*



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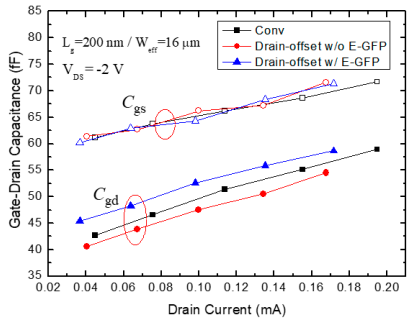

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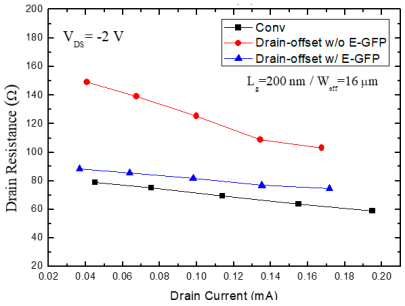

(**d**)

Figure 7. (**a**) f_T and f_{max} of various JL FinTFTs. Extracted (**b**) transconductance, (**c**) parasitic capacitances, and (**d**) parasitic drain resistances of various JL FinTFTs.

3.4. Postmetal Annealing (PMA)

Postmetal annealing (PMA) in forming gas (FG) improves carrier mobility, threshold voltage, subthreshold swing, and interface trap density [13,14]. Figure 8a,b show the transfer characteristic curves and output characteristics curves of various JL FinTFTs after low-temperature PMA in FG at 400 °C for 300 s. Table 3 lists the electrical parameters of various JL FinTFTs after PMA in FG. FG-annealed JL FinTFTs exhibited significantly lower V_{th}, DIBL, SS, and higher on-current than those of JL FinTFTs before FG being annealed. For high-frequency characteristics, after FG annealing, the f_T of various JL FinTFTs was also greatly improved, and the f_{max} even exceeded 1 GHz. Table 4 presents a comparison with previously proposed JL poly-Si TFTs. For p-type JL poly-Si TFTs, a high f_T value of about 0.79 GHz at $V_{DS} = -2$ V was obtained here.

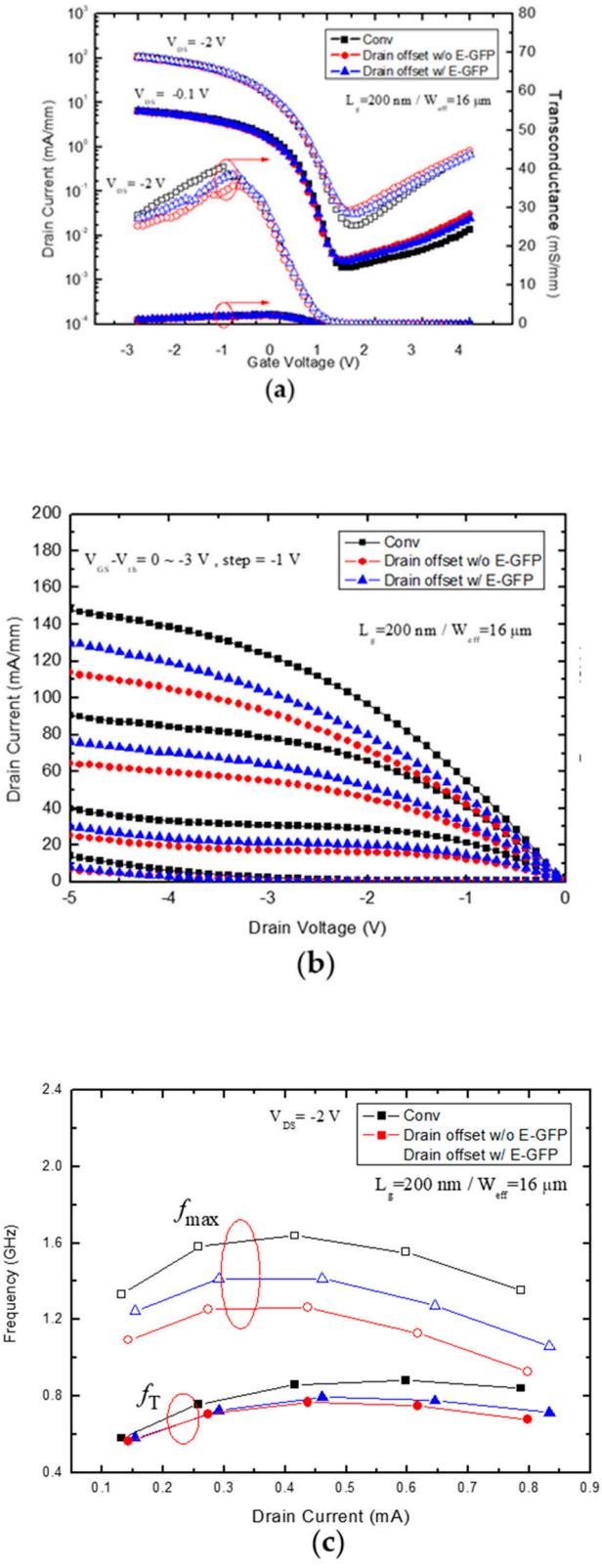

Figure 8. (**a**) Transfer curves, (**b**) output curves, and (**c**) f_T and $f_{\max}$ of various JL FinTFT after PMA in FG at 400 °C for 300 s.

Table 3. Electrical parameters of the JL FinTFTs with various structures after PMA in FG at 400 °C for 300 s.

Device	V_{th} (V)	DIBL (mV/V)	SS (mV/dec)	I_{on}/I_{off} (A/A)	I_{ON} (mA/mm)
Conventional	0.33	186	275	6.69×10^3	111
Drain offset w/o E-GFP	0.25	201	298	1.42×10^3	103
Drain offset w/E-GFP	0.27	198	299	3.49×10^3	106

Table 4. Parameters in comparison with other reports.

	This Work	Ref. [15]	Ref. [16]
Structure	p-type JL FinTFT (drain offset w/E-GFP)	p-type JL stacked GAA nanosheet TFT	n-type JL planar TFT
Channel material	Poly-Si	Poly-Si	Poly-Si
$W_0/W_{eff}/L$ (nm/μm/μm)	50/16/0.2	30/21/0.08	NA/8/0.4
V_{th} (V)	0.27	−0.4 (single)	−0.19
DIBL (mV/V)	198	400 (single)	161
SS ((mV/dec)	299	230 (single)	309
I_{on}/I_{off} (A/A)	3.49×10^3	2.4×10^6 (single)	8×10^7
Peak f_T (GHz)	0.79@V_{DS} = −2 V	0.048@V_{DS} = −4 V (single)	3.36@V_{DS} = 2 V
Peak f_{max} (GHz)	1.4@V_{DS} = −2 V	NA	7.37@V_{DS} = 2 V

4. Conclusions

In this work, the drain offset structure was used to increase the breakdown voltage. However, lower drain offset doping concentrations degraded DC and RF characteristics. Drain offset JL FinTFTs with E-GFP not only present a higher on-state current, higher breakdown voltage, and lower $R_{on,sp}$, but also a higher f_T and f_{max} than those of the one without E-GFP. The JL FinTFT with drain offset rendered the electric field distribution more uniform and improved the breakdown voltage, but the drain offset region with low doping concentration increased drain resistance. By extending the GFP above the p^-/p^+ junction, a hole accumulation layer could be induced on the surface of the drain offset region, resulting in lower drain resistance, and improved DC and high-frequency characteristics. Drain offset JL FinTFTs with E-GFPF solve the tradeoff between breakdown voltage and $R_{on,sp}$. Drain offset JL FinTFT with E-GFP exhibited higher breakdown voltage than that of the conventional one, although the current capability slightly decreased. The tradeoff between current and voltage capabilities can be improved through optimization in drain offset length, p^- concentration, and premetal dielectric thickness. In addition, LFNs were similar for all three structures in the studied frequency range. Furthermore, the FG-annealed JL FinTFTs exhibited great DC and high-frequency electrical properties, and the f_{max} even exceeded 1 GHz.

Author Contributions: H.-H.H. conceived and designed the experiments; H.-H.H. and C.-L.H. fabricate the transistors; C.-L.H., Z.-Y.L. and G.-T.C. measured the electrical characterization; H.-H.H. and C.-L.H. analyzed the data; H.-H.H. and K.-M.C. supervised the project; H.-H.H. wrote the manuscript; and all authors contributed discussions and feedback to the manuscript and the project. All authors have read and agreed to the published version of the manuscript.

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Conflicts of Interest: The authors declare no conflict of interest.

References

1. Botrel, J.; Savry, O.; Rozeau, O.; Templier, F.; Jomaah, J. Polysilicon high frequency devices for large area electronics: Characterization, simulation and modeling. *Thin Solid Film.* **2007**, *515*, 7422–7427. [CrossRef]
2. Chen, Y.-J.E.; Lee, Y.-J.; Yu, Y.-H. Investigation of Polysilicon Thin-Film Transistor Technology for RF Applications. *IEEE Trans. Microw. Theory Tech.* **2010**, *58*, 2076911. [CrossRef]
3. Kim, S.Y.; Loke, W.-F.; Jung, B.; Roy, K. High-Frequency Modeling of Poly-Si Thin-Film Transistors for Low-Cost RF Applications. *IEEE Trans. Electron Devices* **2012**, *59*, 2296–2301. [CrossRef]
4. Yu, Y.-H.; Chen, Y.-J.E. Ring-Based Direct Injection-Locked Frequency Divider in Display Technology. *IEEE Microw. Wirel. Components Lett.* **2008**, *18*, 752–754. [CrossRef]
5. Lin, W.M.; Liu, S.I.; Kuo, C.H.; Li, C.H.; Hsieh, Y.J.; Liu, C.T. A phase-locked loop with self-calibrated charge Pumps in 3-μm LTPS-TFT Technology. *IEEE Trans. Circuits Syst. II Express Briefs* **2009**, *56*, 142–146.
6. Yu, Y.-H.; Lee, Y.-J.; Li, Y.-H.; Kuo, C.-H.; Li, C.-H.; Hsieh, Y.-J.; Liu, C.-T.; Chen, Y.-J. An LTPS TFT Demodulator for RFID Tags Embeddable on Panel Displays. *IEEE Trans. Microw. Theory Tech.* **2009**, *57*, 1356–1361. [CrossRef]
7. Lee, C.-W.; Afzalian, A.; Yan, R.; Akhavan, N.D.; Xiong, W.; Colinge, J.-P. Drain Breakdown Voltage in MuGFETs: Influence of Physical Parameters. *IEEE Trans. Electron Devices* **2008**, *55*, 3503–3506. [CrossRef]
8. Simoen, E.; Veloso, A.; Matagne, P.; Collaert, N.; Claeys, C. Junctionless Versus Inversion-Mode Gate-All-Around Nanowire Transistors from a Low-Frequency Noise Perspective. *IEEE Trans. Electron Devices* **2018**, *65*, 1487–1492. [CrossRef]
9. Veloso, A.; Parvais, B.; Matagne, P.; Simoen, E.; Huynh-Bao, T.; Paraschiv, V.; Vecchio, E.; Devriendt, K.; Rosseel, E.; Ercken, M.; et al. Junctionless gate-all-around lateral and vertical nanowire FETs with simplified processing for advanced logic and analog/RF applications and scaled SRAM cells. In Proceedings of the 2016 IEEE Symposium on VLSI Technology, Honolulu, HI, USA, 14–16 June 2016; pp. 1–2. [CrossRef]
10. Lovelace, D.; Costa, J.; Camilleri, N. Extracting small-signal model parameters of silicon MOSFET transistors. In Proceedings of the 1994 IEEE MTT-S International Microwave Symposium Digest (Cat. No.94CH3389-4), San Diego, CA, USA, 23–27 May 1994. [CrossRef]
11. Tasker, P.J.; Hughes, B. Importance of source and drain resistance to the maximum fT of millimeter-wave MODFETs. *IEEE Electron Device Lett.* **1989**, *10*, 291–293. [CrossRef]
12. Lim, T.C.; Armstrong, G.A. The impact of the intrinsic and extrinsic resistances of double gate SOI on RF performance. *Solid-State Electron.* **2006**, *50*, 774–783. [CrossRef]
13. Choi, R.; Onishi, K.; Kang, C.S.; Cho, H.-J.; Kim, Y.; Krishnan, S.; Akbar, M.; Lee, J. Effects of deuterium anneal on MOSFETs with HfO_2 gate dielectrics. *IEEE Electron Device Lett.* **2003**, *24*, 144–146. [CrossRef]
14. Simoen, E.; Rothschild, A.; Vermang, B.; Poortmans, J.; Mertens, R. Impact of forming gas annealing and firing on the Al_2O_3 p-Si interface state spectrum. Electrochem. *Solid-State Lett.* **2011**, *14*, H362–H364. [CrossRef]
15. Hu, H.H.; Meng, C.F.; Wang, W.H.; Lu, T.H.; Lee, Y.J.; Sung, P.J.; Chen, K.M. RF Characteristics of Stacked Poly-Si Nanosheets Thin Film Transistors. In Proceedings of the 2021 Silicon Nanoelectronics Workshop (SNW), Kyoto, Japan, 13 June 2021.
16. Tsai, T.-I.; Chen, K.-M.; Lin, H.-C.; Lin, T.-Y.; Su, C.-J.; Chao, T.-S.; Huang, T.-Y. Low-Operating-Voltage Ultrathin Junctionless Poly-Si Thin-Film Transistor Technology for RF Applications. *IEEE Electron Device Lett.* **2012**, *33*, 1565–1567. [CrossRef]