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A 0.0012 mm^2 6-bit 700 MS/s 1 mW Calibration-Free Pseudo-Loop-Unrolled SAR ADC in 28 nm CMOS

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Abstract: This paper presents a high-speed successive approximation register (SAR) analog-to-digital converter (ADC) that takes advantage of both asynchronous SAR ADC and loop-unrolled (LU) SAR ADC. By utilizing the output of the dynamic amplifier (DA) to generate an asynchronous clock, the reset time for the DA can be hidden behind the comparator latching time. Dedicated latches for each digital-to-analog converter (DAC) element eliminate the need for DAC switching logic. The proposed inverter-inserted three-stage comparator significantly reduces the input-referred offset of the comparator. The prototype 6-bit 700 MS/s SAR ADC was implemented in a 28 nm CMOS process and has a small 0.0012 mm^2 area. The measured peak DNL and INL without any mismatch calibration were 0.33 and 0.27 LSB, respectively. With Nyquist input, the measured signal-to-noise and distortion ratio (SNDR) and spurious-free dynamic range (SFDR) were 34.07 and 47.52 dB, respectively. The power consumption was 1 mW under a supply voltage of 1.0 V, leading to a Walden figure of merit (FoM) of 34.6 fJ/conversion-step at 700 MS/s.

Keywords: asynchronous clock; loop-unrolled SAR; dynamic amplifier; calibration free; inverter-inserted comparator; split latch

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1. Introduction

The high-speed communication systems such as ADC-based transceivers for high-speed I/O standards using four-level pulse modulation (PAM-4) required low-resolution (6–8 bit) and tens of GS/s time-interleaved (TI) ADC [1–3]. The performance of these systems is greatly affected by the characteristics of input bandwidth, sampling rate, effective resolution, power consumption, and area of the TI ADC. In order to realize a low-power TI ADC of several tens of GS/s, a single channel ADC used as a sub-ADC must be designed to be very compact and high-speed. During the past decade, successive approximation register (SAR) analog-to-digital converters (ADCs) have become a dominant ADC architecture as sub-ADCs of the TI ADC, covering a wide range of resolution and speed owing to advanced process technologies, mostly attributed to their digital friendly architecture [4–11]. The need for high-speed clocks for internal loop operation in a synchronous SAR ADC can be eliminated by using asynchronous architecture [12–14]. It could even make the conversion speed faster, because the next comparison can be conducted as soon as the previous decision is completed, without the need to wait for the next clock. Nevertheless, the logic delay, due to the digital-to-analog converter (DAC) control, and the comparator reset time needed for every decision cycle, due to the repeatedly used single comparator, create a fundamental speed bottleneck for asynchronous SAR ADC. The time spent for the repeated reset and DAC control can be eliminated by unrolling the loop with an architecture of so-called loop-unrolled (LU) SAR, which uses as many comparators as the ADC resolution [15–21]; accordingly, the conversion speed can be further enhanced. However, the major drawbacks of the LU SAR ADC are offset mismatches among the multiple comparators, which require burdensome offset calibration with a foreground [15–17] or background using an additional

comparator [18–20]. Meanwhile, the offset calibration burden could be alleviated by redundancy bits [21]. However, in order to use the redundancy bit, not only is an additional conversion cycle required, but also the design complexity increases, because two different types of ADCs should be used as in [21].

In this paper, we propose a calibration-free pseudo-loop-unrolled (P-LU) SAR ADC architecture that has the speed advantage of an LU SAR ADC without the burden of offset calibration. As the comparator can be designed such that its offset is dominantly determined by the offset of a preamplifier, a single preamplifier can be shared for every decision, as in a conventional SAR ADC. Therefore, the overall area of the ADC can be designed to be compact, without a complex calibration block, and operate with enhanced conversion speed.

This paper is organized as follows. In Section 2, the conventional LU SAR ADC architecture is reviewed. Section 3 describes the architecture of the proposed P-LU ADC. Detailed circuit implementations of the inverter-inserted comparator, the clock generator, and the high-speed logic are explained in Section 4. Section 5 shows the measurement results, and Section 6 concludes the paper.

2. Review of LU SAR ADC Architecture

Figure 1 shows a conventional 6-bit LU SAR ADC with six comparators; each of them is dedicated to an individual capacitor for control of the DAC. After the input voltage is sampled by the bootstrapped (BTS) track-and-hold (T/H), the MSB code is obtained by the enable clock ($\Phi_{EN\langle 5\rangle}$) synchronized with the external sampling clock (Φ_S). When the MSB decision is complete, the clocks for the following comparators are generated from their previous comparators, in order, by the clock generation (CG) blocks. This eliminates the need for DAC switching logic or comparator reset time, leaving the essential operations of comparator latching and DAC settling time as the ultimate speed limitation factors, while the need for offset calibration becomes an additional burden, for example, in area and power consumption.

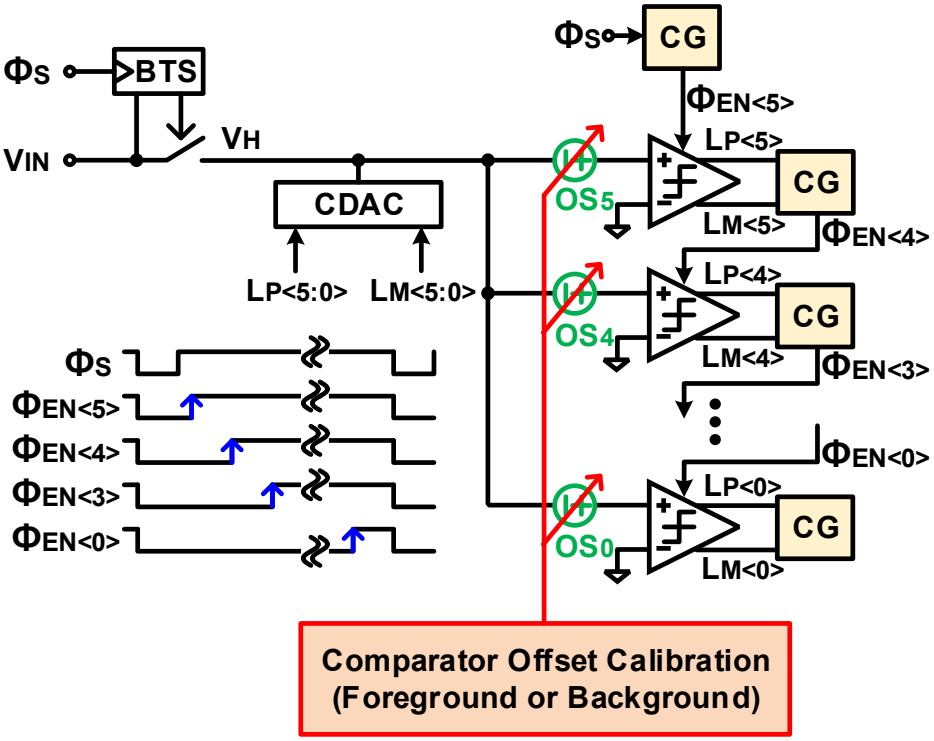

Figure 1. Conceptual block and timing diagram of conventional LU SAR ADC [15–20].

The offset mismatches of the comparators can be calibrated for foreground [15–17] and background [18–20]. Since the foreground calibration technique requires an additional current cell or capacitor in the comparator, it adversely affects the power consumption and operation speed. In addition, a hardware burden on the area is increased by the addition of logic blocks for detecting and correcting the offset errors. Meanwhile, the offset mismatch of the comparator is changed according to the PVT variations as well as process mismatch. Therefore, for the PVT-insensitive design, the offset mismatch of the comparators inside the LU SAR ADC needs to be calibrated against the background [18–20]. The application of the background offset calibration technique affects the conversion speed of the ADC, because it requires additional time for calibration after conversion is complete. In this paper, we propose a calibration-free ADC architecture that can overcome the disadvantages of foreground and background calibration techniques in the previously reported LU SAR ADCs.

3. Proposed Pseudo-LU SAR ADC

In our design, we want to eliminate the need for offset calibration of the comparator with a single preamplifier while hiding the reset time of the preamplifier behind the essential operations to achieve a conversion speed comparable to that of LU SAR ADCs. With this motivation, the proposed P-LU SAR ADC architecture is shown in Figure 2. The proposed P-LU SAR ADC consists of a T/H, a binary controlled capacitive DAC (CDAC), a self-triggered DA(ST-DA), a Φ_{EN} generator (Latch EN GEN), and six latches. The CDAC is designed with a split-capacitor scheme, as in [22], and the total capacitance of the CDAC is 32 fF with a 0.5 fF unit capacitor. If the switching scheme of the CDAC using a common voltage, V_{CM}, as in [15], is applied to the proposed P-LU SAR ADC, the size of the CDAC can be reduced in half compared to the split-capacitor scheme. However, the switching scheme using V_{CM} increases the design burden on switches and control logics for V_{CM}. On the other hand, the split-capacitor scheme requires only switches for the reference top and bottom voltages. Therefore, the switches for the CDAC can be designed compactly, and can be directly controlled by the differential outputs of the six latches, $L_{P<5:0>}$ and $L_{M<5:0>}$, as shown in Figure 2. In other words, the logic delay for switching the CDAC is very short. The reset phase (when Φ_{DA} is low, the D_P and D_M nodes are discharged to ground) and the amplification phase (when Φ_{DA} is high, the D_P and D_M nodes are charged to VDD) of the DA are determined by the asynchronous timing generator (Async. TG) based on the output signals of the DA (D_P and D_M). The differential signals amplified by the ST-DA are converted into digital code by each latch synchronized to the rising edge of the Φ_{DA} using the Latch EN GEN as shown in the timing diagram in Figure 2. The operation details of the ST-DA and the Latch EN GEN are covered in Section 4. The proposed ADC has a single ST-DA for pre-amplification and multiple latches dedicated to switching individual DAC elements, as in the LU SAR ADC. Owing to the dedicated latches, the proposed structure does not require reset time for the latches, as in the LU SAR ADC.

Figure 3a shows the critical clock path of the conventional LU SAR ADC using a double-tail comparator [23] in each cycle, which can be expressed as follows.

$$T_{1cycle} = t_{DA,\,amp} + t_{Latch} + \max\{t_{DAC},\ t_{CG,\,LU}\} \quad (1)$$

Here, $t_{DA,\,amp}$, t_{Latch}, t_{DAC}, and $t_{CG,\,LU}$ represent the delay time of DA amplification, the comparator latching, the DAC settling, and the CG logic, respectively. Unlike the conventional LU SAR ADCs, in which the next clock is generated by sensing the output of the latch, this P-LU SAR ADC uses the outputs of the DA for the next clock generation, because the DA outputs can be indicators of the comparator decision state, as in [24], which utilized the DA outputs to avoid metastability. By moving the CG block forward to the input of the latch, as illustrated in Figure 3b, the DA clock generation time ($t_{CG,\,PLU}$) can

be hidden behind the latching + DAC settling time ($t_{Latch}+t_{DAC}$) owing to their parallel operation. The cycle of P-LU SAR ADC can be described as follows.

$$\begin{aligned} T_{1cycle} &= t_{DA,\,amp} + t_{CG,\,PLU} \\ &\approx t_{DA,\,amp} + t_{Latch} + t_{DAC} \end{aligned} \quad (2)$$

To obtain a speed comparable to that of the LU SAR ADC, the time for DA clock generation ($t_{CG,\,PLU}$) should be designed similar to the time for ($t_{Latch}+t_{DAC}$) as Equation (2). Note that the double-tail comparator combining the DA and latch increases the number of stages over the strong-arm comparator used in the conventional LU SAR ADCs [15–20], but it could be designed with a competitive latching time under the condition of low input common voltage [23]. From Equations (1) and (2), the proposed P-LU SAR ADC not only realizes a conversion speed comparable to that of the LU SAR ADCs, but also eliminates the offset calibration burden, which is a disadvantage of the conventional LU SAR ADC. As a result, the proposed ADC can be designed with a competitive conversion speed and a very small area compared to the LU SAR ADCs.

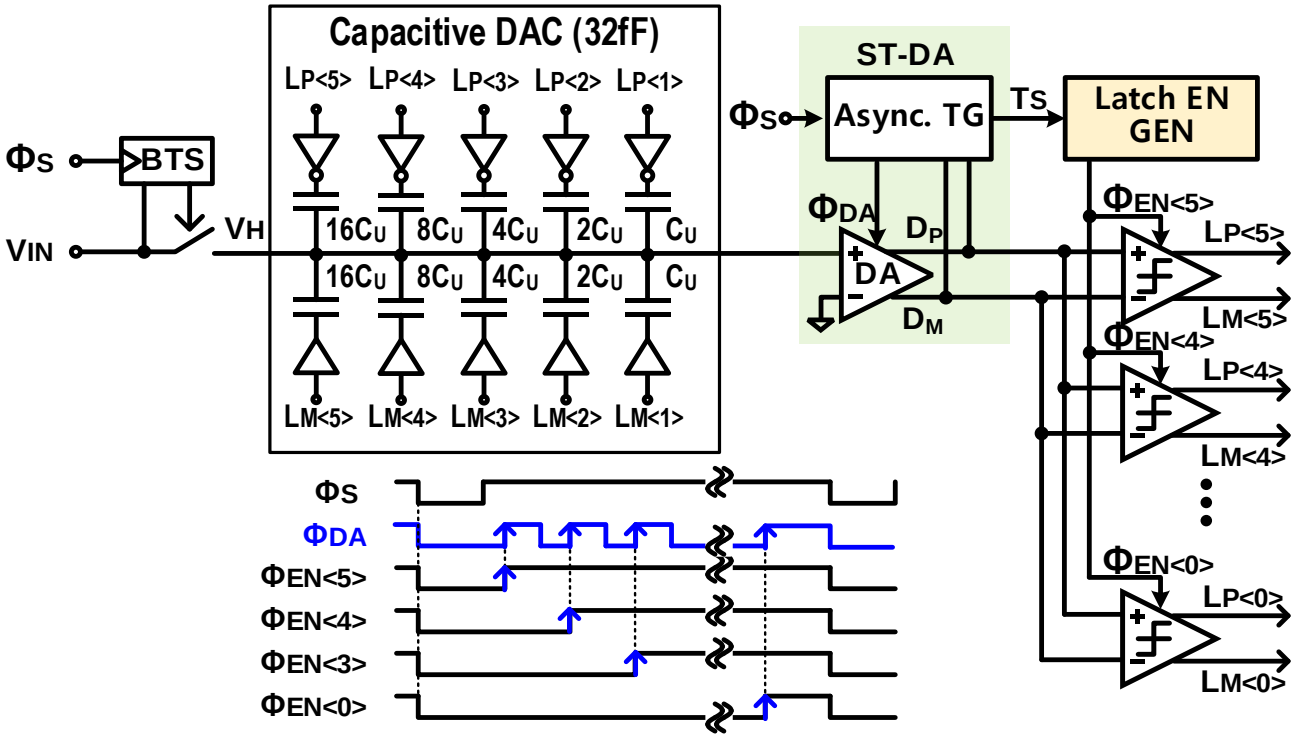

Figure 2. Conceptual block and timing diagram of proposed calibration-free P-LU SAR ADC.

The characteristics and advantages of the proposed P-LU SAR ADC introduced so far are summarized and compared with the previously reported SAR ADCs in Table 1. In the conventional asynchronous SAR ADC [14], the conversion time is increased by the comparator reset time and the DAC switching logic delay. Meanwhile, in the LU SAR ADC [15–21], the input gate capacitance is increased by the comparator required as much as the resolution (N bits). Furthermore, the hardware burden and current consumption of the ADC are increased by the offset calibration for the comparators [15–20]. In the case of LU SAR + SAR ADC using a redundancy bit, an additional conversion cycle is required to obtain the redundancy bit. Moreover, the time for the comparator reset and register operation in the fine stage asynchronous SAR ADC affects the conversion time [21].

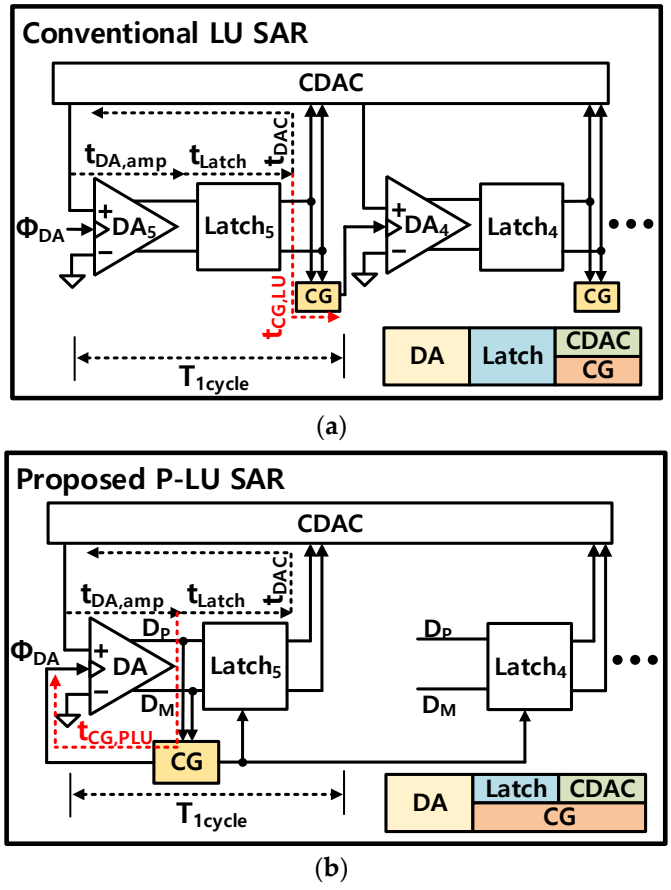

Figure 3. Comparison of the main clock paths of (**a**) the LU SAR ADC and (**b**) the proposed P-LU SAR ADC.

Table 1. Comparison for SAR ADC architectures.

N-bit	Async. SAR [14]	LU SAR [15–17] (Boreground cal.)	LU SAR [18–20] (Background cal.)	LU SAR + SAR [21] (Redundancy bit)	P-LU SAR (This Work)
# of comparators	1	N	N + 1	N	One DA + N
# of input gates	1	N	N + 1	N	1
Conversion cycle	N	N	N + 1	N + 1	N
Offset calibration	Not needed	Needed	Needed	Not needed	Not needed
Comparator reset	Needed	Not needed	Not needed	Partially Needed	Hidden
DAC switching logic	Needed	Not needed	Not needed	Not needed	Not needed

In this work, since the proposed P-LU SAR ADC uses only one DA as a preamplifier, it could be designed with a small input gate capacitance without offset calibration such as in the conventional SAR ADC. Moreover, as with the LU SAR ADC, the P-LU SAR ADC can eliminate the effects of the comparator reset time and the DAC switching logic delay. That is, the proposed ADC can be designed as compact, power efficient, and high speed.

4. Circuit Implementation

4.1. Inverter-Inserted Three-Stage Comparator

To discuss the specific timing in our design, we need first to discuss the detailed circuit design of the comparator. To achieve low input-referred offset without calibration despite the wide spread of the offset distribution of the following multiple latches, the preamplifier must provide a sufficiently high gain. In addition, the preamplifier should have enough

driving capability for the multiple latches. In this design, therefore, an inverter-inserted three-stage comparator was proposed, consisting of one DA as a preamplifier, six latches for 6-bit conversion, and an inverter stage after the DA to provide sufficient gain and driving strength, as shown in Figure 4a.

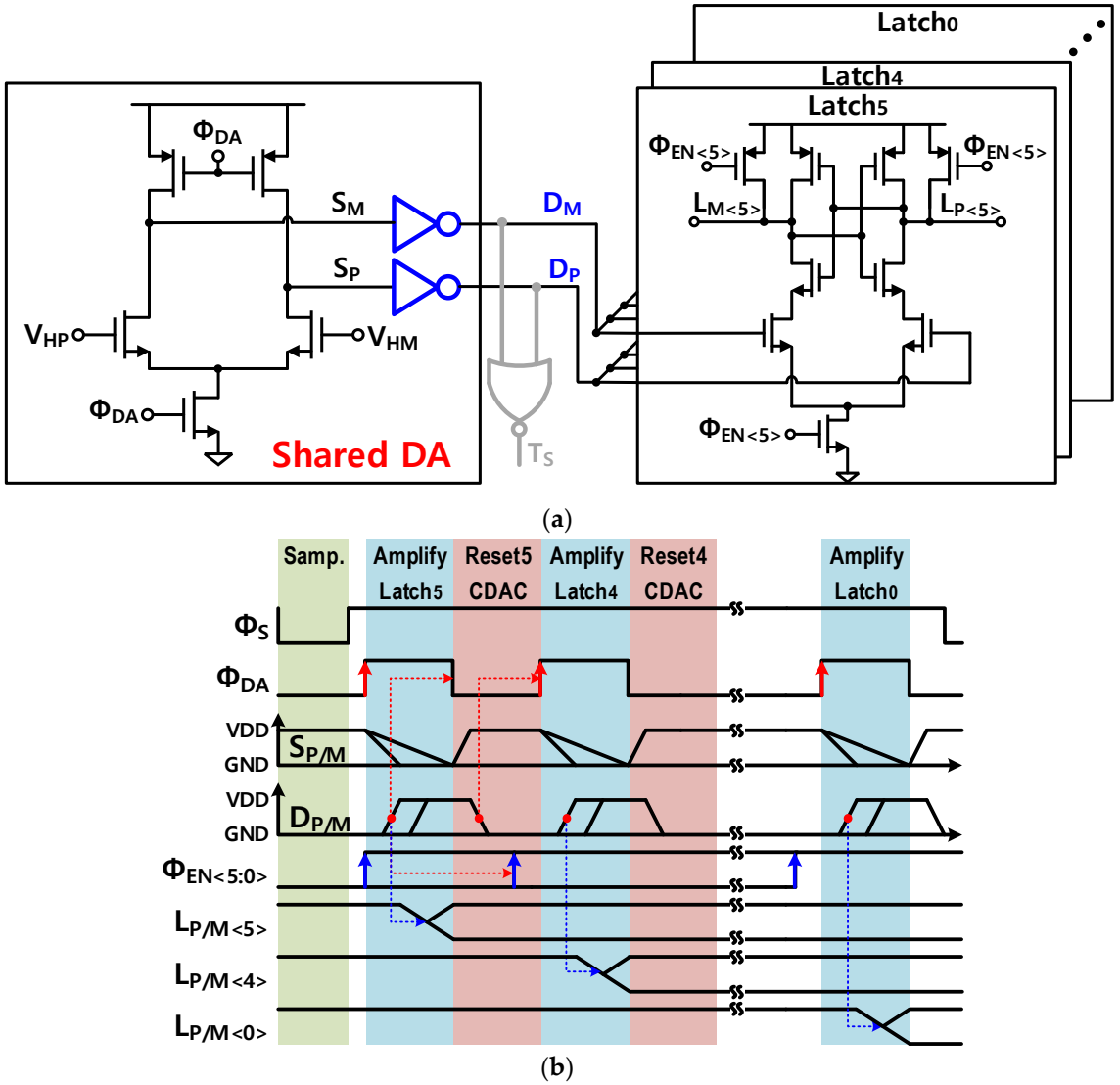

Figure 4. Inverter-inserted three-stage comparator. (**a**) Circuit and (**b**) timing diagrams.

Figure 4b shows the timing diagram to explain the operation of the proposed comparator in more detail. In the sampling phase (i.e., Φ_S is 0), the DA and six latches were reset. After the input sampling was completed, Φ_{DA} became 1 for amplification and $\Phi_{EN\langle 5\rangle}$ was enabled to ready $Latch_5$. In the amplification phase of the DA, D_P and D_M were charged to VDD with a delay difference. Note that the delay information of the D_P and D_M nodes was generated by the inverter stage based on the slope difference of S_P and S_M nodes. Since the inverter stage converted the slope information of the S_P and S_M nodes into the logic levels, this architecture reduced concern about the latch metastability; then, the final stage worked as digital latches, with enable signals of Φ_{EN}. As the D_P and D_M nodes were charged to VDD, the MSB code was determined according to the difference in activation time between the input transistors of $Latch_5$. The DAC operation started immediately with the output of $Latch_5$ ($L_{P<5>}$ and $L_{M<5>}$) and was completed before the next conversion cycle began. Keep in mind that, as mentioned in Section 3, the DA and latches were triggered by D_P and D_M, except for the MSB conversion cycle. Therefore, after the amplification phase, Φ_{DA}

became 0 for reset, and $\Phi_{EN\langle 4\rangle}$ was enabled to ready $Latch_4$. This DA-based conversion cycle was repeatedly performed from $Latch_4$ to $Latch_0$ for $\Phi_{EN\langle 4:0\rangle}$. The details for the timing generation of Φ_{DA} and $\Phi_{EN\langle 4:0\rangle}$ are explained in Section 4.2.

As one of the major motivations of the proposed architecture was to reduce the input-referred offset mismatch by the gain of DA, the comparator offset distribution was simulated. Figure 5 shows several histograms of the offset mismatch from the Monte Carlo simulation results with 1000 samples. Figure 5a shows the distribution of the input-referred offset of a conventional strong-arm latch without a preamplifier; the standard deviation was 15 mV. As the differential input range of this ADC was 800 mVdiff, and the 1 LSB voltage was 12.5 mVdiff, the estimated offset distribution could degrade the performance of the ADC. With a DA for preamplification, the standard deviation of the input-referred offset was reduced to 7 mV thanks to the gain of the DA, as shown in Figure 5b. However, when the 3σ value was considered, it was not sufficiently small. As shown in Figure 4, in the amplification phase, the S_P and S_M nodes were discharged to ground with different slopes according to the input voltage difference. By inserting an inverter pair between the DA and the six latches as shown in Figure 4, the slope difference of S_P and S_M nodes was converted into a delay difference by the gain of the inverter. That is, the input difference of the latch following the inverter was increased. As a result, the standard deviation of the input-referred offset was reduced to 1.16 mV, as shown in Figure 5c. Because the 3σ value (3.5 mV) was smaller than 0.5 LSB (6 mV), the proposed ADC did not require any burdensome offset calibration.

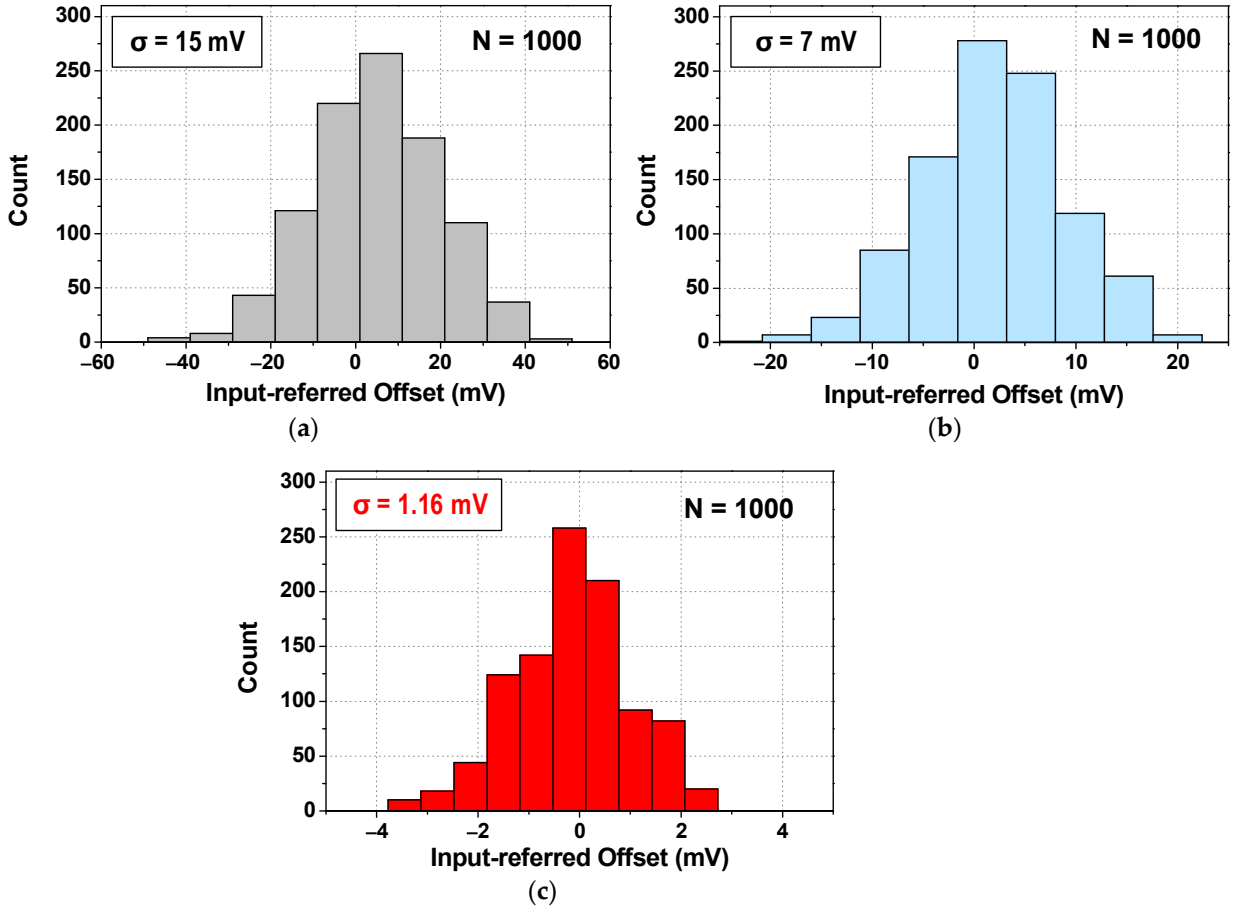

Figure 5. Monte Carlo simulation results of input-referred offset mismatch. (**a**) Strong-arm latch, (**b**) DA + latch, and (**c**) inverter-inserted comparator (this work).

4.2. Clock Generator (CG)

A detailed logic diagram of the CG block for the proposed P-LU SAR ADC architecture and its timing diagram are shown in Figure 6. The CG block generated the clock for DA (Φ_{DA}) and the enable signals for the latches ($\Phi_{EN\langle 5:0\rangle}$). When Φ_S changed to 1, Φ_{DA} became 1 for amplification, and $\Phi_{EN\langle 5\rangle}$ was enabled to ready $Latch_5$. Then, the DA developed the outputs, D_P and D_M, with different delays depending on the input, and the T_S node became 0 by sensing D_P and D_M to end the amplification. After a delay of an AND gate, Φ_{DA} fell to 0 to reset the DA (i.e., D_P and $D_M \rightarrow 0$). This made T_S node 1, and this triggered the next DA amplification and readied $Latch_4$ with $\Phi_{EN\langle 4\rangle} = 1$, using the Latch EN GEN. This one cycle of loop operation can be summarized as follows.

$$T_{1cycle} = t_{DA,amp} + t_{Logic1} + t_{DA,rst} + t_{Logic2} \quad (3)$$

Here, t_{Logic1}, t_{Logic2}, and $t_{DA,rst}$ represent the time of logic for Φ_{DA} falling, logic for Φ_{DA} rising, and the DA reset, respectively. As t_{Logic1} and t_{Logic2} are related to Φ_{DA} generation through the same logic gates, they will have almost the same values. Equations (2) and (3) imply that the time for DA clock generation should be designed similar to the time for latching (t_{Latch}) + DAC settling (t_{DAC}), as in Equation (4).

$$t_{Logic1} + t_{DA,rst} + t_{Logic2} \approx t_{Latch} + t_{DAC} \quad (4)$$

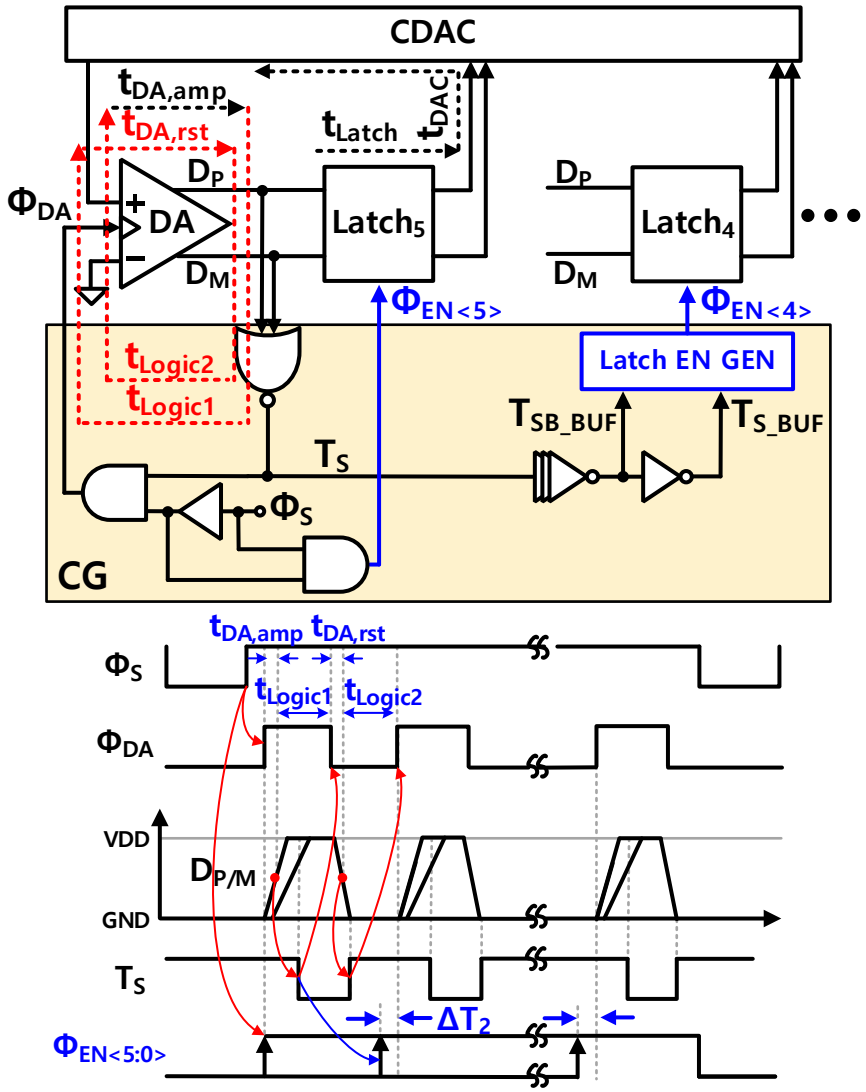

Figure 6. Logic for the CG block in P-LU SAR ADC and the timing diagram.

Based on the comparator design shown in Figure 4, let us discuss the actual timing of the decision loop in more detail. Even though the inserted inverters increased $t_{DA,amp}$ and $t_{DA,rst}$, they could be designed as short as 50 ps and 30 ps, respectively, in nominal condition for our 28 nm process. t_{Logic1} ($\approx t_{Logic2}$) including NOR and AND gates could be designed within 50 ps. As briefly mentioned earlier, there are two prominent design issues related to the CG block, which are moved to the input of the latch (i.e., D_P and D_M).

The first issue regards the parallel operation of the DA reset and the comparator latching. It should be guaranteed that the comparator latching completes before the DA reset, as described in Equation (5).

$$t_{Logic1} + t_{DA,rst} > t_{Latch} \tag{5}$$

Certainly, if $t_{Logic1} + t_{DA,rst} \gg t_{Latch}$ then the speed of the loop operation will be degraded. To verify Equation (5) for our design, a simulation was performed with zero input (i.e., $V_{HP} = V_{HM} = V_{CM}$). Figure 7 shows the timing difference between the DA reset path and the latching path ($\Delta T_1 = t_{Logic1} + t_{DA,rst} - t_{Latch}$) under supply and temperature variation with 1000 samples. Although the conditions varied, ΔT_1 was always positive and guaranteed that the comparator decision was not disturbed by the DA reset.

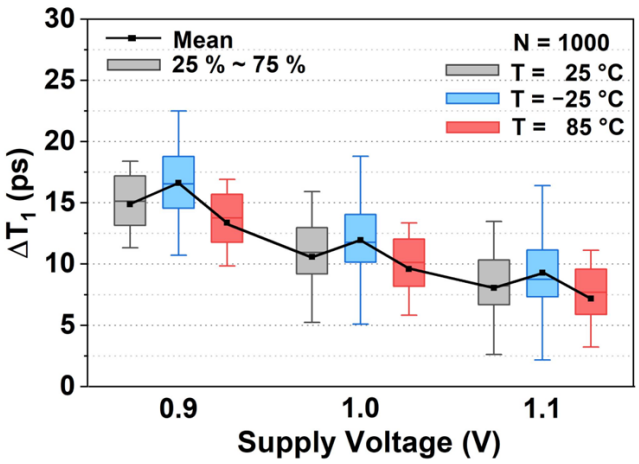

Figure 7. Mean and standard deviation of ΔT_1 ($= t_{Logic1} + t_{DA,rst} - t_{Latch}$) under supply voltage and temperature variation.

The second issue is the timing of the latch enable (Φ_{EN}): as both D_P and D_M reach VDD in a short time by DA amplification, the latch should be enabled as soon as the DA operation begins. Unlike the conventional double-tail comparator, in which the turn-on time of the latch should be carefully controlled [23], in our architecture the latch operation begins only after the rise of the inverter outputs, D_P and D_M (=inputs to the latches), by the DA operation. Therefore, it is enough if Φ_{EN} can be ready earlier than the rising of Φ_{DA} (i.e., $\Delta T_2 > 0$ shown in Figure 6), which provides a sufficient timing margin. Details regarding this follow below.

4.3. High-Speed Logic for Latch Enable Generation

Both Φ_{DA} and Φ_{EN} are generated by T_S, and they will have different delays. In order to satisfy the condition of $\Delta T_2 > 0$ without speed degradation, the logic for Φ_{EN} generation should be fast. In typical SAR ADCs, $\Phi_{EN\langle 5:0\rangle}$ is realized with a shift register. A typical true single-phase clock (TSPC) flip-flops; because the number of stages along the clock-to-output path was three or four, the Φ_{EN} generator (Latch EN GEN in Figure 6) was custom-designed as shown in Figure 8a. This circuit included only two stages to generate each Φ_{EN} and enhanced the overall speed of the logic.

The operation of the Latch EN GEN can be explained with its timing diagram, shown in Figure 8b. During $\Phi_S = 0$, all $\Phi_{EN\langle 5:0\rangle}$ were reset. After sampling ($\Phi_S = 1$), if the first DA conversion of the MSB cycle was complete, T_{S_BUF} became 0, and T_{SB_BUF} became 1. Therefore, the MN node of the first block was discharged to GND, and $\Phi_{EN\langle 4\rangle}$ was enabled. Starting with the falling edge of T_S, the number of logic gates for generating the rising edge of Φ_{DA} was the same as that for generating the rising edge of Φ_{EN}, but the reset time of DA ($t_{DA,\,rst}$) was added to the path of generating Φ_{DA}. Therefore, this design still guaranteed $\Delta T_2 > 0$. When DA reset again, T_{S_BUF} became 1, and the output (Q) of the first block became 1 to make $\Phi_{EN\langle 3\rangle}$ ready. By repeating this operation, each Φ_{EN} for SAR conversion was generated. With the designed clock path and the proposed inverter-inserted three-stage comparator, the design condition of $\Delta T_2 > 0$ was verified.

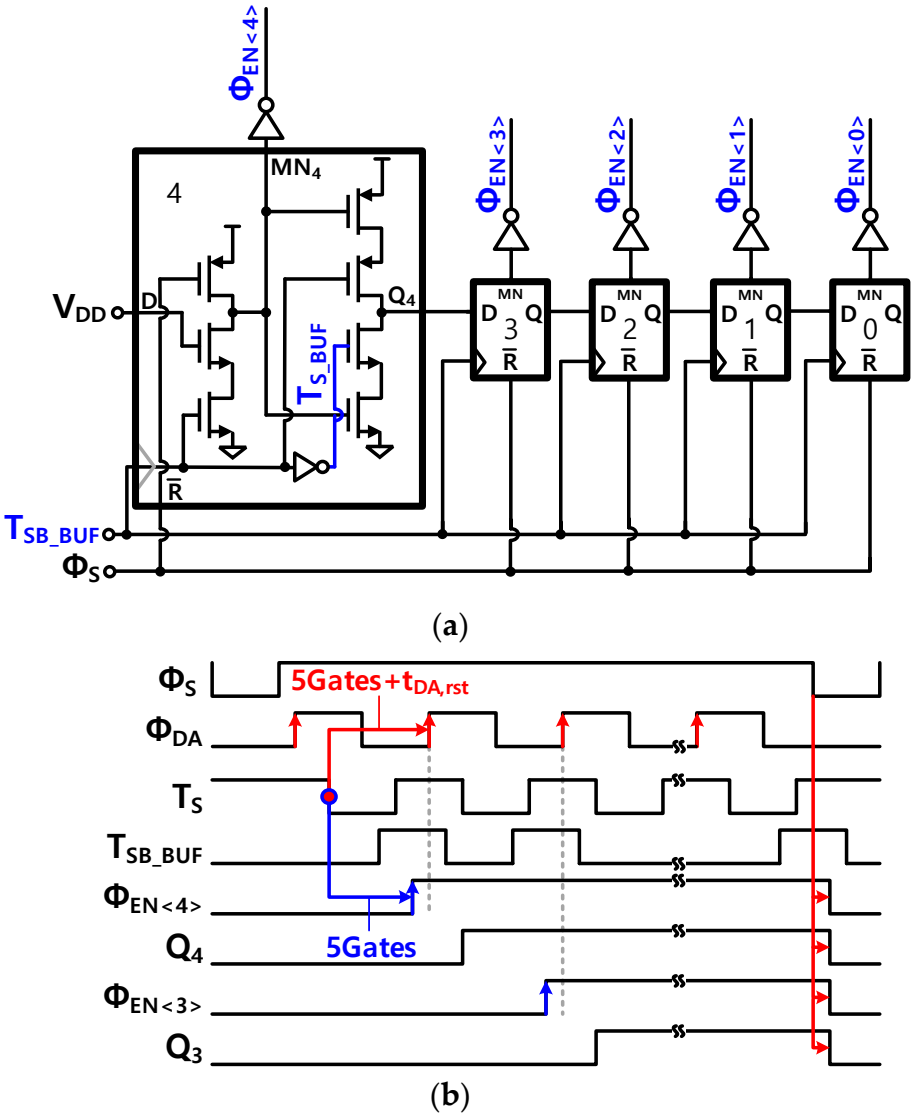

Figure 8. Latch EN GEN with domino logic using tri-state inverters. (**a**) Block and (**b**) timing diagrams.

Figure 9 provides the simulation results of ΔT_2 with 1000 samples. Despite the supply and temperature variation, ΔT_2 was always positive and larger than 5 ps. This means that each Φ_{EN} was ready earlier than the rising of Φ_{DA}, as desired.

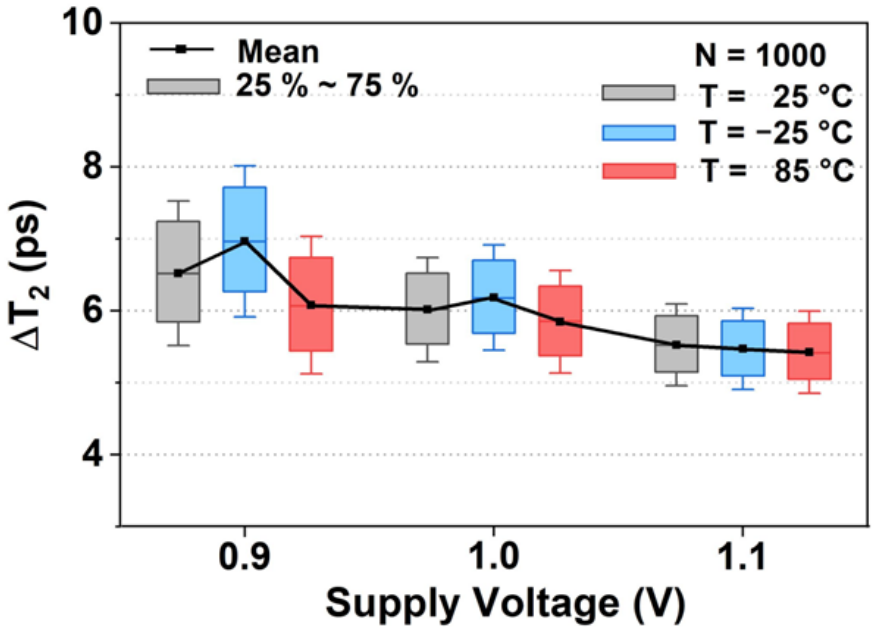

Figure 9. Mean and standard deviation of ΔT_2 (rising edge of Φ_{DA} minus the rising edge of Φ_{EN}) under supply voltage and temperature variation.

5. Measurement Results

A prototype 6-bit calibration-free P-LU SAR ADC was designed to have a 700 MS/s conversion rate in a 28 nm CMOS process. Figure 10 shows a die photograph. Since the LU SAR conversion is possible without a calibration engine by utilizing the ST-DA and the inverter-inserted comparator, the proposed ADC can be designed as compact as the conventional asynchronous SAR ADCs with enhanced conversion speed. As a result, the core area of the proposed P-LU SAR ADC including sampling network, DA, latches, clock generator, and CDAC was 30 µm × 40 µm.

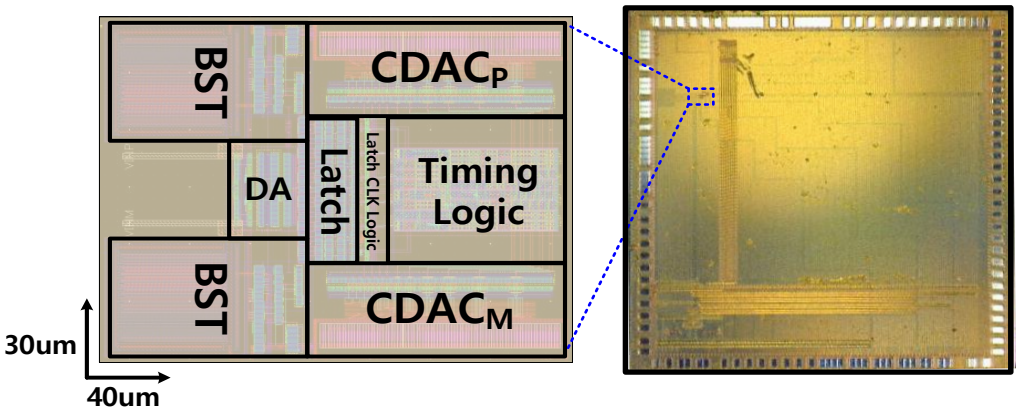

Figure 10. Die photograph.

The measured DNL and INL are shown in Figure 11. With the application of the ST-DA and the inverter-inserted comparators, the peak DNL and INL values were −0.33/+0.31 LSB and −0.13/+0.27 LSB, respectively.

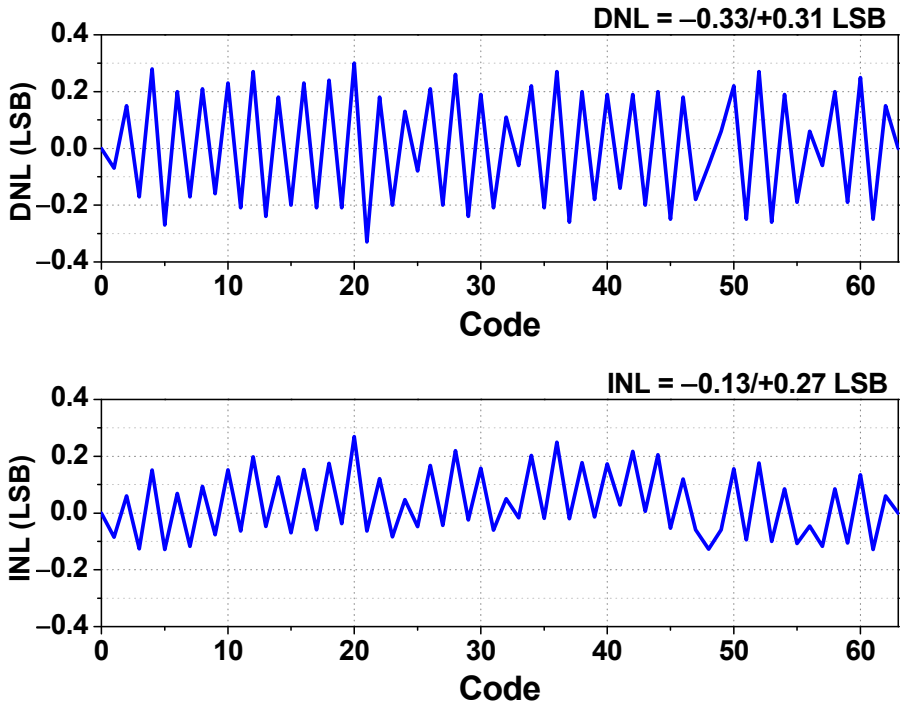

Figure 11. Measured DNL and INL.

The measured signal-to-noise and distortion ratio (SNDR) and spurious-free dynamic range (SFDR) results of five samples with a 349.74 MHz input at a 700 MS/s are shown in Figure 12. The SNDR and SFDR for the five samples were above 34 dB and 47 dB, respectively. Although the number of measurement samples was rather limited, these measurement results indirectly showed that the proposed ADC could achieve good performance without an offset calibration.

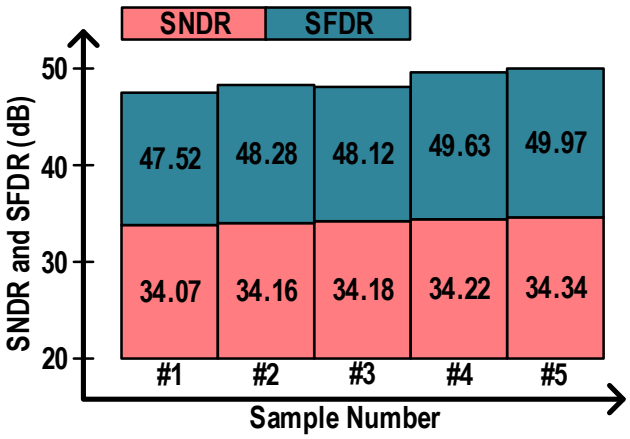

Figure 12. Measured SNDR and SFDR from five different samples near Nyquist input at 700 MS/s.

Figure 13 shows the fast Fourier transform (FFT) results of the minimum (Figure 13a: Sample #1) and maximum (Figure 13b: Sample #5) SNDR among the five samples shown in Figure 12. As shown in Figure 13a, the minimum SNDR and SFDR were 34.07 dB and 47.52 dB, respectively, and the effective number of bits (ENOB) was 5.36 bits even without comparator offset calibration.

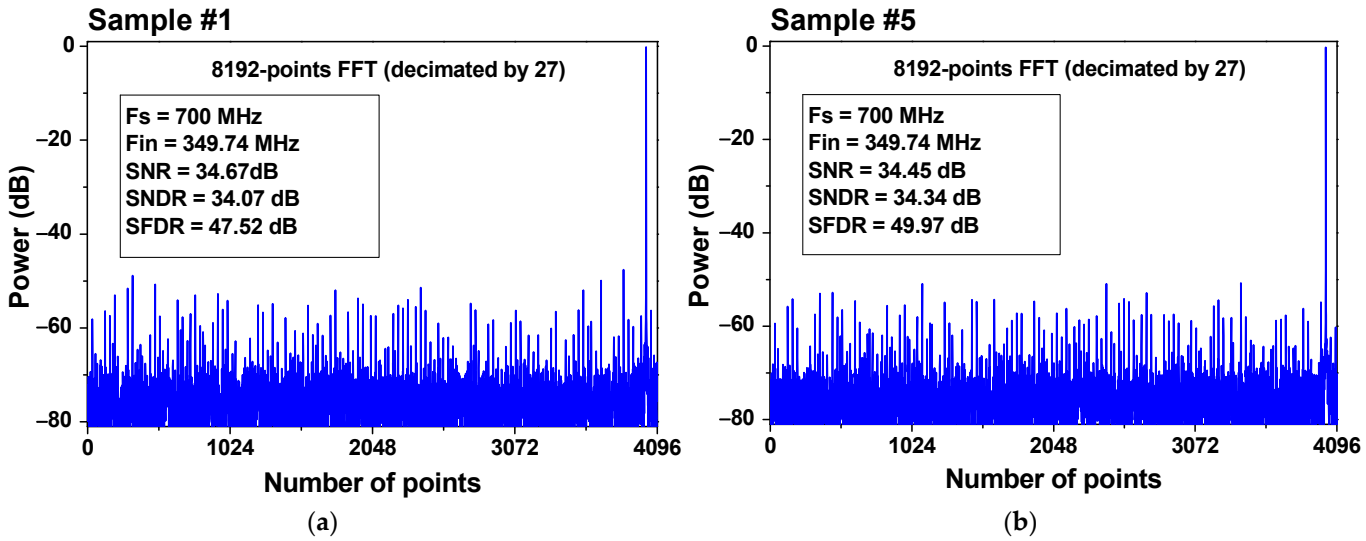

Figure 13. Measured FFT spectrums with a 349.74 MHz input at a 700 MS/s sampling rate. (**a**) Sample #1. (**b**) Sample #5.

The dynamic performances with various input frequencies and sampling rates are shown in Figure 14a,b, respectively. Below 200 MHz input frequency, the SFDR degraded due to a measurement environment issue, but the SNDR was very linear up to the Nyquist input frequency. Moreover, the SNDR was quite constant regardless of the sampling rate.

Figure 15 shows the measured SNDR and SFDR with various supply voltages. Even with ±10% supply variation, the ADC performance stayed constant in the condition of a 249.82 MHz input at 500 MS/s.

The prototype ADC operated under a 1 V supply and consumed 1.0 mW power at a 700 MS/s sampling rate. Figure 16 shows the power breakdown. For the gain of the ST-DA to reduce the input-referred offset mismatch and the high-speed design of the latch, the power consumption of the ST-DA, inverters, and six latches was the highest at 41%, followed by the CG block with 31%.

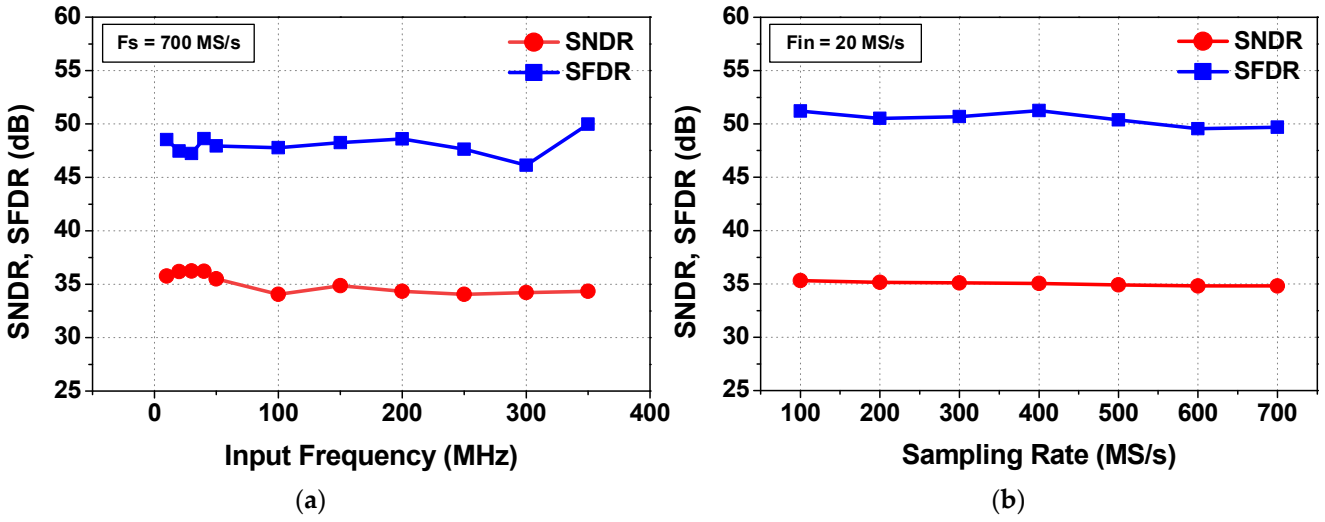

Figure 14. Measured SNDR and SFDR with various (**a**) input frequencies at 700 MS/s, (**b**) sampling rates with a 20 MHz input.

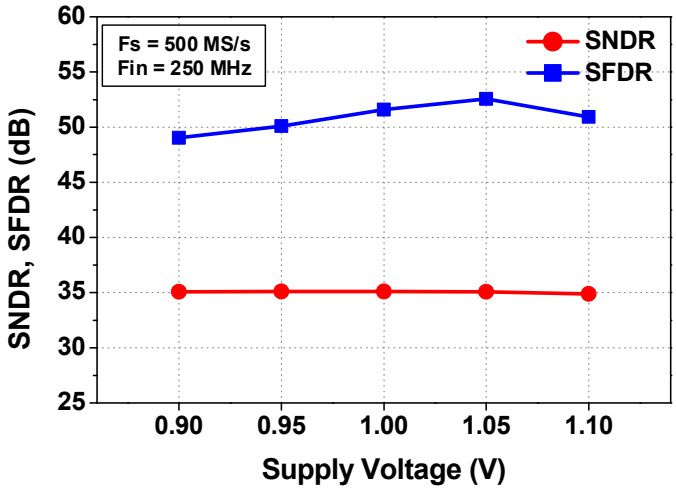

Figure 15. Measured SNDR and SFDR with various supply voltages within ±10%.

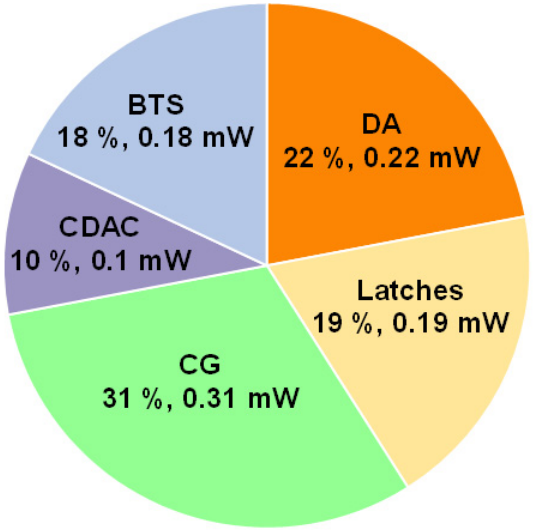

Figure 16. Power breakdown.

In Table 2, the performance of the proposed ADC is summarized and compared with those of recently reported 6–8 bits ADCs with sampling frequency and architecture similar to our design. The proposed ADC was designed with competitive conversion speed compared to the previously reported LU SAR ADCs. In addition, thanks to the P-LU SAR architecture with shared DA and an inverter-inserted comparator, the proposed ADC did not require offset calibration. In the LU SAR ADC, since the comparator does not reset until the SAR conversion is finished, the input kickback error accumulates in the CDAC every comparison cycle [18]. Therefore, as in [18], the LU SAR ADC should also consider the offset calibration for the input common change. On the other hand, in the proposed P-LU SAR ADC, since the six latches share one DA that repeats reset and trigger every comparison cycle, the proposed P-LU SAR ADC is very linear without an additional calibration circuit. As a result, the core area was designed to 0.002 mm^2, which was the smallest among the compared ADCs as shown in Table 2. Therefore, the proposed P-LU SAR ADC can be used as compact single channel ADC for high-speed TI ADC. The achieved Walden figure-of-merit (FOM) was competitive at 34.6 fJ/conversion step.

Table 2. Performance comparison.

	This Work	**ESSCIRC16 Ragab [19]**	**TCAS17 Chen [16]**	**TCAS18 Chung [21]**	**TCAS21 Akkaya [18]**	**CICC19 Li [25]**	**JSSC21 Oh [22]**	**JSSC16 Chan [26]**	**ISSCC21 Kiene [27]**
Architecture	P-LU SAR	LU SAR	LU SAR	LU SAR + SAR	LU SAR	2–3b/cycle	SAR-Flash	TI 3b/cycle	TI LU SAR
# of channels	1	1	1	1	1	1	1	4	2
Technology (nm)	28	40	40	55	28(FDSOI)	40	28	65	40
Resolution (bit)	6	8	6	6	8	7	8	6	6
F_S (GS/s)	0.7	0.35	0.7	1.3	0.8	0.9	1	5	0.9
Area (mm^2)	0.0012	0.024 [1]	0.004	0.03	0.0037	0.014	0.0056	0.09	0.045
Supply (V)	1.0	1.1	1.2	1.2	1.0	1.1	1.1	1.0	1.1
DNL_{MAX} (LSB)	0.33	0.9	0.9	0.78	0.74	0.5	0.59	1.4	0.5 [1]
INL_{MAX} (LSB)	0.27	0.9	0.6	0.85	0.65	0.8	0.82	0.95	0.5 [1]
C_{IN} (fF)	32	249	30.4	32	64	25.2	64	31	63.5
$SNDR_{@Nyq.}$ (dB)	34.0	43.7	34.8	30.5	42.5	39.7	45.5	30.7	33.4
$SFDR_{@Nyq.}$ (dB)	47.5	59.5	47.8	36.3	50.7	54.8	59.4	43.1	48.4
Power (mW)	1.0	1.37	0.95	3.5	2	2.6	2.55	5.5	0.7
Walden FOM [2] (fJ/conv.-step)	34.6	31.3	30.0	99	22.8	36.6	16.6	39	20
Offset Calibration	Not needed	Background	Foreground	Not needed	Background	Background	Foreground	Foreground	Foreground

[1] Estimated value. [2] Walden FoM = Power/(2^{ENOB} × Sampling frequency).

6. Conclusions

A 6-bit 700 MS/s calibration-free P-LU SAR ADC was presented in a 28 nm CMOS process. The proposed inverter-inserted three-stage comparator with a shared DA removed the mismatches of the input transistors. Moreover, the mismatches of the latches were reduced by the gain of the DA. Therefore, this design relaxes the burden of calibration in LU SAR ADC, with competitive speed, and enables a compact area. At a 700 MS/s sampling rate, the prototype ADC consumed 1.0 mW under 1 V power supply, and the ENOB was 5.36 bits under Nyquist input. The proposed ADC achieved a Walden FOM of 34.6 fJ/conversion step, and only occupies a core area of 0.0012 mm^2.

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Abbreviations

SAR	Successive approximation register
ADC	Analog-to-digital converter
DA	Dynamic amplifier
ST-DA	Self-triggered DA
LU	Loop-unrolled
P-LU	Pseudo-loop-unrolled
CG	Clock generation
BTS	Bootstrapped
T/H	Track-and-hold
CDAC	Capacitive digital-to-analog converter

SNR	Signal-to-noise ratio
SNDR	Signal-to-noise distortion ratio
SFDR	Spurious-free dynamic range
ENOB	Effective number of bits
DNL	Differential non-linearity
INL	Integrated non-linearity
FoM	Figure-of-merit

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