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Modelling a New Multifunctional High Accuracy Analogue-to-Digital Converter with an Increased Number of Inputs

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Abstract: This paper presents a multi-input analogue-to-digital functional converter manufactured using switched capacitors. A new method of multifunctional analogue-to-digital processing was tested, which allowed the number of inputs to be increased to 10 without compromising accuracy. An algorithm was developed, and the converter's operation was modelled based on this method. It was found that error values are not significantly affected by the number of input voltages. The value of the lowest input voltage has a decisive influence on the conversion time. The examined multi-input analogue-to-digital functional converter performs multiplication, division, exponentiation, and root extraction operations. The exponent of the power and the degree of the root corresponds to the number of inputs of the converter.

Keywords: analogue-to-digital converter; multi-input devices; functional processing; switched capacitors; accuracy

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1. Introduction

When measuring analogue quantities, there is often a need for their functional processing. Moreover, it is desirable to obtain new relations between input and output quantities for information processing. That is why analogue-to-digital functional converters (ADCFs) are so widely used in automation and measuring equipment. At the current stage of development of microelectronics, the use of circuits on switched capacitors is a promising direction in the creation of functional converters. Such ADCFs have a wide range of functionalities with a simple structure and their particular important advantage is that they are able to work with wide range of analogue input signals. Of the many different ADCFs, it advantageously distinguishes itself by the wide range of logarithmic/antilogarithmic ADCF input signals. The functionality of such ADCFs is extended by increasing the number of logarithmic circuits at their input, including the number of inputs being equal to the number of logarithmic circuits. However, the greatest disadvantage of an ADCF with multiple logarithmic circuits is that it is difficult to obtain identical logarithmic circuit characteristics. The lack of identity of the characteristics leads to an increase in the ADCF error and causes the need for additional corrections, which significantly complicates the practical implementation. Therefore, in the current state of integrated circuit technology, it is impossible to produce more than three identical logarithms in a single ADCF chip. Such converters with three inputs are manufactured by the world's leading companies, Analog Devices (AD538), Burr-Broun (4301/2), and National Semiconductor (LH0094),

and they can perform many operations, such as multiplication, division, exponentiation, and square root.

1.1. Problem Formulation

Modern automation and robotics systems devices process an increasing amount of measurement information from object sensors. In order to increase their efficiency, it is necessary to constantly improve the devices that convert analogue signals into digital form, and to increase the number of data inputs. Leading manufacturers of analogue-to-digital converter (ADC) integrated circuits are looking for a compromise between the high metrological performance of the ADC and the number of input signals [1–3]. Most precision ADCs have up to three analogue inputs. Some chips have eight signal inputs. An example is the ADS7830 chip from Texas Instruments. A further increase in the number of input signals requires an analysis of the ADC input unit parameters in terms of error growth. The disadvantages of such converters are the speed reduction due to the alternate connection of each input to the internal ADC with a switch and the low accuracy (up to eight bits). In ADCs using switched capacitors, the parameters are determined by the ratio of the capacitors, not their nominal values. In addition, the modern development of integrated circuit manufacturing in CMOS (complementary metal-oxide semiconductor) technology has enabled the realisation of capacitors with many times higher accuracy compared to resistors (from two to seven times), improving their temperature characteristics and reducing power consumption [4–6]. This greatly simplifies the interworking of the ADC's component blocks (unit components) and allows building a high-speed ADC with high precision. In [6], a comparison of logarithmic and linear ADCs was made on the basis of biomedical applications in which the signals have a wide range. Logarithmic ADCs have been shown to be better in the area of smaller signals, but they have a larger absolute error for large amplitudes. However, linear ADCs have a smaller input range.

Despite significant advances in ADC and ADCF technology, design issues remain unexplored in terms of multifunctional high-accuracy ADCs with an increased number of inputs.

1.2. Analysis of Recent Publications

Scientists and engineers are actively working to develop precise ADCs for various purposes. A comparison of linear and logarithmic ADCs, including those utilising switched capacitors, indicated the applicability of the latter in the small-signal domain [7]. The literature [8,9] considers the use of logarithmic ADCs of 9–10 binary digits and increasing their accuracy using a C–2C matrix and a network of logic elements. In monograph [10], impulse feedback was introduced to increase accuracy of the new converters. Conversion errors of LADCs with successive approximation on switched capacitors are reduced by decreasing the impacts inside the capacitor cell, in particular leakage currents and parasitic charge transfer [11,12]. A significant increase in accuracy was achieved by introducing weight redundancy and calibration algorithms [13–15]. The disadvantage of the above converters is that they cannot process many input voltages. It should be noted that when the number of input signals is greater than three, there is a need for their functional processing, including multiplication, division, exponentiation and so on.

In [16], a new functional analogue-to-digital conversion method was proposed. The method is implemented using switched capacitors with two groups of inputs. This method increases processing speed by adding logarithmic circuit codes over the elements in parallel. The disadvantage of devices implemented with this method is a relatively complex technical solution.

In [17], the functional analogue-to-digital conversion method was used [16] in order to increase the accuracy of measuring the position of the object. However, the possibility of increasing the number of inputs and the impact of their number on the accuracy of processing have not been investigated.

In [18] a multi-input multifunctional ADCF was proposed, which is characterised by a simplified technical solution and increased reliability compared to the device described in [16].

The work [19] is a short summary of research of the theory and practice of functional analogue-to-digital processing methods and means on switched capacitors.

The structure and operation of a logarithmic ADC with pulse feedback are described in [20]. The quantization error of the developed converter does not exceed 0.1%. The feature and advantage of the device is the implementation of a capacitor cell on one capacitor thanks to pulse feedback.

Ref. [21] describes the implementation of the 8-bit logarithmic Pipeline ADC on switched capacitors. The input sample and hold stage and the polarisation switching stage are realised on the switched capacitors. The dynamic range of the input signal is 80 dB. The disadvantage is the limitation of the input signal range to 1 V.

The work [22] describes the logarithmic Pipeline ADC, made in the KMON 0.35 µm technology. Due to the translinear principle, a simple structure and low energy consumption ADC was achieved. The input signal ranges from 0.7 nA to 100 nA. Output code—eight binary digits. In many applications this accuracy is insufficient.

A neurostimulator made in the form of an integrated circuit is described in [23]. It is used in medicine to treat and study neurological disorders, including Parkinson's disease. The neurostimulator includes circuits on switched capacitors: logarithmic ADC, filters, amplifiers, and a 64-channel digital-to-analogue converter. The use of circuits on switched capacitors significantly reduces the power consumption of devices, which is especially important for the performance of integrated circuits.

In [24], it was proposed to develop and implement a miniature LADC, a device with a cyclic architecture. The advantage is low power consumption. It can be used to linearize the characteristics of sensors. Its error below 2% corresponds to six binary digits.

Logarithmic ADCs [11,21,23,24] do not provide an error value of less than 0.4%, and a further reduction in error is associated with a speed decrease due to processing time lengthening from several to tens of milliseconds.

A new logarithmic ADC was proposed in [25]. The device works with a recursive algorithm to improve accuracy and speed. The disadvantage of this device is the relatively complex technical solution.

Papers [26–29] are devoted to linear ADC with indirect voltage-time conversion using Dickson charge pumps. The advantage of this approach is the simplification of technical solutions and increased technological efficiency when implementing them as integrated circuits. In [26], a simple method of designing transmitters based on charge pumps is given to reduce energy consumption. The textbook [27] on charge pumping topologies gives recommendations on the optimal solution for ultra-low power devices. A linear ADC based on a Dickson pump was described in [28], which made it possible to implement a converter without the use of analogue amplifiers and current sources. In ADC [29], low-level signals are amplified by Dickson pumps and time is quantized by simple functional nodes.

In a recent publication [30], the influence of parasitic capacitances of the components of logarithmic ADC converters with successive approximation and a variable logarithm base has been presented.

The novelty in the presented article in comparison with [11,16,19] is the development of an algorithm and modelling of the operation of a multi-input multifunctional analogue-to-digital converter (ADCF) on switched capacitors, which includes two groups of inputs. The voltages applied to the first group will be multiplied and the voltages applied to the second group of inputs will be included in the denominator of the conversion function. The proposed analogue-to-digital functional converter (ADCF) also allows the performance of exponentiation or root extraction operations of any degree. It should be noted that these operations are among the longest in digital information processing.

In the ADCF, they are performed simultaneously with the conversion of the input analogue signal to digital. The value of the exponent of a power or degree of a root corresponds to the number of inputs. For example, for five inputs, applying the same

voltage to them will produce a code at the output corresponding to the fifth power for the first group of inputs or the fifth-degree root for the second group of inputs.

Presented multi-input multifunctional ADCF based on switched capacitors can be used in the generation and processing of signals for electrotherapeutic applications [31,32].

1.3. The Aim of This Work

The aim of this work is to determine the processing errors of multi-input multifunctional ADCF on switched capacitors based on the proposed method and to establish an acceptable number of input voltages that will provide the desired processing accuracy [16]. To achieve this goal, the following tasks were set:

- The development of the work algorithm of a multi-input multifunctional ADCF converter;
- The modelling and, on the basis of its results, estimation of errors in the processing of multi-input multifunctional ADCF.

In the article, we used the methods of computer modelling and computer experiment to study the errors and the equations that we derived from the well-known laws of electrical engineering and electrostatics.

2. Presentation of the Main Research Material

The multi-input multifunctional ADCF is built using switched capacitors with charge redistribution.

Figure 1 shows the graphs illustrating the essence of the transformation method. The input voltages U_{IN1}, U_{IN2}, . . . , U_{INn}, reference voltage U_{ref}, the compensation voltage U_k, and the number of dosing—processing steps i_k are shown.

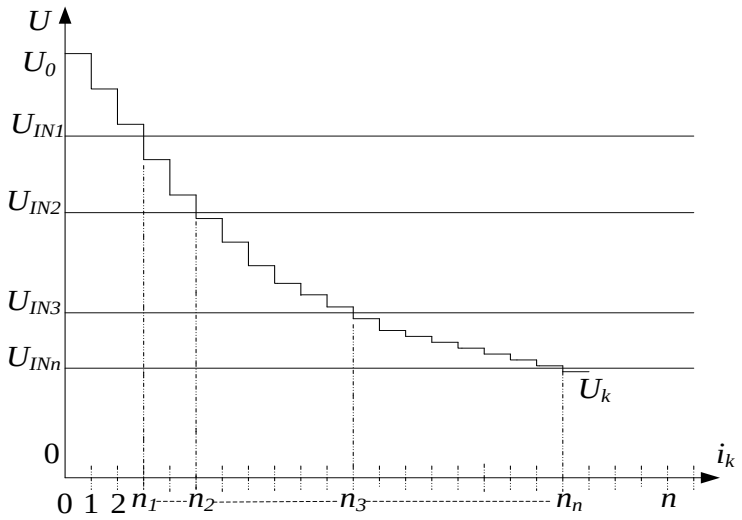

Figure 1. Voltage diagrams of a new method for functional analogue-to-digital conversion.

During processing, the compensation voltage U_k is varied by metered amounts starting from the reference voltage level U_{ref} and compared with the input voltages U_{IN1}, U_{IN2}, . . . , U_{INn}.

Processing takes place until the state of all the comparators, which compare the compensation voltage with each of the input voltages, changes.

The comparator to which the lowest input voltage is connected will operate last.

When processing is complete, a code will be stored in the reversing counter to which the outputs of the logarithmic circuits were sequentially connected:

$$N_c = \frac{1}{\ln \zeta} \cdot \left(\sum_{d=1}^{m} \ln \frac{U_{1d}}{U_{ref}} - \sum_{k=1}^{p} \ln \frac{U_{lk}}{U_{ref}} \right) \quad (1)$$

where: d—is the number of logarithmising circuits of the first group, connected to the additive input of the reversing counter, where d varies from 1 to m;

k—is the number of logarithmising circuits of the second group connected to the subtractive input of the reversing counter, where k varies from 1 to p.

The result of the entire transformation will be created in an anti-logarithmising circuit based on the output code of the reversing counter:

$$N_{fp} = anty \ln N_c \quad (2)$$

According to the new method of functional analogue-to-digital processing proposed in [16] and the diagrams illustrating its operation (Figure 1), a generalised operating algorithm was developed as shown in Figure 2.

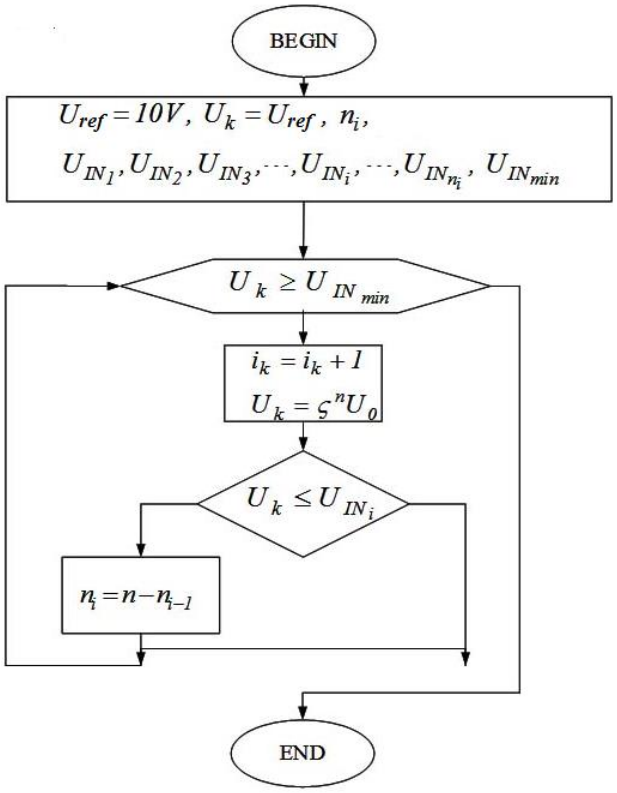

Figure 2. Generalised block diagram of the algorithm of operation of a multi-input multifunctional ADCF.

Figure 2 includes: U_k—compensation voltage, $U_{IN\ min}$—the smallest of the input voltages, U_{ref}—reference voltage, i_k—number of dosing—processing steps, n_i—number of logarithmising circuit capacitor cells in which processing takes place.

The total number of input voltages to be processed by the device shall be given as initial data. It should be noted that in the implementation of the circuit it does not matter which inputs are supplied with a higher or lower voltage. To simplify the algorithm and programme, the input voltages were set in descending order in the computer simulation.

For the total processing time, we take the processing time of the lowest input voltage, which is the longest. The processing of other input voltages is performed in parallel and will finish earlier. The processing time is estimated based on the number of doses—processing steps i_k.

To determine other initial data, such as the nominal output code or the maximum permissible error, it is necessary to determine the logarithm base. To select the logarithm

base, we use the value of the processing error we want to obtain. Then, the base of the logarithm is determined by the expression:

$$\zeta = \frac{1}{1 + \frac{\delta}{100\%}} \tag{3}$$

where: δ—is the value of the desired error expressed as a percentage.

In converters with charge redistribution, ζ is defined by the ratio of the capacitances of the storage and metering capacitors

$$\zeta = \frac{C_D}{C_D + C_A} < 1 \text{ where } C_D << C_A$$

The physical value of the logarithm base will be determined by the ratio of C_D and C_A capacities, in particular for ζ = 0.999 and δ = 0.1%, the capacitance value C_D = 1 nF and C_A = 1 µF.

The output data illustrate the extent of processing. This is the range of permissible values of the analogue signal within the scope of the reference voltage to the minimum value of the input voltage. The range has been established from U_{ref} = 10 V do $U_{IN\ min}$ = 0.001 V, i.e., in the range 1 mV–10 V. This corresponds to the best solutions of logarithmic converters. Using the processing range, the nominal output code (N_{nom}) can be determined from the selected logarithm base ζ = 0.999:

$$N_{nom} = \frac{1}{\ln \zeta} \cdot \ln \frac{U_{\min}}{U_{\max}} \tag{4}$$

The above relationship for ζ = 0.999 suggests that the nominal code is N_{nom} = 9214.

The initial value of the compensation voltage is assumed to be equal to the reference voltage. Further processing takes place by reducing the compensation voltage as illustrated in Figure 1.

The maximum absolute and relative errors for the multifunctional ADCF can be estimated using the expressions

$$\Delta U_n = \zeta^{n-1}(\zeta - 1)U_{ref} \text{ and } \delta_{U_n} = \frac{\zeta^{n-1}(\zeta - 1)U_{ref}}{10} \cdot 100\% \tag{5}$$

It should be noted that the conversion error is taken into account over the entire range of operation, i.e., up to 10 V.

The conversion error of each individual input voltage will be obtained from the set value of the input voltage and the value of the compensation voltage at which the comparator state of the corresponding logarithmising circuit changes.

If the compensation voltage is equal to the *i*-th input voltage, the state of the corresponding comparator is changed, processing at this input is terminated. The number of doses—conversion steps i_k and the corresponding code from the N_i logarithmic circuit shall be determined, taking into account the number of input voltages whose conversion is completed.

3. Analysis of the Study Results

This paper presents the test results of the developed algorithm for an ADCF converter with five input voltages. Various combinations of any five input voltages in the range 1 mV–10 V were analysed.

The results obtained for an assumed relative error of 0.1%, corresponding to a 10-bit converter word and a logarithm base of ζ = 0.999, are shown below.

For input voltages U_{IN1} = 9.5 V; U_{IN2} = 7.5 V; U_{IN3} = 6 V; U_{IN4} = 2.44 V; U_{IN5} = 0.99 V (Figure 3a), the maximum error, according to relation (5), does not exceed 0.09%.

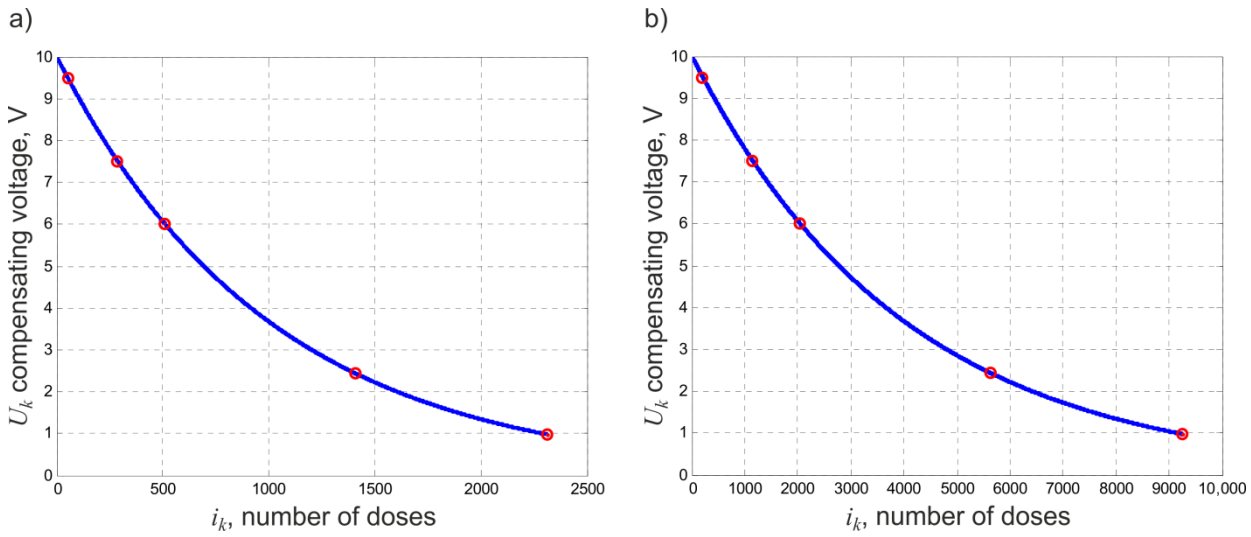

Figure 3. Operation graphs of the multifunctional ADCF converter for five input voltages: U_{IN1} = 9.5 V; U_{IN2} = 7.5 V; U_{IN3} = 6 V; U_{IN4} = 2.44 V; U_{IN5} = 0.99 V for the given errors: (**a**) 0.1% and (**b**) 0.025%.

The simulation showed that the relative error values for each input voltage are: δ1 = 0.06%, δ2 = 0.01%, δ3 = 0.05%, δ4 = 0.008%, δ5 = 0.002%, i.e., not exceeding the maximum permissible error.

The numerical values of the output code are formed from the corresponding numbers of dosing pulses and vary according to the mathematical function implementing the ADCF according to relation (1). For the example shown in Figure 3, i.e., for five input voltages, when they are multiplied, we obtain:

$$\begin{aligned} N_{out} &= \frac{1}{\ln\zeta}\cdot\left(\sum_{d=1}^{5}\ln\frac{U_d}{U_{ref}}\right) = \\ &= \frac{1}{\ln\zeta}\cdot\left(\ln\frac{U_{IN1}}{U_{ref}}+\ln\frac{U_{IN2}}{U_{ref}}+\ln\frac{U_{IN3}}{U_{ref}}+\ln\frac{U_{IN4}}{U_{ref}}+\ln\frac{U_{IN5}}{U_{ref}}\right) \end{aligned} \tag{6}$$

This value corresponds to the ideal value of the output code. Each component of expression (6) corresponds to the number of doses i_k or processing steps n_i of each of the input voltages. Therefore, the converter output code value can be represented as:

$$N_{out} = i_{k_1} + i_{k_2} + i_{k_3} + i_{k_4} + i_{k_5} \tag{7}$$

where: $i_{k_1} = n_1, i_{k_2} = n_2, i_{k_3} = n_3, i_{k_4} = n_4, i_{k_5} = n_5$—number of doses needed to convert each input voltage $U_{IN1} \div U_{IN5}$.

The code from expression (7) corresponds to the output code obtained during the simulation. The summation error of the processing code is determined by a known formula, taking into account expressions (6) and (7) and the nominal code value.

The same is true when multiplying and dividing the input voltages by the ideal output code value:

$$\begin{aligned} N_{out} &= \frac{1}{\ln\zeta}\cdot\left(\sum_{d=1}^{3}\ln\frac{U_d}{U_{ref}}-\sum_{k=1}^{2}\ln\frac{U_k}{U_{ref}}\right) = \\ &= \frac{1}{\ln\zeta}\cdot\left(\ln\frac{U_{IN1}}{U_{ref}}+\ln\frac{U_{IN2}}{U_{ref}}+\ln\frac{U_{IN3}}{U_{ref}}-\ln\frac{U_{IN4}}{U_{ref}}-\ln\frac{U_{IN5}}{U_{ref}}\right) \end{aligned} \tag{8}$$

Then, the output code value obtained during the simulation will correspond to:

$$N_{out} = i_{k_1} + i_{k_2} + i_{k_3} - i_{k_4} - i_{k_5} \tag{9}$$

In the example (Figure 3a), when multiplying all input voltages $f = U_{IN1} \cdot U_{IN2} \cdot U_{IN3} \cdot U_{IN4} \cdot U_{IN5}$, the output code was obtained with a total relative error of 0.025%, and by realising the function $f = \frac{U_{IN1} \cdot U_{IN2} \cdot U_{IN3}}{U_{IN4} \cdot U_{IN5}}$, it was less than 0.015%.

The reduction in multiplication and division error is achieved through partial error compensation, as the relative errors of the numerator and denominator have different signs.

Processing took 2314 cycles, which is less than 5.8 ms. The results obtained correspond to the processing of a device with a converter word length greater than 10 bits, i.e., a 12-bit converter.

For a 12-bit multifunctional ADCF converter, the converter error is 0.025% and the logarithmic basis is $\zeta = 0.99975$. The logarithm base $\zeta = 0.99975$ corresponds to the capacitance of the metering and storage capacitors with respective capacitances of $C_D = 1$ nF and $C_M = 3.9$ µF. A further reduction in processing errors was achieved. Namely, for the above example of the input voltage set (Figure 3b), the maximum error for this case according to (5) is 0.023745%, which is less than 0.025%. The nominal output code according to (4) is $N_{nom} = 36842$.

For each of the input voltages, the following errors were obtained by simulation (Figure 3b): $\delta 1 = 0.02\%$, $\delta 2 = 0.002\%$, $\delta 3 = 0.007\%$, $\delta 4 = 0.003\%$, $\delta 5 = 0.0007\%$.

When performing the multiplication function of all input values (Figure 3b) $f = U_{IN1} \cdot U_{IN2} \cdot U_{IN3} \cdot U_{IN4} \cdot U_{IN5}$, an output code with a relative error of less than 0.006% was obtained, and performing the function $f = \frac{U_{IN1} \cdot U_{IN2} \cdot U_{IN3}}{U_{IN4} \cdot U_{IN5}}$, an output code with a relative error of less than 0.0015% was obtained.

The processing time is 9252 doses, corresponding to 23 ms.

The results obtained correspond not to 12-bit processing, but 14-bit processing.

Figures 4 and 5 show error graphs over the entire processing range for the voltage and processing time of the multifunctional ADCF converter with five input voltages. The following symbols have been adopted for the graphs: "blue *" for the 10-bit converter and "red o" for the 12-bit converter.

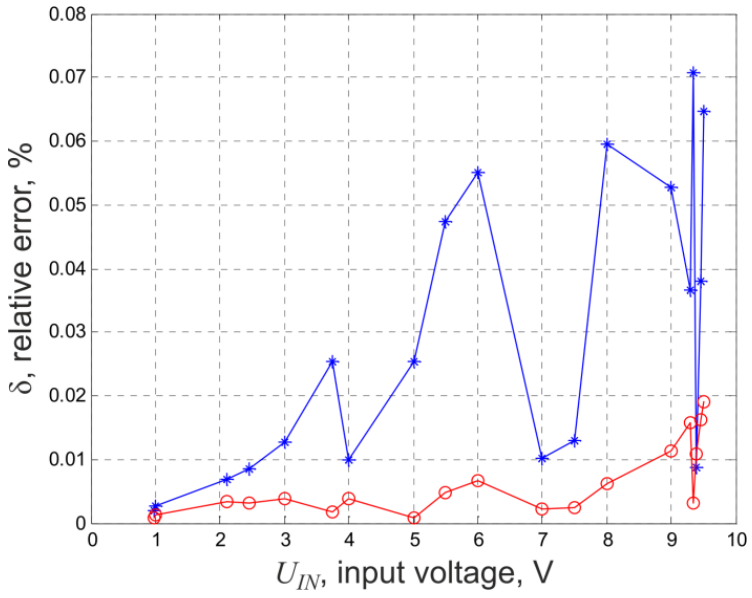

Figure 4. Graphs of the processing error of the multifunctional ADCF converter: 10-bit (blue *) and 12-bit (red o), for five input voltages.

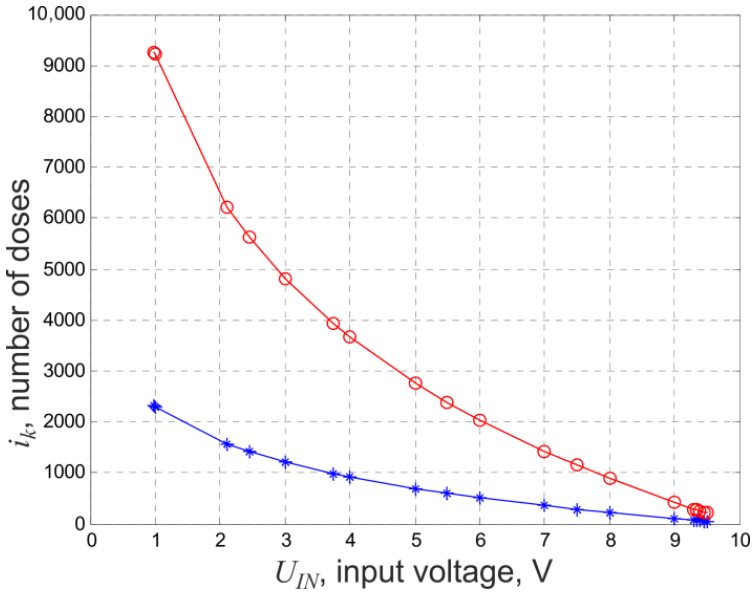

Figure 5. Graphs of processing time of the multifunctional ADCF: 10-bit (blue *) and 12-bit (red o), for five input voltages.

Summarising the results of modelling various combinations of any five input voltages in the range 1 mV to 10 V for the 10-bit and 12-bit ADCF, we can conclude that the relative conversion errors for most input voltages are less than 0.07% and 0.019%, respectively. These errors decrease as these voltages decrease and do not exceed 0.019% for voltages less than 1 V. The processing time increased from 125 µs (50 doses) and 515 µs (206 doses) at the upper end of the range to 5.75 ms (2300 doses) and 23 ms (9200 doses) for input voltages below 1 V, respectively.

The output code errors when converting 5 input voltages for the 10-bit ADCF both when multiplying and multiplying and dividing the input voltages are 0.013–0.025%, while for the 12-bit converter they are 0.0015–0.003%. This means that the errors obtained are 4–6 times smaller than assumed. This corresponds to the errors of converters with a slightly higher bit rate (by 2–3 bits).

Similar simulations were performed for 10 input voltage values for 10-bit ($\zeta = 0.999$) and 12-bit ($\zeta = 0.99975$) converters. It is advisable to separate the area of input voltages close to the top of the range, i.e., up to 10 V, and the area of input voltages close to the bottom of the scop, i.e., close to 1 V.

Figure 6 shows graphs of the total voltage errors in the Figure 6a,b parts of the input voltage range for a ten-input multifunctional ADCF. Figure 7 shows graphs of the duration of voltage processing in the Figure 7a,b parts of the input voltage range for a ten-input multifunctional ADCF. The charts use the following designation: "blue x" for the 10-bit converter, and "red o" for the 12-bit converter.

Summarising the results of modelling various combinations of any ten input voltages in the range 1 mV–10 V for the 10-bit and 12-bit ADCF, we can conclude that the relative conversion errors for most input voltages are less than 0.09% and 0.019%, respectively, these errors decrease with the decrease of these voltages and do not exceed 0.0026% and 0.0013% for voltages less than 1 V.

The conversion time of the converters increased from 250 µs (100 doses) and 1 ms (400 doses) at the upper end of the range, respectively, to 5.75 ms (2300 doses) and 23 ms (9200 doses) for input voltages below 1 V.

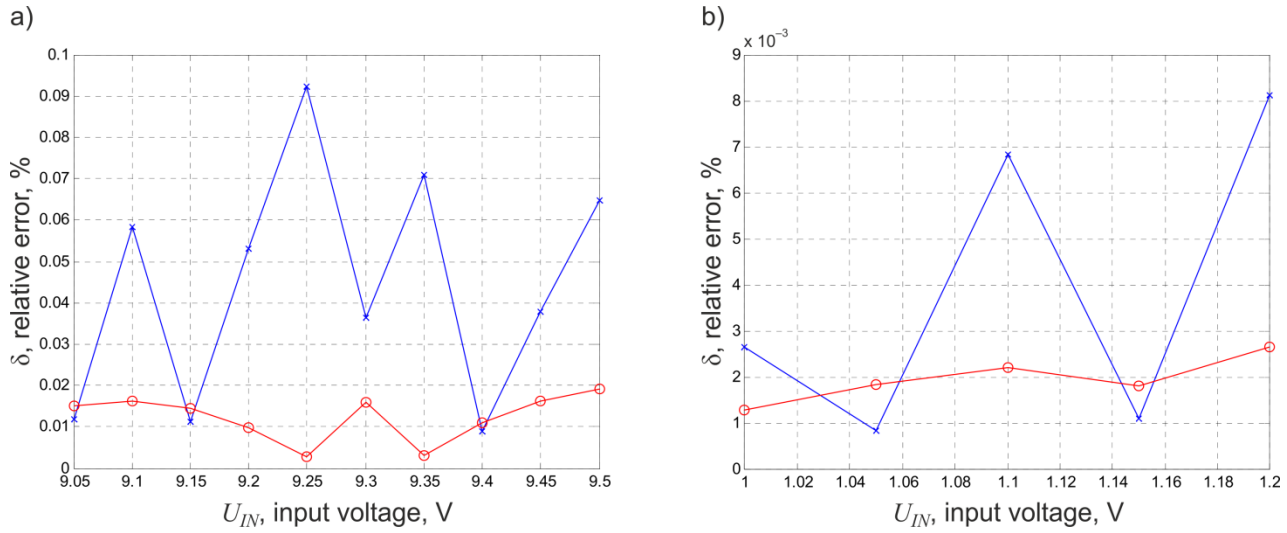

Figure 6. Graphs of the relative processing error of the multifunctional ADCF converter for 10 input voltages and set errors of 0.1% (blue x) and 0.025% (red o): (**a**) for the upper part of the operating range; (**b**) for the lower part of the operating range.

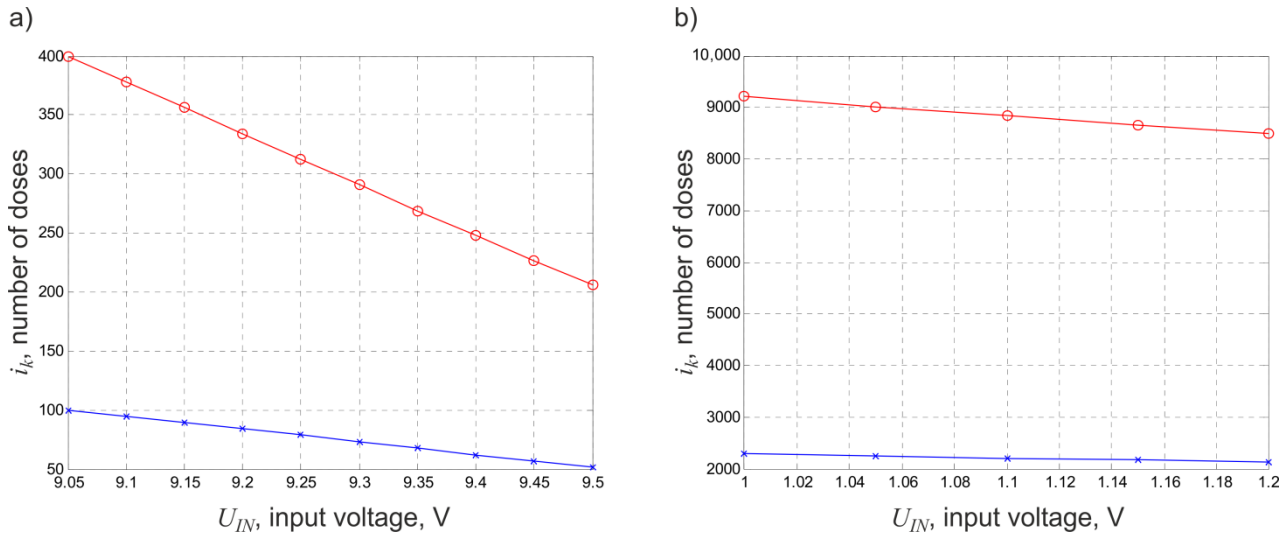

Figure 7. Processing time diagrams of the multifunction ADCF converter for 10 input voltages and set errors of 0.1% (blue x) and 0.025% (red o): (**a**) for the upper part of the operating range; (**b**) for the lower part of the operating range.

The output code errors when processing the 10 input voltages are 0.025–0.05% for the 10-bit ADCF and 0.0035–0.017% for the 12-bit ADCF. This means that the errors obtained are 1.5–4 times smaller than assumed. This corresponds to a processing error with a bit size that is 1–2 binary digits higher than set.

It can be concluded that the presented method of multifunctional analogue-to-digital conversion [16] allows processing more than three input voltages, which was proved in the presented analysis for input voltages from 5 to 10. In this method, the maximum permissible error can be set (selected) by the user before the processing begins.

Table 1 presents a summary of the results of the modelling of multi-input multifunctional ADCF.

Table 1. Summary of the results of modelling of multi-input multifunctional ADCF.

Name	Units	5 Inputs	5 Inputs	10 Inputs	10 Inputs
Input voltage range	V	10–0.001	10–0.001	10–0.001	10–0.001
Output code	bit	10	12	10	12
Rated value of the relative error	%	0.1	0.025	0.1	0.025
Maximum actual value of the relative error for input voltages from 10 V to 1 V in multiplication—division	%	0.025	0.003	0.05	0.017
The maximum actual value of the relative error for input voltages below 1 V in multiplication—division	%	0.015	0.0015	0.025	0.0035
Maximum processing time for input voltages from 10 V to 1 V in multiplication—division	mS	0.125	0.515	0.25	5.75
Maximum conversion time for input voltages less than 1 V for multiplication—division	mS	5,75	23.0	1.0	23.0

4. Conclusions

As a result of the conducted research:

1. The multifunctional ADCF work algorithm with the number of input voltages from 5 to 10 was developed. Its advantage is the possibility to set the desired conversion error before conversion begins, the value of which is determined by the logarithm base.
2. Based on the multifunctional modelling of the multifunctional ADCF with the number of input voltages from 5 to 10, it can be concluded that in the range of input signals from 10 V to 1.0 mV:
    - The maximum real value of the relative ADCF error on 10 and 12 bits does not exceed 0.025% and 0.003% for five inputs and 0.05% and 0.017% for 10 inputs, respectively;
    - The maximum ADCF conversion time for 10 and 12 bits does not exceed 0.125 mS and 0.515 mS for five inputs and 0.25 mS and 5.75 mS for 10 inputs, respectively;
    - The error values of the output code are on average four and two times lower than the nominal value for 5 and 10 ADCF inputs, respectively, that is, the ADCF has two- and one- digit precision with respect to the nominal value;
    - The multi-input ADCF converter can perform multiplication, division, exponentiation, and root extraction operations without any reduction in accuracy;
    - The value of the lowest of the input voltages is decisive for the speed of conversion: the lower the input voltage is, the longer the processing time.
3. The use of modelling results gives the possibility of increasing the accuracy of multi-input ADCFs and extending the scope of their application in various systems for the functional processing of information from a large number of sensors. The latter include automation, information and measurement systems, aviation, space, and many others.

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