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Effects of Varying the Fin Width, Fin Height, Gate Dielectric Material, and Gate Length on the DC and RF Performance of a 14-nm SOI FinFET Structure

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Abstract: The FinFET architecture has attracted growing attention over the last two decades since its invention, owing to the good control of the gate electrode over the conductive channel leading to a high immunity from short-channel effects (SCEs). In order to contribute to the advancement of this rapidly expanding technology, a 3D 14-nm SOI n-FinFET is performed and calibrated to the experimental data from IBM by using Silvaco TCAD tools. The calibrated TCAD model is then investigated to analyze the impact of changing the fin width, fin height, gate dielectric material, and gate length on the DC and RF parameters. The achieved results allow gaining a better understanding and a deeper insight into the effects of varying the physical dimensions and materials on the device performance, thereby enabling the fabrication of a device tailored to the given constraints and requirements. After analyzing the optimal values from different changes, a new device configuration is proposed, which shows a good improvement in electrical characteristics.

Keywords: FinFET; gate-length downscaling; high-k gate dielectric; RF parameters; SOI; TCAD simulation

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1. Introduction

The structure of the fin field-effect transistor (FinFET) has completely emerged as a promising design solution for CMOS logic and memory circuit design because of its good immunity to short channel effects (SCEs) [1–3]. This technology enables the creation of high-performance ultra-scaled, high-density integration, and high-performance silicon (Si) chips [1–4]. In the silicon industry, device miniaturization is still considered a key feature to achieve better short-channel performance. Currently, a great effort concerns the development of FinFET devices with dimensions below 5 nm that represent the target in the near future [4–8]. Despite the effort made to create devices with dimensions below 5 nm, many aspects still remain to be clarified and optimized, also with a view to a larger-scale application of the devices.

This paper presents an investigation of 3D 14-nm FinFET on thin silicon on insulator (SOI) wafer using Silvaco tools. The SOI technology shows significantly large improvement compared to the previous FinFET technology. For better Si channel controllability, hafnium oxide (HfO_2) was used to cover the Si channel as a gate dielectric. The impact of varying the fin width (W_{fin} = 4, 6.5, 15, and 20 nm), fin height (H_{fin} = 10, 15, 20, 25, 30, and 35 nm), gate dielectric materials (TiO_2, La_2O_3, HfO_2, Al_2O_3, Si_3N_4, and SiO_2), and gate length (L_g = 5, 10, 15, and 20 nm) on the DC and RF performance of the considered structure is carefully analyzed and discussed. The analysis is performed by investigating the following

parameters: threshold voltage (V_{th}), subthreshold slope (SS), drain-induced barrier lowering ($DIBL$), on-state current (I_{on}), off-state current (I_{off}), I_{on}/I_{off} ratio, transconductance (g_m), gate capacitance (C_{gg}), and cut-off frequency (f_T). The development of a comparative analysis enables gaining a better understanding of how to improve device performance, depending on the given fabrication constraints and application requirements.

It should be underlined that the great interest in the FinFET technology is witnessed by the many papers that have been published over the years to investigate the FinFET performance by using both TCAD simulations [8–13] and measurements [14–18]. Although a measurement-based investigation is a mandatory step prior to the use of a device in real applications, the TCAD simulation is considered a powerful and costless type of analysis to optimize device performance. This is because the TCAD tool allows predicting how the device performance changes by varying the design parameters without the need for time-consuming and costly experiments [13].

The rest of this paper is structured as follows: Section 2 presents the device structure, Section 3 describes the developed model for the achieved simulations, Section 4 reports and discusses the obtained findings; and the last section concludes the paper.

2. Device Structure

The 3D 14-nm SOI FinFET device has been simulated using Silvaco TCAD. Figure 1 shows the 3D schematic diagram of the FinFET device with a physical gate length (L_g) of 20 nm. The geometrical parameters and material properties are specified in previously published papers [1–3]. HfO_2 is used as a gate dielectric material. The doping densities of the source (n-type), drain (n-type), and covered fin (p-type) region were 1×10^{21} cm^{-3}, 1×10^{21} cm^{-3}, and 1×10^{16} cm^{-3}, respectively. The contact resistance of 1×10^{-9} Ω.cm^2 was selected for the source/drain region. Table 1 illustrates the physical parameters of the investigated model.

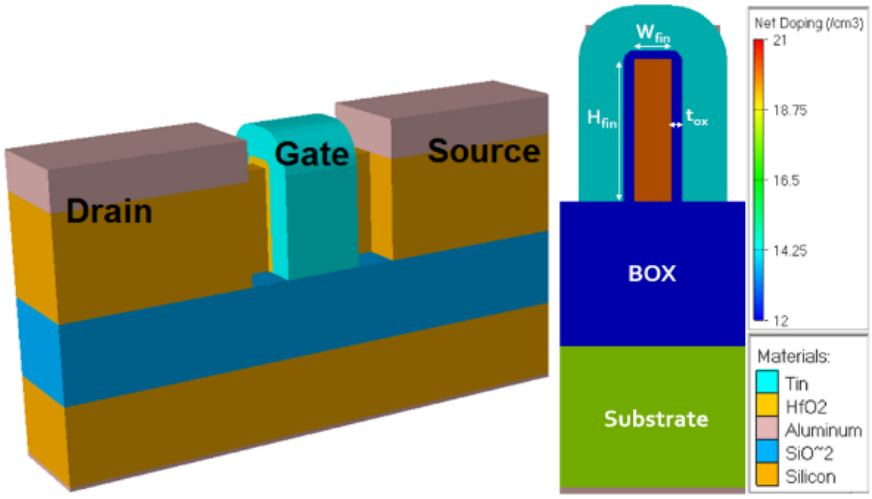

Figure 1. Structure of 3D 14-nm SOI n-FinFET device with a single fin.

Table 1. Device parameters for a 14-nm n-FinFET.

Parameters	Values
Channel length, L_g	20 nm
Fin height, H_{fin}	26 nm
Fin width, W_{fin}	6.5 nm
S/D length, $L_{S/D}$	50 nm
S/D extension length, $L_{S/D}$	7 nm
Buried oxide (SiO_2) thickness, t_{BOX}	50 nm
Gate dielectric (HfO_2) thickness, t_{ox}	4 nm
Channel doping (boron, p-type), N_{ch}	10^{16} cm^{-3}
S/D doping (arsenic, n-type), $N_{S/D}$	10^{21} cm^{-3}
S/D extension doping (arsenic, n-type)	10^{19} cm^{-3}
Si substrate doping (boron, p-type)	10^{16} cm^{-3}
Gate work function (TiN (Sn), Φ_m)	4.32 eV

3. Simulation Model

For device simulation, CVT, CCSMOB, ANALYTIC, BGN, SRH, and Auger recombination were also included. Fermi–Dirac distribution has been enabled. For quantum confinement, the BQP model was considered [13]. By considering a FinFET device based on using one single fin, the effective channel width can be estimated as follows

$$W_{eff} = 2H_{fin} + W_{fin} \tag{1}$$

where H_{fin} is the fin height and W_{fin} is the fin width.

The electron (n) and hole (p) densities with BQP equation can be expressed by [13]

$$n = N_c e^{-\frac{(E_c + qQ)}{k\,T_L}} \tag{2}$$

$$p = N_v e^{-\frac{(qQ\,-\,E_v)}{k\,T_L}} \tag{3}$$

$$Q = \frac{-h^2}{2}\frac{\gamma\nabla\left(M^{-1}\nabla\left(n^{\alpha}\right)\right)}{n^{\alpha}} \tag{4}$$

N_c and N_v are the effective density of states for electrons and holes, respectively. E_c and E_v are the conduction and valence bands, respectively. k is the Boltzmann constant, T_L is the local lattice temperature, q is the electric charge, Q is the quantum potential, M^{-1} is the inverse effective mass tensor, and γ and α are two adjustable parameters.

Device Validation

Initially, the investigated 14-nm SOI n-FinFET model was carefully calibrated according to the experimental data in [1]. In order to match the simulated I–V curves with the experimental data from IBM [1], some physical parameters such as the doping density, thickness, source/drain extension length, and gate work function were carefully adjusted. Figure 2 illustrates simulated I–V characteristics at two different values of V_{ds}: 0.05 V (linear) and 0.8 V (saturation). I–V model curves exactly match with the experimental as is observed at both bias conditions. The device characteristics of the investigated model are compared to the experimental outputs [1] and presented in Table 2. To further validate the developed model, the simulation results were compared also to Sun's work [2]. Figure 3 presents the output I–V characteristics of the investigated model at different gate-source voltages. Figure 3 shows a non-zero current for V_{gs} just above V_{th} and the increase in I_{ds} with increasing input voltage V_{gs}.

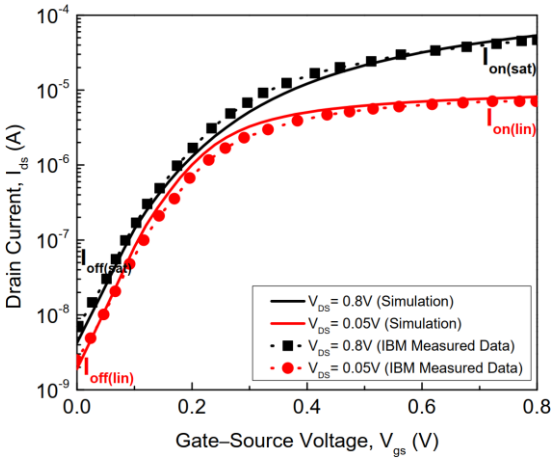

Figure 2. Simulation and experimental I–V curves of the investigated FinFET model [1].

Table 2. Characteristics for the investigated FinFET model.

Device Characteristics	This Work	Ref. [1]	Ref. [2]
V_{dd} (mV)	800	800	800
$V_{th,\,lin}$ (mV)	137	-	162
$V_{th,\,sat}$ (mV)	120	-	147
$I_{on,\,lin}$ (µA)	8.11	7.06	7.64
$I_{on,\,sat}$ (µA)	53.6	-	58.15
$I_{off,\,lin}$ (nA)	1.89	2.51	1.43
$I_{off,\,sat}$ (nA)	4.22	-	2.51
$I_{on,\,lin}/I_{off,\,lin}$	4.29×10^3	-	5.32×10^3
$I_{on,\,sat}/I_{off,\,sat}$	1.27×10^4	-	2.32×10^4
SS_{lin} (mV/dec)	61	67	62.83
SS_{sat} (mV/dec)	64.91	-	63.45
$DIBL$ (mV/V)	43.32	55	20.5

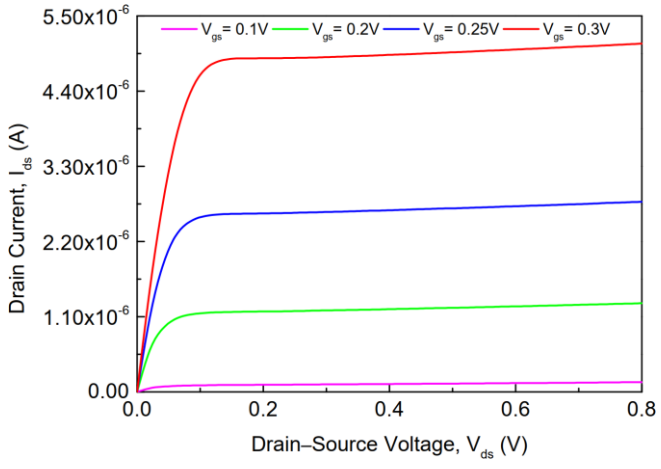

Figure 3. Output I–V curves of the investigated FinFET model with different gate–source voltages.

To evaluate the SCEs, the subthreshold slope (SS) and drain-induced barrier lowering ($DIBL$) are extracted as follows [4,11]

$$SS = \frac{d(V_{gs})}{d[log(I_{ds,sat})]} \tag{5}$$

$$DIBL = \frac{\left|V_{th,\,sat} - V_{th,\,lin}\right|}{V_{DD} - 0.05V} \tag{6}$$

where V_{gs} is the gate-source voltage and $I_{ds,sat}$ is the drain current (under saturated biasing condition). $V_{th,sat}$ and $V_{th,lin}$ are the threshold voltages under saturated and linear conditions, respectively. The values of SS and $DIBL$ are, respectively, 61 mV/dec and 43.32 mV/V for the 14-nm n-FinFET. These parameters are approximately maintained the same as the ones reported in papers [1–4].

The cut-off frequency (f_T) is considered as a crucial RF parameter which defines the speed response of the RF circuit design. The f_T can be expressed by [14–17]

$$f_T = \frac{g_m}{2\pi C_{gg}} = \frac{g_m}{2\pi\left(C_{gs} + C_{gd}\right)} \tag{7}$$

where g_m is the transconductance, C_{gg} is the total gate capacitance, C_{gs} is the gate-source capacitance, and C_{gd} is the gate-drain capacitance.

4. Results and Discussion

In this section, the effects of changing the fin width, the fin height, the gate dielectric material, and the gate length on the device performance are analyzed and investigated for the SOI FinFET structure under study. The investigated tri-gate FinFET device has a 3D channel as illustrated in Figure 1. The model was calibrated with an agreement to IBM's model (see Figure 2). The electrical characteristics of the FinFET device are evaluated at a room temperature of 300 K.

4.1. Effects of the Fin Width/Height on Device Performance

In this study, it is important to start by investigating the effect of different fin size ratios on device characteristics. To analyze the impact of the fin width on the device performance, the fin width of the studied structure was varied from 4 nm to 20 nm with the fin height kept fixed at 26 nm. It should be underlined that, although a larger fin width allows enlarging the total gate width (see Equation (1)), when the gate length shrinks, the W_{fin} width has to shrink as well in order to maintain an efficient suppression of the SCEs [19]. Figure 4 reports the effect of changing the fin width on the transfer I–V characteristics and the corresponding transconductance (Triangle symbols) for the investigated device. As can be clearly observed, the increase in the fin width leads to a reduction of the threshold voltage, in agreement with what is expected from previous studies [18]. In addition, owing to the increase of the total gate width (see Equation (1)), a larger fin width implies an increase in the drain current and transconductance [9,18]. Figure 5 shows the total gate capacitance versus V_{gs} for the studied device with different values of the fin width. As can be seen, as V_{gs} increases, C_{gg} increases until its value becomes roughly constant [4]. The value of C_{gg} decreases by decreasing the fin width, due to the reduction of the total gate width. Figure 6 shows f_T variation as a function of V_{gs} for the studied device with different values of the fin width. The peak in f_T increases as W_{fin} reduces. The behavior of f_T is mainly due to the impact of the fin width on C_{gg} rather than on g_m, as can be observed from Figures 4–6. The peak point of f_T is 3.9 THz at V_{gs} = 0.21 V with a V_{ds} = 0.05 V for a device with a fin width of 4 nm.

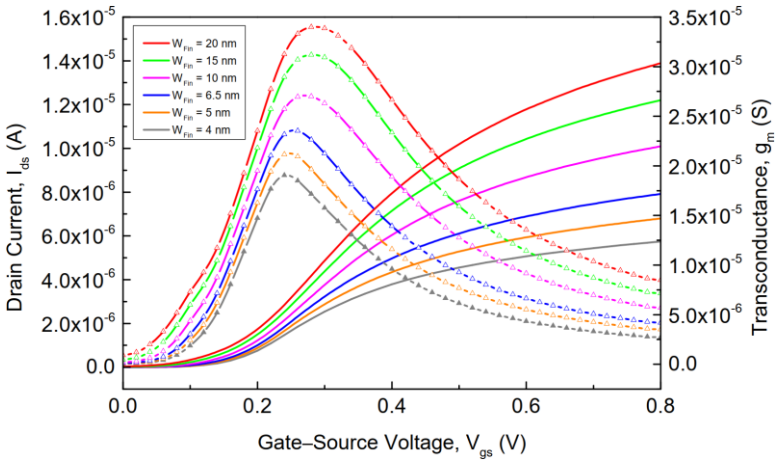

Figure 4. Behavior of the drain current (left axis) and transconductance (Triangle symbols, right axis) versus the gate–source voltage with different values of the fin width at V_{ds} = 0.05 V. The fin height is kept fixed at 26 nm.

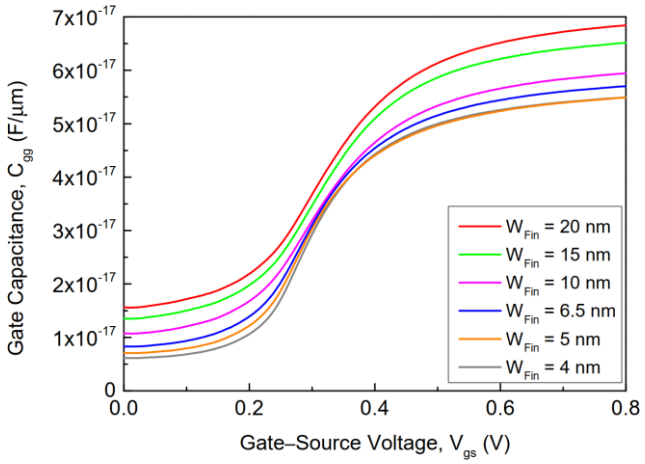

Figure 5. Gate capacitance as a function of gate–source voltage with different values of the fin width at V_{ds} = 0.05 V. The fin height is kept fixed at 26 nm.

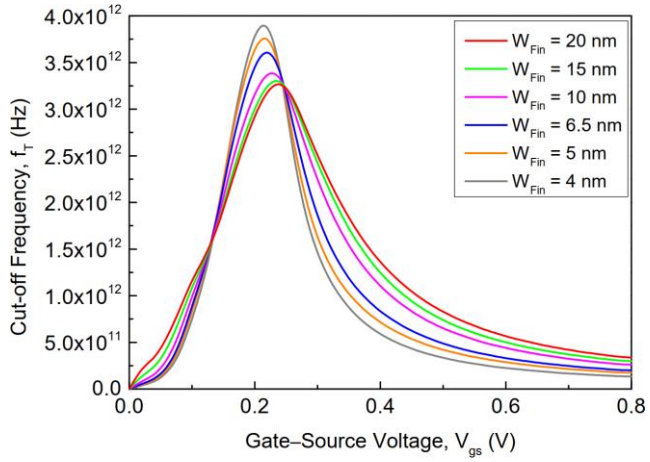

Figure 6. Cut-off frequency as a function of gate–source voltage with different values of the fin width at V_{ds} = 0.05 V. The fin height is kept fixed at 26 nm.

The variations of the threshold voltage, subthreshold slope, on-current, and off-current with different values of the fin height (H_{fin} = 10, 15, 20, 25, 30, and 35 nm) and of the fin width (W_{fin} = 4, 6.5, 15, and 20 nm) are shown in Figures 7–10, respectively. Figure 7 shows a reduction in the threshold voltage with increasing H_{fin} and/or W_{fin}. Figure 8 shows the impact of H_{fin} on the subthreshold slope for FinFET devices with different values of W_{fin} at V_{ds} = 0.05 V. This figure shows a slight impact of changing H_{fin} on *SS* when considering the lower values of the fin width (i.e., 6.5 nm and 4 nm), whereas a marked increase in *SS* is observed with increasing H_{fin} and/or W_{fin} when considering higher values of the fin width. It was observed that, for the studied FinFETs, a smaller fin width leads to better device performance in terms of *SS*. This confirms that studying the impact of varying fin width and fin height is essential for enabling technology development, since they can have a strong impact on the short channel effects. As expected, the increase in the gate width by increasing H_{fin} and/or W_{fin} leads to an increase in both on-state current and off-state current, as reported in Figures 9 and 10. Figure 9 shows the impact of H_{fin} on the switching current (I_{on}) for FinFET devices with different W_{fin} at V_{gs} = V_{ds} = 0.8 V. It is achieved a rapid increase in I_{on} as W_{fin} and/or H_{fin} increase. Figure 10 shows the impact of H_{fin} on the leakage current (I_{off}) for FinFET devices with different W_{fin} at V_{gs} = 0 V and V_{ds} = 0.8 V. It is achieved a clear decrease in I_{off} as W_{fin} and/or H_{fin} decrease. In particular, Figure 10 shows a slighter impact of changing H_{fin} on I_{off} when considering the lower values of the fin width (i.e., 6.5 nm and 4 nm), whereas a more marked decrease in I_{off} is observed with decreasing H_{fin} and/or W_{fin} when considering higher values of the fin width. The electrostatic can be improved effectively with shorter fin width, which can report better mitigation of the leakage current for the nanoscale devices. This could be a good design strategy to enhance device performance, but it will be quite difficult to fabricate the pattern on the device with a very high aspect ratio (H_{fin}/W_{fin}). For a given variation in the fin height, the corresponding change in the device performance of the investigated FinFET model can be linked to what was reported and discussed in detail in Kurniawan's work [20].

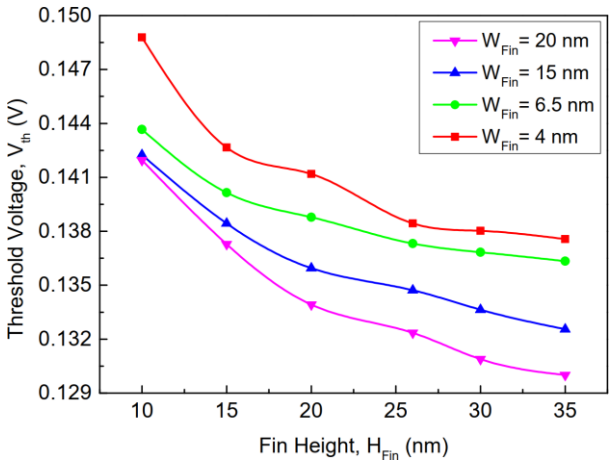

Figure 7. Behavior of the threshold voltage as a function of fin height for FinFET devices with different values of the fin width at V_{ds} = 0.05 V.

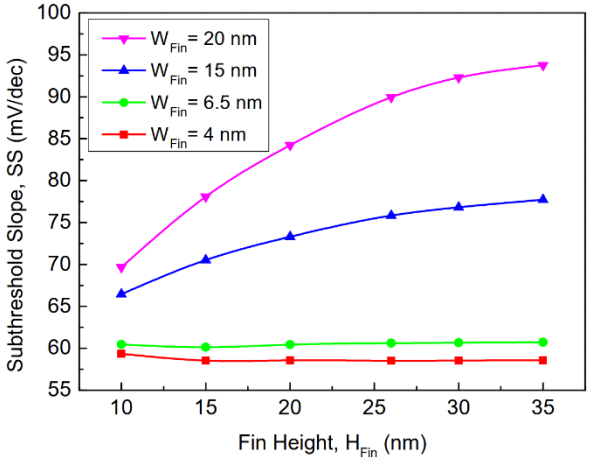

Figure 8. Behavior of the subthreshold slope as a function of fin height for FinFET devices with different values of the fin width at V_{ds} = 0.05 V.

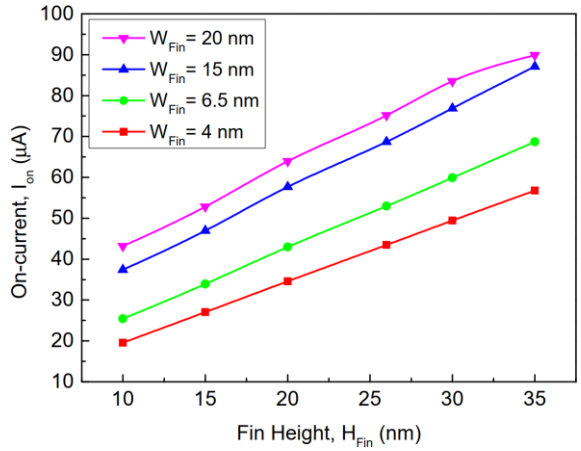

Figure 9. Behavior of the on-current as a function of fin height for FinFET devices with different values of the fin width at V_{gs} = V_{ds} = 0.8 V.

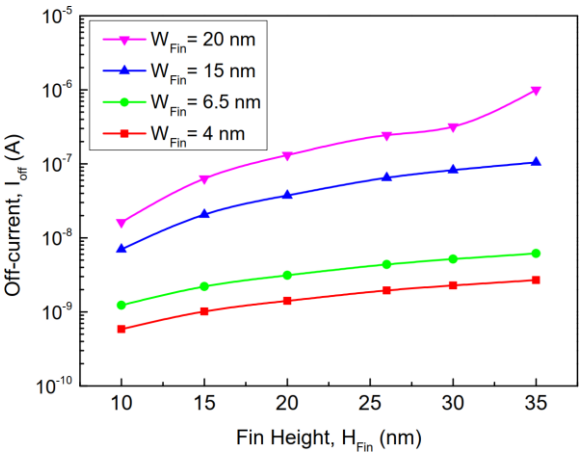

Figure 10. Behavior of the leakage current as a function of fin height for FinFET devices with different values of the fin width at V_{gs} = 0 V and V_{ds} = 0.8 V.

As is well-known, a higher I_{on} is well desired while the leakage current I_{off} should be kept low in order to minimize the static power consumption. Figure 11 shows the effect

of varying the fin height and the fin width on the I_{on}/I_{off} ratio, which is a crucial figure of merit for digital applications. As shown in Figure 11, the I_{on}/I_{off} ratio decreases with increasing H_{fin} and/or W_{fin}. It should be noticed that the highest value of the I_{on}/I_{off} ratio occurs at the lowest height of 10 nm and then decreases approximately exponentially with increasing H_{fin}.

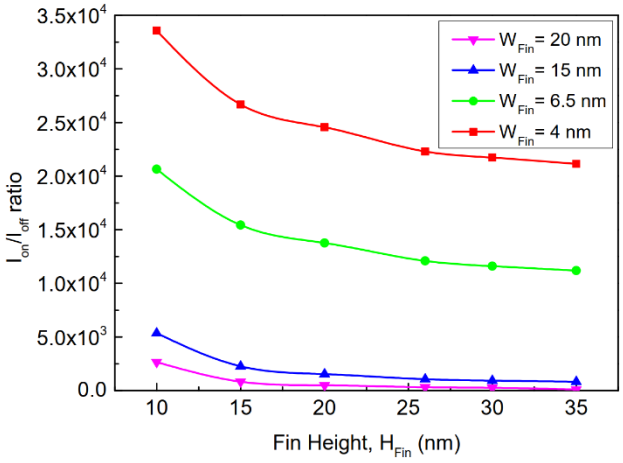

Figure 11. Behavior of the current ratio I_{on}/I_{off} as a function of fin height for FinFET devices with different values of the fin width at V_{ds} = 0.8 V.

4.2. Impact of High-k Dielectric Materials on Device Performance

To analyze the effect of the gate dielectric materials on the device performance, the fin width, fin height, and gate length of the studied structure were fixed at 6.5, 26, and 20 nm, respectively. Figure 12 shows the total gate capacitance versus V_{gs} for different high-k dielectric materials. Under all of the studied cases, C_{gg} starts increasing as V_{gs} increases until saturation, and then it becomes roughly constant, as expected [4]. The value of C_{gg} increases with high-k dielectric material.

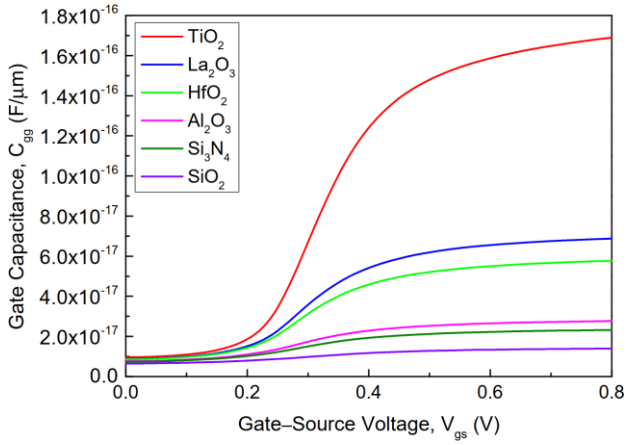

Figure 12. Gate capacitance as a function of gate–source voltage with different gate dielectric materials at V_{ds} = 0.05 V.

The change in transconductance and cut-off frequency with different gate dielectric materials is shown in Figure 13. The analyzed bias point is: V_{gs} = 0.2 V and V_{ds} = 0.05 V. As can be observed from the figure, a remarkable improvement of the device performance is achieved using higher-k material [4,21]. The value of g_m for TiO_2 material is higher compared to the values obtained by using the other dielectric materials, implying a higher amplification capability of the device [4,22]. The resultant behavior of f_T is mainly due to

the impact of the high-k dielectric material on g_m rather than on C_{gg}, as can be noticed from Figures 12 and 13. The highest f_T is obtained at V_{gs} = 0.2 V with V_{ds} = 0.05 V for a FinFET model with TiO_2 material, reflecting the better gate controllability over the channel fin region and hence higher transconductance.

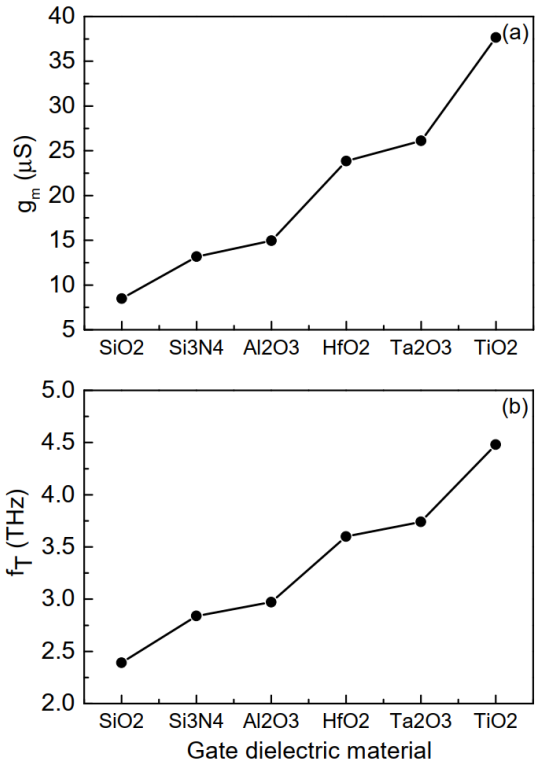

Figure 13. Behavior of (**a**) transconductance and (**b**) cut-off frequency with different high-k gate dielectric materials at V_{ds} = 0.05 V.

In short channel devices, the leakage current can be problematic for switching speed in the circuit by leading to an increase in the I_{on}/I_{off} ratio. The use of a multigate design structure together with high-k dielectric materials proves good mitigation in device issues and demonstrates high switching speed in electric circuits [16–22]. Figure 14 shows the transfer I–V characteristics in a logarithmic scale of 14-nm SOI n-FinFET under on-state bias conditions (V_{ds} = 0.8 V). It is observed that the off-state current decreases, especially with high-k. As expected, using high-k dielectric such as TiO_2 is necessary for short channel devices to mitigate the leakage current. It is also observed that the current flow in the short channel can be improved by using high-k dielectric material. As reported in Figure 15, the highest value of I_{on}/I_{off} occurs at the highest dielectric constant. For many electronic circuit applications, such as amplifiers and digital circuits, the best I_{on}/I_{off} current ratio is at the highest value and therefore it implies better device performance.

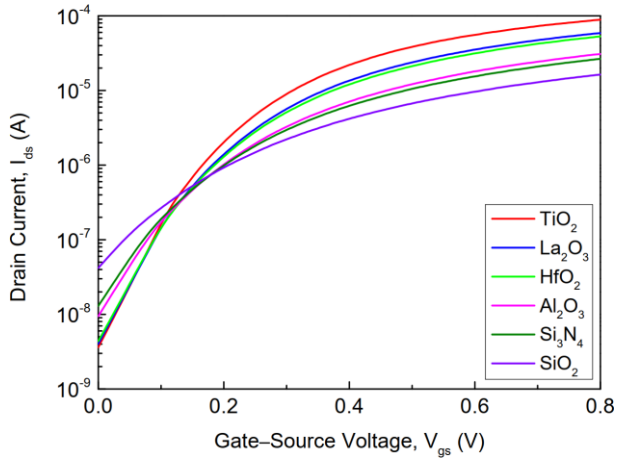

Figure 14. Transfer I–V characteristics in logarithmic scale for FinFET devices with different gate dielectric materials at V_{ds} = 0.8 V.

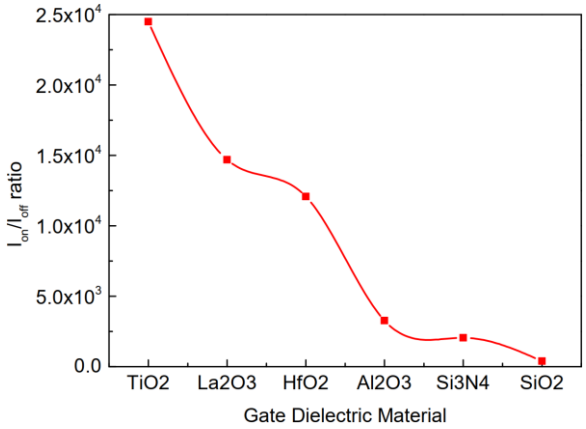

Figure 15. Behavior of the current ratio I_{on}/I_{off} as a function of gate dielectric materials for FinFET devices at V_{ds} = 0.8 V.

4.3. Impact of the Gate Length on Device Performance

To analyze the effect of the gate length on the device performance, the fin width and fin height of the studied structure were fixed at 6.5 nm and 26 nm, respectively. Furthermore, the hafnium oxide was used as a gate dielectric material. There are full-node processes for FinFET technologies, such as 16, 14, 10, 7, 5, and 3 nm in R&D [1,2]. Thus, is very important to investigate the effect of the gate length on calibrated FinFET device performance. Varying device gate lengths can help in judging the numerical model's accuracy in predicting the device characteristics. The change in transconductance with different gate lengths (from 5 nm to 20 nm) is shown in Figure 16. It can be observed from the figure that a remarkable limitation is achieved by scaling down the gate length. The g_m for 10 nm gate length device reaches higher values compared to other devices with different gate lengths [4,18]. The f_T behavior is mainly due to the gate length effect on g_m rather than on C_{gg}, as can be noticed from Figures 16–18. The highest f_T is obtained at V_{gs} = 0.25 V with V_{ds} = 0.05 V for a device with 5 nm gate length, as illustrated in Figure 18. To find the effect of the gate length on the device's I–V characteristics, the gate length was varying from 5 nm to 20 nm. Figure 19 illustrates the effects of the gate length on transfer I–V curves of the device. It is well seen from the figure that reducing the gate length leads to a decrease in the threshold voltage, but it causes an increase in the leakage current (at V_{gs} = 0 V). The variation of the threshold voltage, subthreshold slope, and I_{on}/I_{off} ratio at two gate lengths with different fin widths is shown in Figures 20–22, respectively. As can be observed, V_{th} and SS are sensitive to W_{fin} for a small gate length due to the short channel effect as illustrated in Figures 20 and 21,

respectively [22–27]. As shown in Figure 22, the highest value of I_{on}/I_{off} occurs at the lowest fin width.

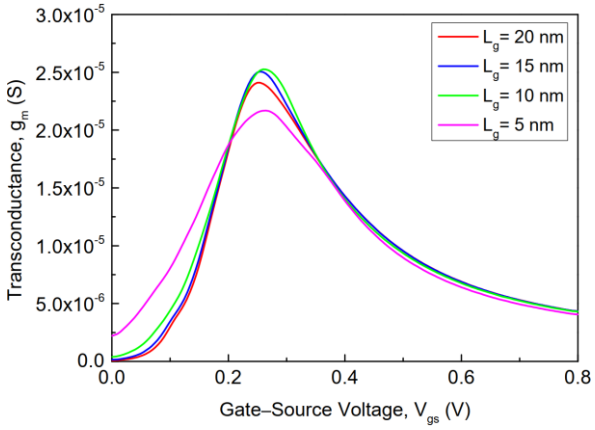

Figure 16. Transconductance as a function of gate–source voltage with different gate lengths at V_{ds} = 0.05 V.

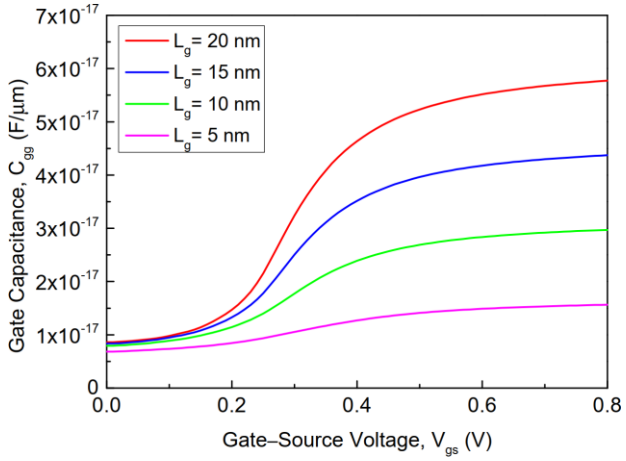

Figure 17. Gate capacitance as a function of gate–source voltage with different gate lengths at V_{ds} = 0.05 V.

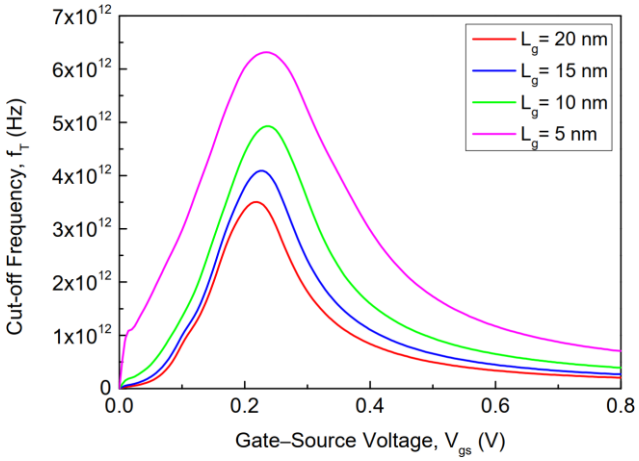

Figure 18. Cut-off frequency as a function of gate–source voltage with different gate lengths at V_{ds} = 0.05 V.

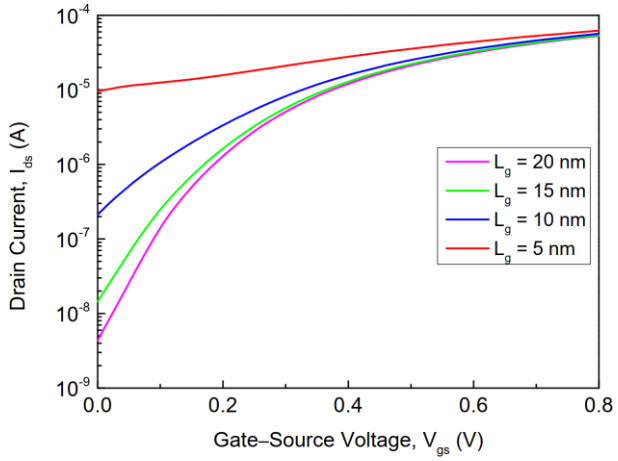

Figure 19. Transfer characteristics logarithmic scale for FinFET devices with different gate lengths at V_{ds} = 0.8 V.

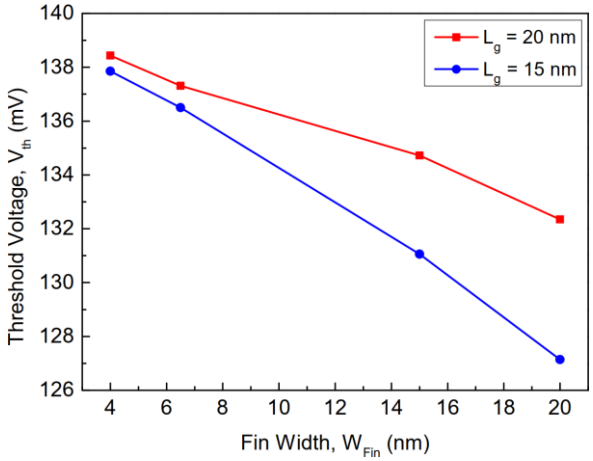

Figure 20. Behavior of the threshold voltage as a function of fin width for FinFET devices with two different gate lengths at V_{ds} = 0.05 V.

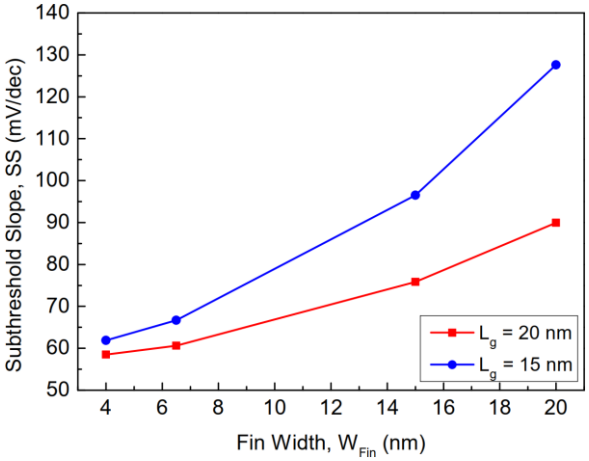

Figure 21. Behavior of the subthreshold slope as a function of fin width for FinFET devices with two different gate lengths at V_{ds} = 0.05 V.

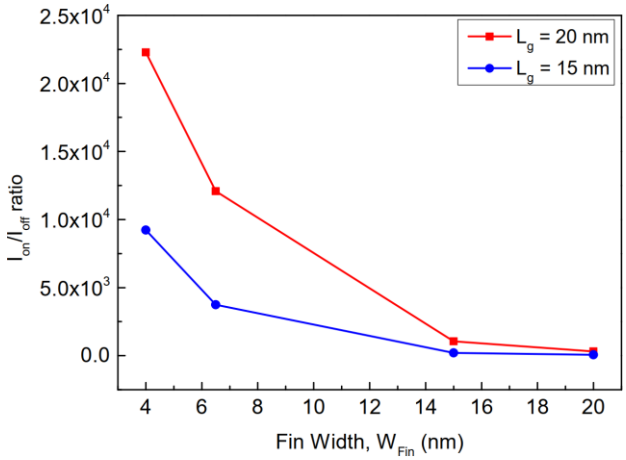

Figure 22. Behavior of I_{on}/I_{off} ratio as a function of fin width for FinFET devices with two different gate lengths at V_{ds} = 0.8 V.

4.4. Device Optimization

Silicon material is used for the fabrication of an optimized FinFET device with a physical gate length of 15 nm. TiO_2 is used as gate dielectric material to replace HfO_2 for better controllability of the gate over the channel. As it is well-known, the electrostatic integrity can be improved by reducing the thickness of the gate oxide [26]. The high-k dielectric thickness is chosen to be 2 nm. Based on the previous investigation, the fin width and fin height are chosen to be equal to 4 nm and 35 nm, respectively. Fin width was scaled down in order to improve FinFET electrostatics. The source/drain spacers are fixed to 7 nm and covered by Si_3N_4. The contact resistivity at the S/D contact/silicon interface is fixed to 10^{-9} Ω.cm^2. The proposed device with the above characteristics shows a good improvement in electrical parameters such as I_{on}, *SS*, and *DIBL* compared to calibrated FinFET [1]. This proves that the improvement of SCEs in the FinFET device reduces sensitivity to the leakage current. It is also interesting to note that I_{on}/I_{off} ratio is approximatively two times greater than the calibrated FinFET. Better device switching (on/off) can result from steeping *SS* and a larger I_{on}/I_{off} ratio. Table 3 illustrates a comparison of the optimized and calibrated device parameters with different 14-nm FinFET device technologies [28–30].

Table 3. Comparison of different 14-nm SOI n-FinFET device technologies.

Device Characteristics	Calibrated Device	Optimized Device	FinFET [28]	FinFET (IRDS 2020) [29]	FinFET [30]
V_{dd} (mV)	800	800	-	-	-
$V_{th,\,lin}$ (mV)	137.31	143.6	-	-	-
$V_{th,\,sat}$ (mV)	120	110.5	-	240	233.55
$I_{on,\,lin}$ (μA)	8.11	17.49	-	-	-
$I_{on,\,sat}$ (μA)	53.6	148.93	-	68.62	10.9 (/μA)
$I_{off,\,lin}$ (nA)	1.89	1.89	-	-	-
$I_{off,\,sat}$ (nA)	4.22	5.35	-	1.76	80.6 (/μA)
$I_{on,\,lin}/I_{off,\,lin}$	4.29×10^3	9.24×10^3	-	-	-
$I_{on,\,sat}/I_{off,\,sat}$	1.27×10^4	2.77×10^4	-	38.933	135.236
SS_{lin} (mV/dec)	60.60	58.80	80	-	-
SS_{sat} (mV/dec)	64.91	58.22	-	72	76.98
DIBL (mV/V)	43.32	22.65	75	50	68.57

Finally, it should be highlighted that nowadays the interest for the FinFET technology is spreading more and more in many fields of application—such as single-molecule detection [31], pH sensing [32,33], biomedicine [34], label-free biosensing [35], 5G power

amplifiers [36], energy harvesting [37], and space application [38], just to mention a few. This wide and ever-expanding range of applications makes evident the increasing need for an accurate optimization of the FinFET structure to satisfy the specific constraints and requirements.

5. Conclusions

In this study, the 3D 14-nm SOI n-FinFET was successfully simulated, performed, and calibrated to experimental data by using Silvaco tools. The effects of varying the fin width, fin height, gate dielectric material, and gate length on device performance were analyzed in terms of both DC and RF parameters. The results indicated that low leakage current and high I_{on}/I_{off} ratio can be obtained with small W_{fin} and H_{fin}. A cut-off frequency on the order of 1 THz was simulated and reported for the investigated FinFET model. The results indicated that this frequency is increased for smaller fin width and a subsequent reduction of gate transconductance. For the optimized device, a transconductance of 69.33 μS and a cut-off frequency of 4.22 THz were achieved at V_{ds} = 0.05 V with V_{gs} = 0.23 V and V_{gs} = 0.22 V, respectively, by using the TiO_2 as the gate dielectric at 15-nm gate length. The developed study provided some useful insights outlining the great potential of the FinFET technology nodes for RF applications with high performance and low power consumption.

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