Article

A Dual Source Switched-Capacitor Multilevel Inverter with Reduced Device Count

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Abstract: Implementing voltage boost multilevel inverter topologies for PV and fuel cell energy sources is highly advantageous. Switched-capacitor multilevel inverters (SCMLI) have a step-up feature with low device requirements and can remove the need for high gain dc-dc converters leading to reduced overall system bulk. This work proposes a dual input SCMLI to achieve an output of nineteen levels while using a low number of components and high boosting factor and self-balancing of capacitor voltages. A comprehensive analysis of the proposed structure is presented, focusing on component requirements, cost and dynamic performance. The efficiency and loss distribution during operation is also provided. The operation and real-time performance of the SCMLI have been verified by simulation. Experimental results further validate the simulation results.

Keywords: multilevel inverter; solar PV; switched-capacitor; experimental validation

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1. Introduction

As the installation of renewable energy systems is gaining traction across the globe, the significance of multilevel inverters (MLIs) as dc-ac conversion devices is at its zenith [1,2]. Since many renewable power sources are composed of numerous low-voltage dc sources such as solar photovoltaic cells, ultra-capacitors, or battery storage systems, they are ideal for forming multiple connected dc-links. A similar case can be observed in hydrogen-based fuel cells investigated for use in high specific energy applications like onboard power systems [3]. MLIs can generate high efficiency and power quality dc-ac conversion at high voltage and high power levels. The reduced harmonic content, reduced individual device ratings and the filter size are some of the attributes of MLIs. Traditionally, MLIs were devised as cascaded H-bridge, flying capacitor and neutral point clamped configurations. Flying capacitor and neutral point clamped topologies have substantial capacitor counts with higher levels, leading to cost and reliability issues and capacitor voltage balancing requirements [4]. Since their inception, numerous evolved configurations have been developed to eliminate their setbacks. Furthermore, the later developed topologies outperform the three traditional topologies in component counts. Currently, researchers are developing MLIs with an application-based approach with fault-tolerance, modularity, efficiency and even weight and volume requirements in mind [5–7].

Extensive efforts have been made in the design of reduced device count structures [8–10]. On a similar note, fault-tolerant reduced device count topologies [10,11] and device count optimization [12] have also been investigated by researchers. Nevertheless, the need for a high number of dc sources leads to practical realization and control complexity issues,

especially with renewable power sources with fluctuating voltage magnitudes. Initially, the inclusion of capacitors in MLIs can be observed in the two classical configurations, NPC and FC themselves. Recently, SCMLI-based topologies, including combinations of capacitors and switch modules in series/parallel configuration, have gained researchers' attention, particularly for applications where a voltage boosting feature is advantageous [13–17]. Low magnitude voltage, including PV or fuel cell, can be significantly increased as a result of this boosting feature. This warrants the exclusion of boost dc/dc converters, which would otherwise be required as intermediate devices [18], thus significantly reducing the overall generation system size, efficiency, and complexity. Nevertheless, the challenges of the inflated device count with higher levels are currently being addressed.

Interestingly, the replacement of multiple dc sources of a CHB with capacitors is investigated in [19], thus requiring a single dc source. The structure proposed in [20] can generate a total of nine levels using two capacitors, one dc source and nine switches with a two-fold boosting factor. The self-balancing of capacitor voltages has the benefit of eliminating the need for additional instrumentation or control circuitry. Similarly, a topology using three interconnected H-bridge structures, one dc source and two capacitors can produce seven levels with a boosting factor of three [21]. The fault-tolerant operation of an SCMLI topology is also investigated in [22]. Feedback linearization control for voltage and current ripple reduction under dynamic and steady operating conditions includes ANN (artificial neural network) in [23].

Furthermore, to reduce the switch current ratings and enable a larger power capability, the usage of multiple dc sources that can split the overall load current among multiple conduction paths is suitable. A 55-level topology with three asymmetrical dc sources and seven capacitors is proposed in [24], but the large number of components involved can negatively affect its reliability. Seven-level modified PUC active rectifier based on floating weighting factors and ANN-MPC based on Lyapunov stability were presented in [24]. A topology using two asymmetrical dc sources, four capacitors and ten switches is presented in [16] with a specific method for capacitor charge balancing. More examples of multiple dc source topologies with reduced device count and self-balancing capabilities can be observed as in [25–41].

A new SCMLI topology has been proposed. The SCMLI is able to produce higher levels with a low device count. In Section 2, the SCMLI operation has been discussed. Comparative assessment of the topology is carried out in Section 3. The performance of the topology is verified in Section 4. The structure's power loss analysis is carried out in Section 5. The conclusion of this work is presented in Section 6.

2. Proposed Topology

The schematic of the proposed topology is shown in Figure 1. The structure consists of two dc voltage sources, one power diode and ten switches, with two switches being bidirectional modules. The two dc sources possess per-unit values of $0.5V_{dc}$ and $2V_{dc}$ (a ratio of 4:1). The two capacitors, C_1 and C_2 , create the boosting effect in their operation. They are charged in series with the $2V_{dc}$ source. The proposed topology can generate a total of 19 levels. The switching states are shown in Table 1. The ratio of the capacitors is $C_1/C_2 = 0.5$. The ratio between the total source voltage and peak output level, known as the boosting factor, is $4.5/2.5 = 1.8$. The capacitor voltages are self-balanced through charging loops on certain levels. Figure 2 illustrates the various conduction paths in operation. The peak blocking voltages across various switches are as follows.

$$V_{ST1} = V_{ST1'} = 0.5V_{dc} \quad (1)$$

$$V_{ST2} = V_{ST2'} = 4.5V_{dc} \quad (2)$$

$$V_{Su} = V_{Su'} = 2V_{dc} \quad (3)$$

$$V_{Sb1} = V_{dc} \quad (4)$$

$$V_{Sb2} = 3V_{dc} \quad (5)$$

$$V_{ST3} = V_{ST3'} = 4V_{dc} \quad (6)$$

Figure 1. Structure of proposed multilevel inverter topology.

Table 1. Switching states.

T_1	T_1'	T_2	T_2'	S_u	S_{b1}	$S_{u'}$	S_{b2}	T_3	T_3'	V_o	C_1	C_2
0	1	0	1	0	0	1	0	0	1	zero	C	C
1	0	0	1	0	0	1	0	0	1	$0.5 V_{dc}$	C	C
0	1	0	1	0	0	1	1	0	0	V_{dc}	C	C
1	0	0	1	0	0	1	1	0	0	$1.5 V_{dc}$	C	C
0	1	0	1	0	0	1	0	1	0	$2 V_{dc}$	C	C
1	0	0	1	0	0	1	0	1	0	$2.5 V_{dc}$	C	C
0	1	0	1	0	1	0	0	1	0	$3 V_{dc}$	-	D
1	0	0	1	0	1	0	0	1	0	$3.5 V_{dc}$	-	D
0	1	0	1	1	0	0	0	1	0	$4 V_{dc}$	D	D
1	0	0	1	1	0	0	0	1	0	$4.5 V_{dc}$	D	D
1	0	1	0	0	0	1	0	1	0	zero	C	C
0	1	1	0	0	0	1	0	1	0	$-0.5 V_{dc}$	C	C
1	0	1	0	0	0	1	1	0	0	$-V_{dc}$	C	C
0	1	1	0	0	0	1	1	0	0	$-1.5 V_{dc}$	C	C
1	0	1	0	0	0	1	0	0	1	$-2 V_{dc}$	C	C
0	1	1	0	0	0	1	0	0	1	$-2.5 V_{dc}$	C	C
1	0	1	0	1	0	0	1	0	0	$-3 V_{dc}$	D	-
0	1	1	0	1	0	0	1	0	0	$-3.5 V_{dc}$	D	-
1	0	1	0	1	0	0	0	0	1	$-4 V_{dc}$	D	D
0	1	1	0	1	0	0	0	0	1	$-4.5 V_{dc}$	D	D

Figure 2. All positive conduction states.

The TSV (total standing voltage) is computed as the summation of these voltages. The bidirectional switches require two modules with the same rating.

$$\text{TSV} = \sum_{n=1}^{10} V_{sn} = 30V_{dc} \quad (7)$$

The per-unit TSV of the structure is given as:

$$\text{TSV}_{\text{p.u.}} = \frac{\text{TSV}}{V_{o,\text{peak}}} = \frac{30V_{dc}}{4.5V_{dc}} = 6.66 \quad (8)$$

The modulation scheme is either low frequency-based (LS-PWM) or high-frequency carrier-based (CB-PWM). Modulation at low frequencies possesses the advantage of reduced switching losses, dv/dt ratings and snubber losses. Low frequency-based modulation techniques comprise the nearest level control (NLC) and the selective harmonic elimination (SHE) methods. The SHE approach is optimum for reducing the filter size but involves the solution of complex non-linear transcendental equations, therefore, being computationally more intensive. Additionally, NLC is more convenient for closed-loop

controlled systems. NLC-PWM has been used in this work. The visual representation of NLC-PWM is depicted in Figure 3. The modulation index M_a is given as:

$$\theta_i = M_a \sin^{-1} \left(\frac{2i-1}{N-1} \right) \quad (9)$$

Figure 3. Nearest level modulation.

Knowing the modulation index M_a , number of levels N and switch index i , the calculation for switching angle θ_i [36,37] is given as:

$$M_a = \frac{V_{ref}}{V_0} \quad (10)$$

3. Comparative Assessment

The proposed SCMLI is compared with recently devised works with a similar level count. The basis for comparisons includes the quantity of power semiconductor switches, diodes, capacitors, gate drivers, boosting factor and cost function. The comparison is shown in Table 2. The proposed SCMLI is superior in terms of component count per unit level, particularly considering levels produced as compared to previous works. Additionally, the comparison is also made using the metric of the cost function (CF) as defined in [38]. An intelligent compact multilevel converter based on passivity ANFIS control was presented in [31].

$$CF = (N_{sw} + N_{gd} + N_d + N_c + \alpha \times TSV_{pu}) N_{dc} \quad (11)$$

$$NCF = \frac{CF}{N_L} \quad (12)$$

Table 2. Comparative Assessment.

Topology	N_L	N_{dc}	N_{sw}	N_{gd}	N_d	N_c	TSV_{pu}	VG	CF
[24]	11	2	11	11	0	1	4.4	1.67	4.66
[26]	13	2	14	11	0	2	5.33	2	4.56
[27]	17	2	10	10	2	2	5.5	2	3.14
[28]	17	2	10	10	2	2	5.5	2	3.14
[29]	13	2	11	10	1	1	6.3	1.5	4.18
[30]	13	2	18	15	0	2	5	2	5.76
[31]	17	2	18	14	2	4	6	2	4.82
[32]	19	2	12	12	6	4	5.8	2.25	3.85
Proposed	19	2	12	10	1	2	6.66	1.8	3.02

From Table 2, it is seen that the proposed SCMLI has the lowest NCF for two values of α . This verifies that the proposed converter has a high number of levels with lower component requirements and a cost-effective design.

4. Power Loss Analysis

The proposed converter's thermal loss model was developed to estimate the topology's loss distribution across various components and efficiencies. The non-ideality in semiconductor components leads to conduction (P_C) and switching losses (P_S). In other words, power dissipation across ON-state resistance leads to conduction losses, and non-instantaneous transitions between ON and OFF states lead to switching losses. The total conduction loss in IGBTs and diodes is obtained using:

$$P_{c_{sw}} = V_{sw}i(t) + R_s i^{\beta}(t) \quad (13)$$

$$P_{c_D} = V_D i(t) + R_D i^2(t), \quad (14)$$

$$P_c = \sum_{k=1}^{N_{sw}} \frac{1}{2\pi} \int_0^{2\pi} (V_{sw}i(t) + R_s i^{\beta}(t)) dt + \sum_{k=1}^{N_D} \frac{1}{2\pi} \int_0^{2\pi} (V_D i(t) + R_D i^2(t)) dt \quad (15)$$

where V_{sw} is the ON-state voltage drop across the switch and V_D is the ON-state drop across the power diode. R_s is the ON-state resistance of the switch, and R_D stands for the ON-state resistance of the diode. Following an assumption of non-linear transitions between device current and voltages, the switching loss is for N_s switches, and with f switching frequency is evaluated as:

$$P_s = \left[\sum_{k=1}^{N_s} (N_{ON_k} E_{ON_k} + N_{OFF_k} E_{OFF_k}) \right] \times f, \quad (16)$$

with N_{ON_k} , N_{OFF_k} , E_{ON_k} , and E_{OFF_k} being associated with switch number (k), are the number of transitions and energy losses in turning ON and OFF, respectively. The total thermal is:

$$P_{loss} = P_c + P_s \quad (17)$$

Conversion efficiency is given by:

$$\eta = \frac{P_0}{P_0 + P_{loss}} \times 100\% \quad (18)$$

The PLECS platform was utilized for the thermal analysis of the SCMLI. The module IGW40N60H3, PG6DI capacitor is implemented with a peak voltage of 450 V. Figure 4 shows the conversion efficiency as compared to two previous topologies. The corresponding distribution of losses for loads is shown in Figure 5. As evident, the conduction losses are dominant due to low-frequency NLC PWM.

Figure 4. Efficiency curve.

Figure 5. Loss distribution across switches (a) Switching Loss (b) Conduction Loss.

5. Results and Discussion

5.1. Simulation Results

The proposed SCMLI topology is simulated in MATLAB and PLECS environments. NLCPWM staircase modulation was used for generating a 19-level output with a 450 V peak at MI = 1.0 and 50 Hz frequency. The topology's dynamic performance with load change was verified, and the load voltage, current and capacitor voltage waveforms are illustrated in Figure 6a. The load was changed from 50Ω to $50 \Omega + 40 \text{ mH}$ at $t = 0.04 \text{ s}$. Similarly, the output of the inverter with a varying modulation index of MI = 0.8, 0.9 and 1 can be observed in Figure 6b. Notably, the balance in capacitor voltages is maintained irrespective of alteration in load or MI. Furthermore, the voltage and current stresses of the switches with a load of $50 \Omega + 40 \text{ mH}$ are given in Figure 7a,b.

Figure 6. (a) Simulation results with load change (b) Simulation results with modulation index change.

Figure 7. Switch stresses during simulation (a) Voltage Stress (b) Current Stress.

5.2. Experimental Verification

The laboratory prototype of the SCMLI topology is shown in Figure 8. The IGBT (IGW40N60H3) and PG6DI capacitors were used. TMS320F28335 DSP and TLP250H gate drivers were used for gating pulse control. A Yokogawa DL1640 oscilloscope was used to capture the resulting waveforms. A peak voltage of 63V at MI = 1 was created. Figure 9 depicts the 19-level load voltage waveform and current through a 210 Ω load. The voltage and current waveforms are in phase with similar wave shapes. The peak voltage and current values are 63 V and 0.3, respectively. Observably, the current lags the output voltage due to the inductive phase lag and is approaching a closer sinusoidal shape. To demonstrate the performance in dynamic conditions, R-load changes are also analyzed. The R-load changed from 210 Ω to 105 Ω , as shown in Figure 10. Additionally, waveforms during no-load to R-load transition are given in Figure 11. The harmonic profile of the 19-level waveform can be seen in Figure 12. The waveform has a THD of 4.3%, which meets EN50160 power quality standards and can eliminate filter demand due to minimal lower order harmonic content. The above results demonstrate the performance of the topology under varying operational requirements.

Figure 8. Experimental Prototype.

Figure 9. 19-level output waveform.

Figure 10. Load change from 210 Ω to 105 Ω .

Figure 11. Load change from no-load to 210 Ω .

Figure 12. Harmonic spectrum.

6. Conclusions

A multisource step-up multilevel inverter with low component requirements and high power quality has been discussed. The operation of the proposed SCMLI is demonstrated, and the self-balancing property of capacitor voltages is shown. Analysis of previous works in developing various MLIs and switched-capacitor configurations with their advantages and setbacks is presented. A comparison of the proposed SCMLI with recent topologies was conducted. The topology's thermal loss analysis was carried out to show its thermal behavior and efficiency. Simulation results have been presented. Experimental results validate the performance in varied operating conditions (load and MI changes).

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