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# A Novel Switched-Capacitor Inverter with Reduced Capacitance and Balanced Neutral-Point Voltage

Zhuyu Xun , Hongfa Ding \* and Zhou He

Wuhan National High Magnetic Field Center, School of Electrical and Electronic Engineering, Huazhong University of Science and Technology, Wuhan 430074, China; xunzhuyu@outlook.com (Z.X.); he\_zhou@hust.edu.cn (Z.H.)

\* Correspondence: dhf@hust.edu.cn

**Abstract:** A novel three-phase switched-capacitor multilevel inverter (SCMLI) with reduced capacitance and balanced neutral-point voltage is proposed in this paper. Applying only one DC source, the three-phase seven-level topology possessing voltage-boosting capability is accomplished without the high-voltage stress of power switches. Owing to the inherent redundant switching states of the proposed topology, two charging approaches that can effectively limit the voltage ripples and path selection for capacitors can be realized. This provides the presented topology with reduced capacitance, balanced neutral-point voltage, good performance in not only the three-phase four-wire system but also the three-phase three-wire system, and low total harmonic distortion (THD) of the output voltage. A comprehensive comparison with previous SCMLIs in various aspects is conducted to validate the merits mentioned above. The simulation results accord with theoretical analyses, confirming the feasibility of the proposed three-phase SCMLI.

**Keywords:** multilevel inverter; switched-capacitor; reduced capacitance; neutral-point voltage imbalance



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## 1. Introduction

Multilevel inverters are important circuit configurations in modern electrical power systems because of their many advantages, such as low total harmonic distortion (THD) of the output voltage, low voltage stress on power devices, and low electromagnetic interference (EMI). The main applications of these inverters include static compensators, high-voltage DC transmission systems, active power filters, and renewable energy systems that include variable-frequency motor drives [1–6]. Neutral-point-clamped (NPC) [7], flying-capacitor [8], and cascaded H-bridge [9] are three well-researched multilevel inverters. These inverters are widely used in practical and commercial applications. However, these inverters have shortcomings such as neutral-point voltage imbalance and the need for excessive isolated DC sources [10]. Owing to the inability to boost the input voltage, the sum of the DC source voltages cannot be less than the amplitude of the output voltage. To overcome the drawbacks mentioned above, many new topologies have been introduced that offer more optimized component utilization, more voltage levels, higher efficiency, and so on [11,12].

Since the input voltage is relatively low compared with the output voltage, boost circuits [13,14] are required in many applications, such as grid-connected photovoltaic modules, distributed generation (DG) systems, and electric vehicles. Inductors or transformers are used in most boost circuits, making the systems bulky and heavy [15]. Therefore, a charge pump is typically adopted as a boost circuit [16]. In the charge pump, the output voltage is equal to the sum of the capacitor voltages and the input voltage. The capacitors in the charge pump are discharged when connected in series and charged when connected in parallel along with the DC source.

Inverters using the same working principle are called switched-capacitor multilevel inverters (SCMLI), which have become a recent research topic of interest [17,18]. Unlike

inductors or transformers, capacitors are used to boost the input voltage. Employing fewer isolated DC sources and related components, they can generate voltage levels. To boost the input voltage, capacitors need to be involved in the load current path. In most SCMLIs, all relevant capacitors are discharged at the top voltage level. In addition, the discharging state can last for a long time according to the modulation method. This time is called the longest discharging time (LDT). As a result, capacitors have difficulty maintaining their voltage, thus exceeding the maximum allowable value of the voltage ripples. This is a critical challenge for existing SCMLIs.

Several methods have been used to solve this problem, but the most adopted method is to increase the capacitance. By employing only one DC source in a three-phase topology, a boost seven-level switched-capacitor inverter was proposed in [19]. The voltage stress of all power switches did not exceed the input voltage, and the capacitance used was 4700  $\mu\text{F}$ . This method increased the volume and cost of the system [20,21]. Another method involves increasing the frequency of the output voltage. A family of SCMLI topologies for high-frequency AC applications was proposed in [22]. This approach can generate more voltage levels with an optimal component count. The main applications of this method have been limited to high-frequency AC systems [23,24]. A third method involves decreasing the maximum allowable modulation index. A novel seven-level inverter for medium-voltage high-power applications was presented in [25], and the maximum allowable modulation index was 0.813. This method reduces the boosting ability of SCMLIs [26]. A fourth method involves reducing the load. A boost single-phase switched-capacitor inverter was presented in [27]. With fewer power switches, this SCMLI could generate nine voltage levels under a resistive load condition (200  $\Omega$ ). However, this method limits the power that SCMLIs can supply when the output voltage is the same [28,29].

Another problem for several SCMLIs that adopt a DC-link converter is the neutral-point voltage imbalance [30–33]. The self-balancing characteristic of these SCMLIs self-regulates the average neutral-point voltage to a certain value (usually half the DC-link voltage). The self-balancing time is long, and the neutral-point voltage may drift excessively. In addition, a three-phase three-wire system can worsen this problem in most traditional three-phase SCMLIs. Additional hardware or software measures are necessary to solve this problem. Regarding software measures, many studies have been carried out based on NPC topology. However, there is little research on this problem in SCMLIs. Hardware measures, such as adding additional components, increase the volume and cost of the system.

Generally, the abovementioned topologies have various disadvantages. To overcome these shortcomings, a novel three-phase SCMLI is presented in this paper. The main advantages of the proposed topology are as follows:

- (1) Less capacitance (200  $\mu\text{F}$ ) is used.
- (2) There is no problem of neutral-point voltage imbalance.
- (3) Good performance is achieved in not only a three-phase four-wire system but also a three-phase three-wire system.
- (4) Only one DC source is used as a three-phase topology.
- (5) All floating capacitors are used to generate the top voltage level.

This paper is organized as follows: the topology of the proposed SCMLI and the operating principle are fully outlined in Section 2. Theoretical analyses of the two charging approaches are provided in Section 3. Control strategies are presented in Section 4. The voltage ripples of the capacitors are carefully analyzed in Section 5. The overall system efficiency is calculated in Section 6. Simulation results and a comprehensive comparison are presented in Section 7. Lastly, a conclusion is drawn in Section 8.

## 2. Proposed SCMLI and Operating Principle

The proposed three-phase SCMLI topology is shown in Figure 1. Employing one DC source and eight capacitors, it can generate seven voltage levels ( $0\text{ V}$ ,  $0.5 V_{\text{dc}}$ ,  $V_{\text{dc}}$ ,  $1.5 V_{\text{dc}}$ ,  $-0.5 V_{\text{dc}}$ ,  $-V_{\text{dc}}$ ,  $-1.5 V_{\text{dc}}$ ) under different kinds of load conditions. The capacitors' rated voltage is  $U_{\text{N}} = 0.5 V_{\text{dc}}$ . Bidirectional switches are used to block positive and negative

voltage stress. The floating capacitors  $C_{1,2}$  are used to generate the top voltage level. They can also balance the voltages of the DC-link capacitors  $C_{dc1,2}$  when needed. Furthermore, the proposed topology is used in a three-phase four-wire system when O and N are connected and is used in a three-phase three-wire system when O and N are not connected.

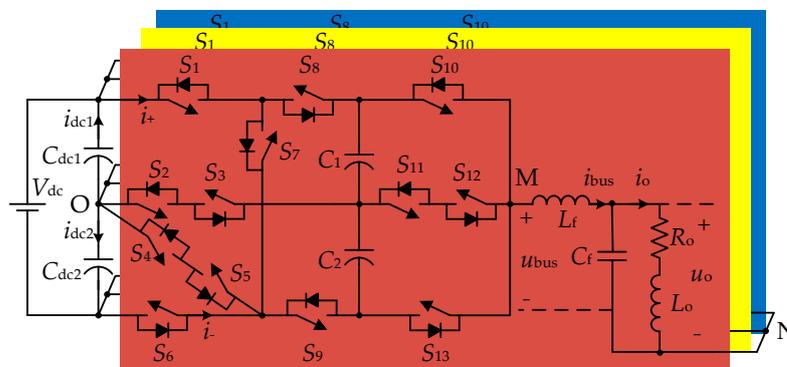
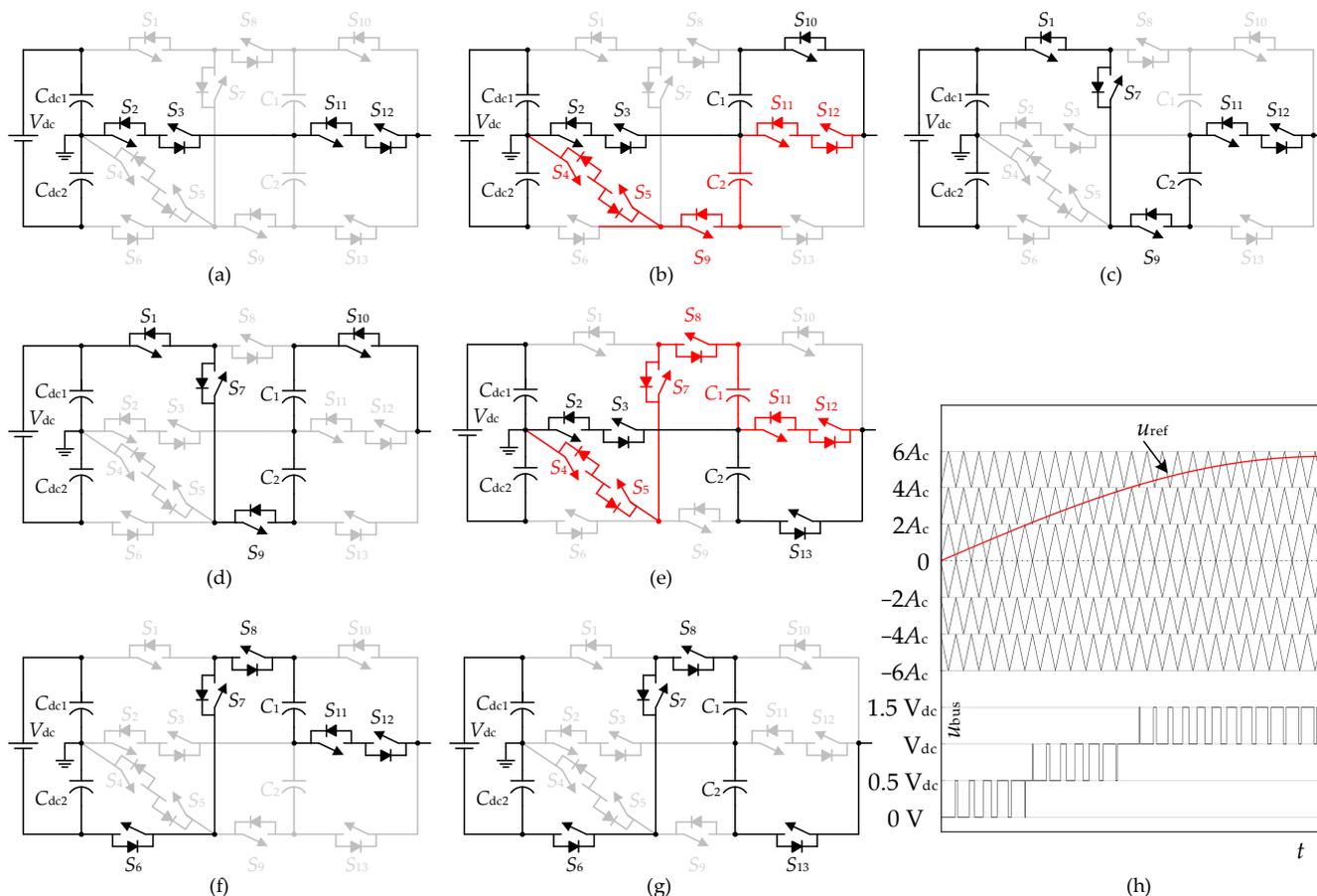


Figure 1. Proposed seven-level three-phase SCMLI topology.

All switching states of the proposed three-phase SCMLI are listed in Table 1. Main switching states are depicted in Figure 2a–g. Other switching states are fully discussed in Sections 3 and 4. To generate 0 V,  $S_2, S_3, S_{11}$ , and  $S_{12}$  need to be ON, as shown in Figure 2a. In Figure 2b,e, the black and red devices represent two different paths. Both  $C_1$  and  $C_2$  can be used to generate not only  $0.5 V_{dc}$  but also  $-0.5 V_{dc}$ . Selecting the right path can make  $u_{C1}$  approach  $u_{C2}$ . In Figure 2c,f, the capacitors  $C_{dc1}, C_2$  and  $C_{dc2}, C_1$  are used to generate  $V_{dc}$  and  $-V_{dc}$ , respectively. To generate  $1.5 V_{dc}$ ,  $S_1, S_7, S_9$ , and  $S_{10}$  need to be ON, as shown in Figure 2d. Similarly, to generate  $-1.5 V_{dc}$ ,  $S_6, S_7, S_8$ , and  $S_{13}$  need to be ON, as shown in Figure 2g. For multilevel inverters, there are several modulation strategies. In this paper, the phase opposition disposition PWM is adopted, which is shown in Figure 2h.

Table 1. All switching states of the proposed three-phase SCMLI.

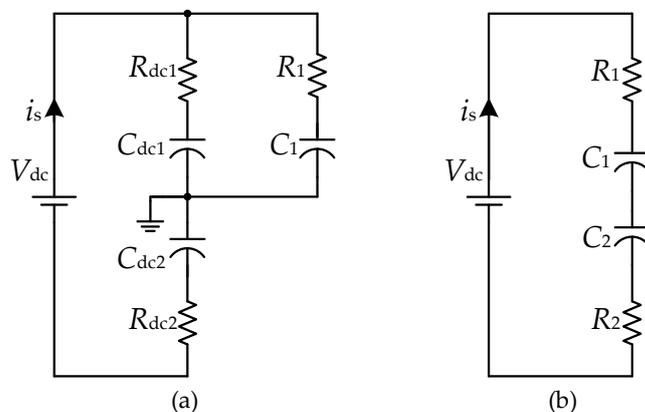
STATES	Voltage	Figure Position	Switches												
	Level		$S_1$	$S_2$	$S_3$	$S_4$	$S_5$	$S_6$	$S_7$	$S_8$	$S_9$	$S_{10}$	$S_{11}$	$S_{12}$	$S_{13}$
1	$1.5 V_{dc}$	Figure 2	1	0	0	0	0	0	1	0	1	1	0	0	0
2	$V_{dc}$	Figure 2	1	0	0	0	0	0	1	0	1	0	1	1	0
3	$V_{dc}$	Figure 5	0	0	0	1	1	0	0	0	1	1	0	0	0
4	$0.5 V_{dc}$	Figure 4	1	0	0	0	0	1	0	1	1	1	0	0	0
5	$0.5 V_{dc}$	Figure 4	0	1	1	0	0	1	0	0	1	1	0	0	0
6	$0.5 V_{dc}$	Figure 4	1	1	1	0	0	0	0	1	0	1	0	0	0
7	$0.5 V_{dc}$	Figure 5	1	0	0	0	0	0	0	1	0	1	0	0	0
8	$0.5 V_{dc}$	Figure 2	0	1	1	0	0	0	0	0	0	1	0	0	0
9	$0.5 V_{dc}$	Figure 2	0	0	0	1	1	0	0	0	1	0	1	1	0
10	0 V	Figure 4	1	0	0	0	0	1	0	1	1	0	1	1	0
11	0 V	Figure 4	0	1	1	0	0	1	0	0	1	0	1	1	0
12	0 V	Figure 4	1	1	1	0	0	0	0	1	0	0	1	1	0
13	0 V	Figure 5	1	0	0	0	0	0	0	1	0	0	1	1	0
14	0 V	Figure 5	0	0	0	0	0	1	0	0	1	0	1	1	0
15	0 V	Figure 2	0	1	1	0	0	0	0	0	0	0	1	1	0
16	$-0.5 V_{dc}$	Figure 4	1	0	0	0	0	1	0	1	1	0	0	0	1
17	$-0.5 V_{dc}$	Figure 4	0	1	1	0	0	1	0	0	1	0	0	0	1
18	$-0.5 V_{dc}$	Figure 4	1	1	1	0	0	0	0	1	0	0	0	0	1
19	$-0.5 V_{dc}$	Figure 5	0	0	0	0	0	1	0	0	1	0	0	0	1
20	$-0.5 V_{dc}$	Figure 2	0	1	1	0	0	0	0	0	0	0	0	0	1
21	$-0.5 V_{dc}$	Figure 2	0	0	0	1	1	0	1	1	0	0	1	1	0
22	$-V_{dc}$	Figure 2	0	0	0	0	0	1	1	1	0	0	1	1	0
23	$-V_{dc}$	Figure 5	0	0	0	1	1	0	1	1	0	0	0	0	1
24	$-1.5 V_{dc}$	Figure 2	0	0	0	0	0	1	1	1	0	0	0	0	1



**Figure 2.** Main switching states of the proposed three-phase SCMLI at (a) 0 V, (b)  $0.5 V_{dc}$ , (c)  $V_{dc}$ , (d)  $1.5 V_{dc}$ , (e)  $-0.5 V_{dc}$ , (f)  $-V_{dc}$ , and (g)  $-1.5 V_{dc}$ . (h) The waveform of the phase opposition disposition PWM in the positive quarter cycle (switching frequency  $f_s = 5$  kHz).

### 3. Capacitor Charging Approaches

Two significant approaches are used in this paper to charge capacitors. Approach I that is first proposed in this paper plays an important role in balancing capacitors voltages and makes it possible for the proposed topology to solve the problem of neutral-point voltage imbalance. Approach II is a widely adopted approach that can charge the capacitors together. The equivalent circuits of approach I and approach II are shown in Figure 3a,b, respectively.  $R_{dc1}$ ,  $R_{dc2}$ ,  $R_1$ , and  $R_2$  are the equivalent resistances of the devices.



**Figure 3.** Equivalent circuit of (a) approach I and (b) approach II.

### 3.1. Approach I

All of the DC-link capacitors  $C_{dc1,2}$  and one of the floating capacitors  $C_{1,2}$  were used to realize approach I in this paper. The circuit mode with  $C_1$ ,  $C_{dc1}$  and  $C_{dc2}$  in Figure 3a is taken as an example to illustrate approach I. The approximation that  $C_{dc1} = C_{dc2} = C_1 = C_0$  and  $R_{dc1} = R_{dc2} = R_1 = R_0$  is introduced to simplify the analysis. The following analysis is based on this approximation. According to the topology, the equivalent capacitance  $C_{eq}$  and the equivalent resistance  $R_{eq}$  can be expressed as follows:

$$\begin{aligned} C_{eq} &= \frac{(C_{dc1} + C_1)C_{dc2}}{C_{dc1} + C_1 + C_{dc2}} = \frac{2}{3}C_0 \\ R_{eq} &= \frac{R_{dc1}R_1}{R_{dc1} + R_1} + R_{dc2} = \frac{3}{2}R_0 \end{aligned} \quad (1)$$

Therefore, the current that flows through the DC source is given by

$$i_s = \frac{V_{dc} - u_{eq}(0)}{R_{eq}} e^{-\frac{t}{R_{eq}C_{eq}}}, \quad (2)$$

where

$$u_{eq}(0) = \frac{u_{Cdc1}(0) + u_{C1}(0)}{2} + u_{Cdc2}(0). \quad (3)$$

The voltage of capacitor  $C_{dc2}$  can be expressed as

$$u_{Cdc2} = u_{Cdc2}(0) + \frac{1}{C_{dc2}} \int_0^t i_s dt = \frac{2}{3} [V_{dc} - u_{eq}(0)] (1 - e^{-\frac{t}{R_0 C_0}}) + u_{Cdc2}(0). \quad (4)$$

The voltage of capacitor  $C_{dc1}$  satisfies the following differential equation:

$$u_{Cdc1} + R_{dc1} C_{dc1} \frac{du_{Cdc1}}{dt} = V_{dc} - u_{Cdc2} - i_s R_{dc2} = \frac{V_{dc} + u_{Cdc1}(0) - u_{Cdc2}(0) + u_{C1}(0)}{3}. \quad (5)$$

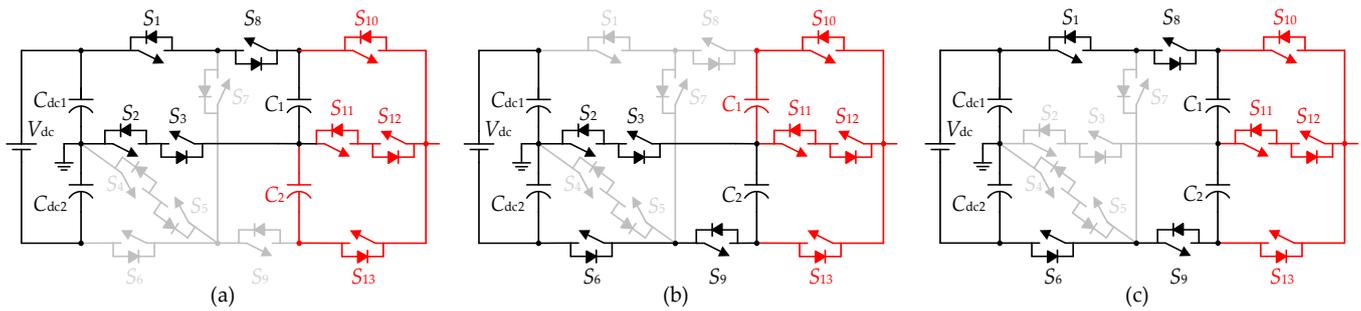
According to Equation (5),  $C_{dc1}$  initial voltage is  $u_{Cdc1}(0)$  and final voltage is  $(V_{dc} + u_{Cdc1}(0) - u_{Cdc2}(0) + u_{C1}(0))/3$ . According to the full response theory of the first order circuit,  $u_{Cdc1}$  can be expressed as

$$u_{Cdc1} = u_{Cdc1}(0) e^{-\frac{t}{R_0 C_0}} + \frac{V_{dc} + u_{Cdc1}(0) - u_{Cdc2}(0) + u_{C1}(0)}{3} (1 - e^{-\frac{t}{R_0 C_0}}). \quad (6)$$

Similarly,  $u_{C1}$  can be expressed as

$$u_{C1} = u_{C1}(0) e^{-\frac{t}{R_0 C_0}} + \frac{V_{dc} + u_{Cdc1}(0) - u_{Cdc2}(0) + u_{C1}(0)}{3} (1 - e^{-\frac{t}{R_0 C_0}}). \quad (7)$$

When  $u_{Cdc1}(0) > 0.5 V_{dc} > u_{Cdc2}(0)$  and  $u_{C1}(0) < 0.5 V_{dc}$ , capacitors  $C_1$  and  $C_{dc2}$  will be charged, and capacitor  $C_{dc1}$  will be discharged according to Equations (4), (6) and (7). When  $u_{Cdc1}(0) < 0.5 V_{dc} < u_{Cdc2}(0)$  and  $u_{C1}(0) > 0.5 V_{dc}$ , capacitors  $C_1$  and  $C_{dc2}$  will be discharged, and capacitor  $C_{dc1}$  will be charged similarly. If approach I is adopted, all relevant capacitor voltages will move toward  $0.5 V_{dc}$ . Furthermore, these voltages will reach  $0.5 V_{dc}$  if  $u_{Cdc1}(0) - u_{Cdc2}(0) + u_{C1}(0) = 0.5 V_{dc}$ . As shown in Figure 4a,  $S_1$ ,  $S_8$ ,  $S_2$ , and  $S_3$  are ON.  $C_1$  and  $C_{dc1}$  are connected in parallel, and approach I is realized. To generate 0 V at the same time,  $S_{11}$  and  $S_{12}$  should be ON. Moreover,  $0.5 V_{dc}$  and  $-0.5 V_{dc}$  can be generated when  $S_{10}$  and  $S_{13}$  are ON, respectively. As shown in Figure 4b,  $S_2$ ,  $S_3$ ,  $S_6$ , and  $S_9$  are ON.  $C_2$  and  $C_{dc2}$  are connected in parallel, and approach I is realized. Similarly, 0 V,  $0.5 V_{dc}$ , and  $-0.5 V_{dc}$  can be generated at the same time.



**Figure 4.** Switching states when (a) approach I is realized and  $C_1$  is used, (b) approach I is realized and  $C_2$  is used, and (c) approach II is realized.

### 3.2. Approach II

Approach II, which is used to balance the floating capacitor voltages, is shown in Figure 3b. Similarly, it is assumed that  $C_1 = C_2 = C_0$  and  $R_1 = R_2 = R_0$ . According to the topology,  $R_{eq} = 2R_0$  and  $C_{eq} = 0.5C_0$ . Therefore,  $i_s$  is given by

$$i_s = \frac{V_{dc} - u_{eq}(0)}{R_{eq}} e^{-\frac{t}{R_{eq}C_{eq}}}, \tag{8}$$

where  $u_{eq}(0) = u_{C1}(0) + u_{C2}(0)$ .  $u_{C1}$  can be calculated as follows:

$$u_{C1} = u_{C1}(0) + \frac{1}{C_1} \int_0^t i_s dt = \frac{1}{2} [V_{dc} - u_{eq}(0)] (1 - e^{-\frac{t}{R_0 C_0}}) + u_{C1}(0). \tag{9}$$

Similarly,  $u_{C2}$  can be expressed as follows:

$$u_{C2} = \frac{1}{2} [V_{dc} - u_{eq}(0)] (1 - e^{-\frac{t}{R_0 C_0}}) + u_{C2}(0). \tag{10}$$

After applying approach II, the average  $u_{C1}$  and  $u_{C2}$  reach  $0.5 V_{dc}$ , according to Equations (9) and (10). Moreover,  $u_{C1}$  and  $u_{C2}$  will reach  $0.5 V_{dc}$  if  $u_{C1}(0) = u_{C2}(0)$ . Approach II can be realized when  $S_1, S_8, S_6,$  and  $S_9$  are ON, as shown in Figure 4c. Any one of  $0 V, 0.5 V_{dc}$ , and  $-0.5 V_{dc}$  can be generated at the same time. These two charging approaches can be realized, which is an important feature of the proposed three-phase SCMLI.

### 4. Control Strategies to Limit Voltage Ripples

To limit voltage ripples, the control strategies of the capacitor voltages are listed in Table 2. For capacitors  $C_1$  and  $C_2$ , the control strategies can be divided into two aspects. The first aspect involves using approach II and making the average of  $u_{C1}$  and  $u_{C2}$  return to  $0.5 V_{dc}$ . Approach II is taken when  $|0.5(u_{C1} + u_{C2}) - 0.5 V_{dc}| > u_\gamma$ .  $u_\gamma$  is an adjustable parameter. The second aspect involves selecting the right path and making  $u_{C1}$  approach  $u_{C2}$ . The path selection for  $C_{1,2}$  is used if  $|0.5(u_{C1} + u_{C2}) - 0.5 V_{dc}| < u_\gamma$ .

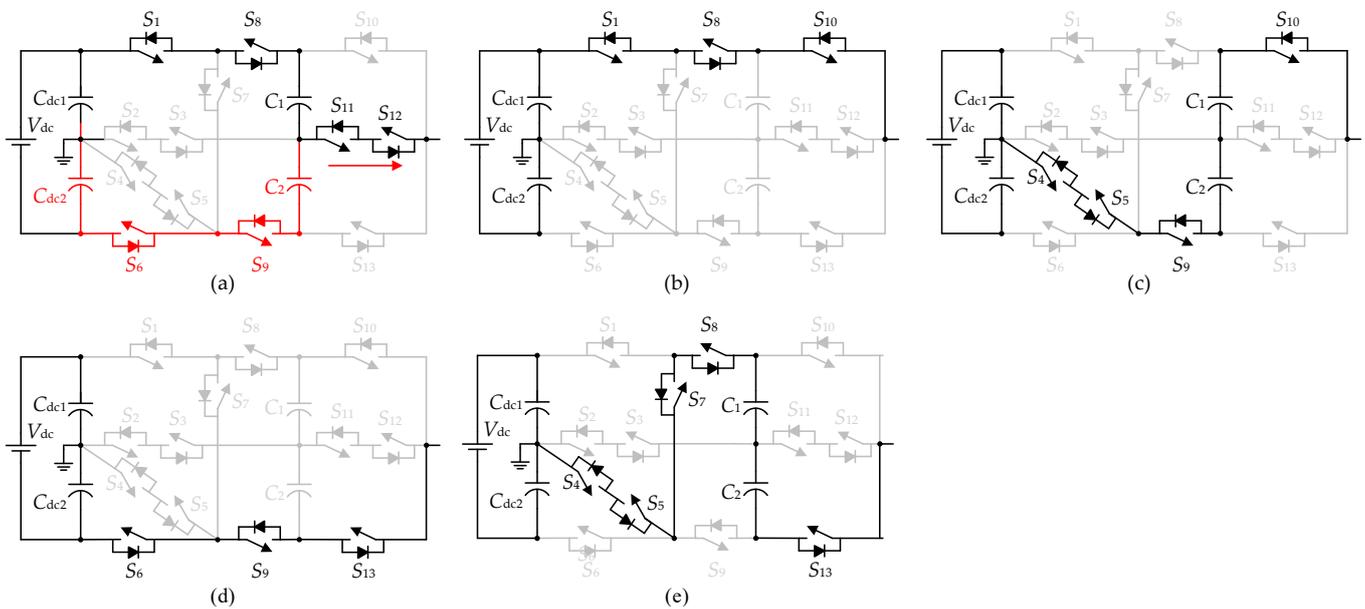
**Table 2.** Control strategies of the capacitor voltages.

Capacitors	Control Strategy
$C_1$ and $C_2$	Approach II, path selection
$C_{dc1}$ and $C_{dc2}$	Approach I, path selection

Similarly, for capacitors  $C_{dc1}$  and  $C_{dc2}$ , the control strategies can be divided into two aspects. The first aspect involves using approach I and making  $u_{C_{dc1}}$  and  $u_{C_{dc2}}$  move toward  $0.5 V_{dc}$ . Approach I is taken when  $|u_{C_{dc1}} - u_{C_{dc2}}| > u_\alpha$ .  $u_\alpha$  is also an adjustable parameter. The second aspect involves selecting the right path and making  $u_{C_{dc1}}$  approach

$u_{C_{dc2}}$ . As  $u_{C_{dc1}} + u_{C_{dc2}} = V_{dc}$ ,  $u_{C_{dc1}}$  and  $u_{C_{dc2}}$  return to  $0.5 V_{dc}$  when  $u_{C_{dc1}}$  reaches  $u_{C_{dc2}}$ . The path selection for  $C_{dc1,2}$  is used if  $|u_{C_{dc1}} - u_{C_{dc2}}| < u_{\alpha}$ .

There are more paths for selection in the proposed topology, and the redundant switching states are depicted in Figure 5a–e. With respect to Figure 5a, the black and red devices represent two different paths.  $S_1, S_8, S_{11}$ , and  $S_{12}$  are ON, and the capacitors  $C_{dc1}$  and  $C_1$  are used to generate 0 V. Similarly,  $S_6, S_9, S_{11}$ , and  $S_{12}$  are ON, and capacitors  $C_{dc2}$  and  $C_2$  are used to generate 0 V. Moreover,  $0.5 V_{dc}$  is generated when  $S_1, S_8$ , and  $S_{10}$  are ON, as shown in Figure 5b, whereas  $-0.5 V_{dc}$  is generated when  $S_6, S_9$ , and  $S_{13}$  are ON, as shown in Figure 5d. In Figure 5c,e, capacitors  $C_1$  and  $C_2$  can be used to generate not only  $V_{dc}$  but also level  $-V_{dc}$ . For capacitors in the proposed topology, path selection is an important control strategy. As shown in Figures 2 and 5, there are various paths for selection at several voltage levels, and the capacitors used are different, making it easier to balance the capacitor voltages. This is one of the main advantages of the proposed topology.



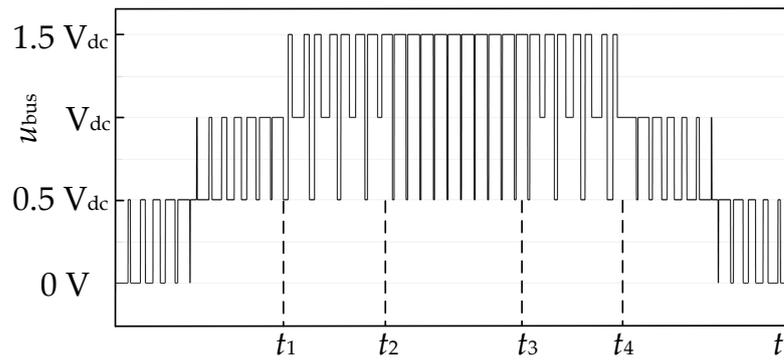
**Figure 5.** Redundant switching states of the proposed three-phase SCMLI structure at (a) 0 V, (b)  $0.5 V_{dc}$ , (c)  $V_{dc}$ , (d)  $-0.5 V_{dc}$ , and (e)  $-V_{dc}$ .

Usually, there is a conflict between the control strategies of  $u_{C_{1,2}}$  and the control strategies of  $u_{C_{dc1,2}}$ . It is important to make a comprehensive decision according to the latest status. In this paper, the top priority is to decide whether to take approach II.  $|0.5(u_{C_1} + u_{C_2}) - 0.5 V_{dc}| > u_{\gamma}$ , and this is the criterion that  $u_{C_1}$  and  $u_{C_2}$  have to meet if approach II is to be taken. After that, approach I is taken when  $|u_{C_{dc1}} - u_{C_{dc2}}| > u_{\alpha}$ . This will make  $u_{C_{dc1}}$  and  $u_{C_{dc2}}$  move toward  $0.5 V_{dc}$ . Then, the path selection for  $C_{dc1,2}$  is used if  $|u_{C_{dc1}} - u_{C_{dc2}}| > u_{\beta}$ .  $u_{\alpha}$  is larger than  $u_{\beta}$ . Lastly, the path selection for  $C_{1,2}$  is used.

The reasons for there being no problem of neutral-point voltage imbalance for the proposed three-phase SCMLI can be divided into two aspects. On the one hand, approach I is adopted in this paper. This approach is an effective measure to balance the capacitor voltages. On the other hand, there are various paths for selection at several voltage levels. These two aspects complement each other, giving the proposed topology the ability to solve the problem of neutral-point voltage imbalance.

### 5. Capacitance Determination

Approach II can be used at 0 V,  $0.5 V_{dc}$ , and  $-0.5 V_{dc}$ . Thus, capacitors  $C_1$  and  $C_2$  are discharged when  $u_{ref} > V_{dc}$  and  $i_{bus} > 0$  in the positive half cycle. To address this problem, an important change to the original modulation method is made in this paper, and the new modulation wave in the positive half cycle is shown in Figure 6.



**Figure 6.** The new modulation wave in the positive half cycle (switching frequency  $f_s = 5$  kHz).

According to the original modulation method, there are two choices in a switching period when  $u_{ref} > V_{dc}$ . These choices are  $u_{bus} = V_{dc}$  and  $u_{bus} = 1.5 V_{dc}$ . In this paper, this condition is expressed as  $u_{bus} \in \{V_{dc}, 1.5 V_{dc}\}$ .  $u_{bus} \in \{0.5 V_{dc}, 1.5 V_{dc}\}$  is added when  $t_1 \leq t \leq t_4$  because the abovementioned control strategies can be realized at  $0.5 V_{dc}$ . Specifically,  $u_{bus} \in \{0.5 V_{dc}, 1.5 V_{dc}\}$  is used in half of the switching periods when  $t_1 \leq t \leq t_2$  or  $t_3 \leq t \leq t_4$ .  $u_{bus} \in \{0.5 V_{dc}, 1.5 V_{dc}\}$  is used in all the switching periods when  $t_2 \leq t \leq t_3$ .

The longest discharging time of floating capacitors is an important SCMLI parameter because the required capacitance can be calculated according to it. The longest discharging time  $t_{ldt}$  of floating capacitors in the proposed three-phase SCMLI can be expressed as

$$t_{ldt} = 2T_s - t_c, \tag{11}$$

where  $T_s$  is the switching period, and  $t_c$  is the minimum duration of  $0.5 V_{dc}$  when  $t_1 \leq t \leq t_2$  or  $t_3 \leq t \leq t_4$ . According to Equation (11), the longest discharging time of floating capacitors in the proposed topology is smaller than  $2T_s$ , which is much shorter than that in other traditional SCMLIs. During the longest discharging time, the current that flows through floating capacitors is  $i_{bus}$ . The voltage variation of floating capacitors that comes from  $i_{bus}$  can be calculated as follows:

$$\frac{\int_{t_{start}}^{t_{end}} i_{bus} dt}{C_{1,2}} \approx \frac{2T_s - t_c}{C_{1,2}} i_{bus}|_{t=t_{start}} < \frac{2T_s}{C_{1,2}} \frac{mA_{boost} V_{dc}}{|Z_{MN}|}, \tag{12}$$

where  $m$  is the modulation index, and  $A_{boost}$  is the voltage gain.  $t_{start}$  and  $t_{end}$  are the start time and end time of the longest discharging time, respectively.  $Z_{MN}$  is the total impedance between point M and point N. Considering that approach I is adopted, Equation (12) needs to satisfy

$$\frac{2T_s}{C_{1,2}} \frac{mA_{boost} V_{dc}}{|Z_{MN}|} < 0.5u_\alpha. \tag{13}$$

According to Equation (13), the required capacitance of floating capacitors can be calculated as follows:

$$C_{1,2} > \frac{4T_s}{u_\alpha} \frac{mA_{boost} V_{dc}}{|Z_{MN}|}. \tag{14}$$

According to Equations (11)–(14), reducing the longest discharging time of the floating capacitors can effectively reduce the capacitance of the floating capacitors.

Approach I, which can make  $u_{C_{dc1}}$  and  $u_{C_{dc2}}$  move toward  $0.5 V_{dc}$ , is taken if  $|u_{C_{dc1}} - u_{C_{dc2}}| > u_\alpha$ . Thus,  $u_{C_{dc1}}$  and  $u_{C_{dc2}}$  can be limited to  $0.5 V_{dc} \pm 0.5 u_\alpha$  with less DC-link capacitance. Similarly, the voltage variation of the DC-link capacitors between

$t_{\text{begin}}$  (the end time of the first approach I) and  $t_{\text{finish}}$  (the start time of the second approach I) can be calculated as follows:

$$\frac{\int_{t_{\text{begin}}}^{t_{\text{finish}}} i_{\text{Cdc1}} dt}{C_{\text{dc1,2}}} \approx \frac{kT_s}{C_{\text{dc1,2}}} i_{\text{Cdc1}}|_{t=t_{\text{begin}}} < \frac{kT_s}{2C_{\text{dc1,2}}} \frac{mA_{\text{boost}} V_{\text{dc}}}{|Z_{\text{MN}}|}, \tag{15}$$

where  $kT_s = t_{\text{finish}} - t_{\text{begin}}$ . To coincide with approach I, Equation (15) needs to satisfy

$$\frac{kT_s}{2C_{\text{dc1,2}}} \frac{mA_{\text{boost}} V_{\text{dc}}}{|Z_{\text{MN}}|} < 0.5u_{\alpha}. \tag{16}$$

According to Equation (16), the required capacitance of the DC-link capacitors can be calculated as follows:

$$C_{\text{dc1,2}} > \frac{kT_s}{u_{\alpha}} \frac{mA_{\text{boost}} V_{\text{dc}}}{|Z_{\text{MN}}|}. \tag{17}$$

According to Equations (14) and (17), the required capacitance of the floating capacitors is similar to that of the DC-link capacitors. Therefore,  $C_{1,2} = C_{\text{dc12}}$  in this paper.

### 6. Efficiency Calculation

In this section, the overall efficiency of the proposed three-phase SCMLI is calculated. First, the conduction loss of the power switches  $P_{\text{con1}}$  can be expressed as

$$P_{\text{con1}} = f_o \sum_{i=1}^{N_{\text{swi}}} \int_0^{T_o} (i_{\text{si}}^2 r_{\text{si}} + i_{\text{si}} V_{\text{si}}) dt, \tag{18}$$

where  $i_{\text{si}}$ ,  $r_{\text{si}}$ , and  $V_{\text{si}}$  are the current, internal resistance, and voltage drop of the  $i$ -th switch, respectively.  $N_{\text{swi}}$  is the number of power switches.  $T_o$  and  $f_o$  are the period and frequency of the output voltage, respectively. The conduction loss  $P_{\text{con2}}$  that comes from the DC-link capacitors and the floating capacitors can be calculated as follows:

$$P_{\text{con2}} = f_o \sum_{i=1}^{N_{\text{ca}}} \int_0^{T_o} i_{\text{Ci}}^2 r_{\text{Ci}} dt, \tag{19}$$

where  $i_{\text{Ci}}$  and  $r_{\text{Ci}}$  are the current and the internal resistance of the  $i$ -th capacitor, respectively.  $N_{\text{ca}}$  is the number of capacitors. The conduction loss of the output filters  $P_{\text{con3}}$  can be calculated as follows:

$$P_{\text{con3}} = f_o \sum_{i=1}^{N_{\text{fil}}} \int_0^{T_o} (i_{\text{Lfi}}^2 r_{\text{Lfi}} + i_{\text{Cfi}}^2 r_{\text{Cfi}}) dt, \tag{20}$$

where  $i_{\text{Lfi}}$  and  $r_{\text{Lfi}}$  are the current and the internal resistance of the  $i$ -th filter inductor, respectively.  $i_{\text{Cfi}}$  and  $r_{\text{Cfi}}$  are the current and the internal resistance of the  $i$ -th filter capacitor, respectively.  $N_{\text{fil}}$  is the number of filters.

To simplify the analysis, the voltage and the current of the power switches are considered to have a linear relation with time during the switching process. Therefore, the switching loss  $P_{\text{off}(i,j)}$  that is caused by the  $j$ -th turning OFF process of the  $i$ -th switch is given by

$$P_{\text{off}(i,j)} = f_o \int_0^{t_{\text{off}}} v(t) i(t) dt = f_o \int_0^{t_{\text{off}}} \frac{V_{\text{off}(i,j)}}{t_{\text{off}}} t \left[ -\frac{I_{\text{off}(i,j)}}{t_{\text{off}}} (t - t_{\text{off}}) \right] dt = \frac{1}{6} V_{\text{off}(i,j)} I_{\text{off}(i,j)} t_{\text{off}} f_o, \tag{21}$$

where  $V_{\text{off}(i,j)}$  and  $I_{\text{off}(i,j)}$  are the voltage after the turning OFF process and the current before the turning OFF process, respectively. Similarly, switching loss  $P_{\text{on}(i,j)}$  that is caused by the  $j$ -th turning ON process of the  $i$ -th switch is given by

$$P_{\text{on}(i,j)} = \frac{1}{6} V_{\text{on}(i,j)} I_{\text{on}(i,j)} t_{\text{on}} f_o, \quad (22)$$

where  $V_{\text{on}(i,j)}$  and  $I_{\text{on}(i,j)}$  are the voltage before the turning ON process and the current after the turning ON process, respectively. According to Equations (21) and (22), the total switching loss  $P_{\text{sw}}$  can be calculated by

$$P_{\text{sw}} = \sum_{i=1}^{N_{\text{swi}}} \left( \sum_{j=1}^{N_{\text{on}(i)}} P_{\text{on}(i,j)} + \sum_{j=1}^{N_{\text{off}(i)}} P_{\text{off}(i,j)} \right) = \frac{1}{6} f_o \sum_{i=1}^{N_{\text{swi}}} \left( t_{\text{on}} \sum_{j=1}^{N_{\text{on}(i)}} V_{\text{on}(i,j)} I_{\text{on}(i,j)} + t_{\text{off}} \sum_{j=1}^{N_{\text{off}(i)}} V_{\text{off}(i,j)} I_{\text{off}(i,j)} \right), \quad (23)$$

where  $N_{\text{on}(i)}$  and  $N_{\text{off}(i)}$  are the number of  $i$ -th switch turning ON processes and turning OFF processes, respectively.

According to Equations (18)–(20), and (23), the overall efficiency of the proposed topology is given by

$$\eta = \frac{P_o}{P_o + P_{\text{con1}} + P_{\text{con2}} + P_{\text{con3}} + P_{\text{sw}}}. \quad (24)$$

## 7. Simulation Results and Comparison

### 7.1. Simulation Results

MATLAB/Simulink was chosen as the simulation software. The parameters of the proposed three-phase SCMLI are listed in Table 3. The input voltage was set as 200 V, which resembles many other SCMLIs. Thus, the rated voltage of the capacitors was 100 V. The modulation ratio was 0.95, and the output voltage was 285 ( $300 \times 0.95$ ) V. The capacitance used was 200  $\mu\text{F}$ , which meets the requirement of Equation (15). The output power was 1884 W, and the resistive–inductive load  $Z_1$  was 40  $\Omega$ , 100 mH.  $u_\alpha$  was 8 V since the maximum allowable voltage ripple of capacitors was 10 V (10% of the rated voltage). The filter capacitor was 80  $\mu\text{F}$ , and the filter inductor was 4 mH. The switching frequency was 20 kHz. This frequency can reduce the requirement of capacitance according to Equation (15). The output frequency was 50 Hz.

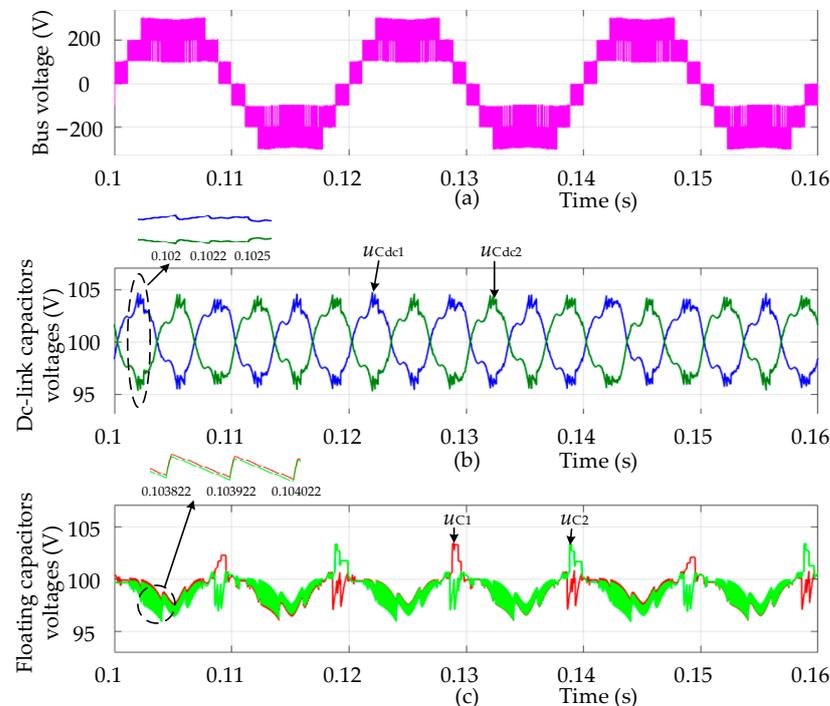
**Table 3.** Parameters of the proposed three-phase SCMLI.

Parameters	Value
$V_{\text{dc}}$	200 V
Capacitor rated voltage	100 V
Modulation ratio	0.95
Output voltage	285 V
$C_1, C_2, C_{\text{dc1}},$ and $C_{\text{dc2}}$	200 $\mu\text{F}$
Output power	1884 W
Resistive–inductive load $Z_1$	40 $\Omega$ , 100 mH
$u_\alpha$	8 V
Filter capacitor	80 $\mu\text{F}$
Filter inductor	4 mH
Switching frequency	20 kHz
Output frequency	50 Hz

#### 7.1.1. Performance in Three-Phase Four-Wire System

To assess the performance of the proposed three-phase SCMLI in the three-phase four-wire system,  $Z_o = Z_1$  is given. Figure 7a shows the observed A-phase bus voltage. The top voltage level was 300 V, and the proposed three-phase SCMLI could boost the input voltage. Because  $u_\alpha$  was equal to 8 V, the voltages of the DC-link capacitors in the A-phase were limited to 96–104 V, as shown in Figure 7b. Approach I could move the voltage of DC-link capacitors toward 100 V when they were larger than 104 V or smaller than 96 V.

Figure 7c shows the floating capacitor voltages in the A-phase, which were approximately 96–103 V. It can be seen in this figure that the longest discharging time of floating capacitors was shorter than  $2T_s$ . These waveforms meet the voltage ripple requirement, which should be less than 10% of the rated voltage.



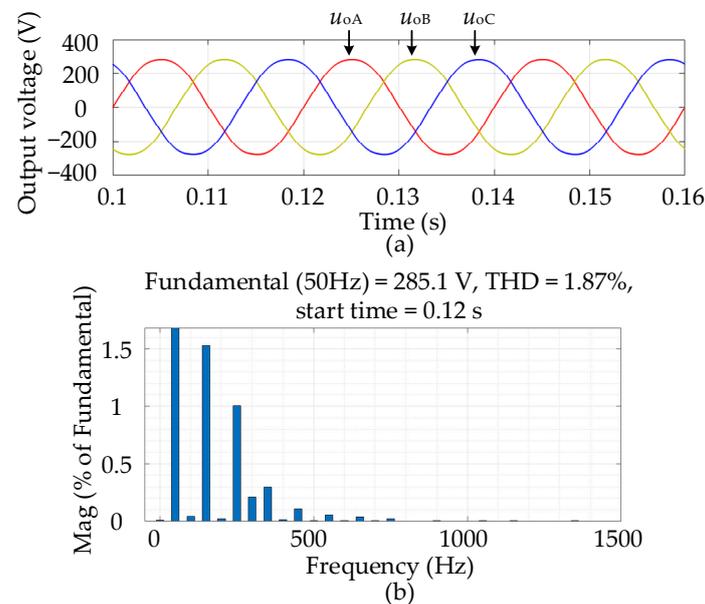
**Figure 7.** (a) The bus voltage, (b) DC-link capacitor voltages and (c) floating capacitor voltages of the A-phase under the resistive–inductive load condition.

The output voltage of each phase under the resistive–inductive load condition is shown in Figure 8a, and the fast Fourier transform (FFT) result of the A-phase output voltage is shown in Figure 8b. According to the result, THD = 1.87%, and the amplitude of the fundamental component was 285.1 V. This amplitude agrees with the modulation ratio because the desired amplitude of the output voltage was 285 V. Similarly, the output current of each phase under the resistive–inductive load condition is shown in Figure 9a, and the FFT result of the A-phase output current is shown in Figure 9b. THD = 0.83%, and the amplitude of the fundamental component was 5.605 A. The quality of all the waveforms was high, which is attributable to the low-voltage ripples of the capacitors.

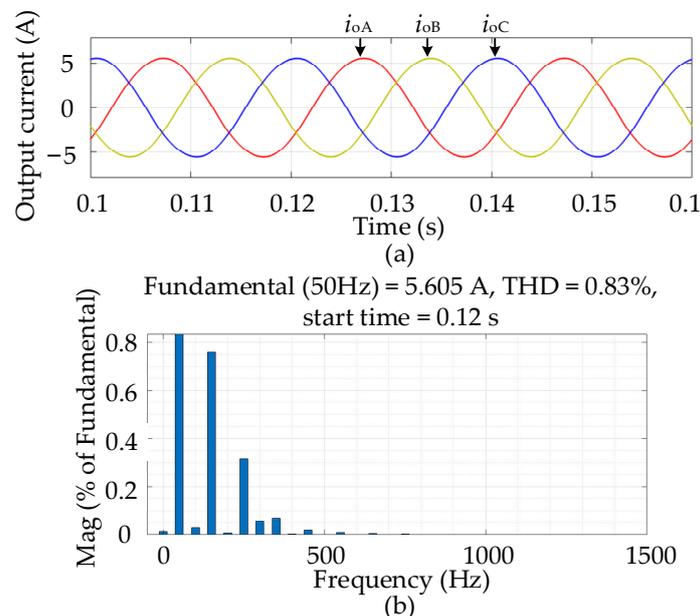
To further test the performance of the proposed three-phase SCMLI, a resistive–inductive load transient is given. The time when the load changed from  $Z_o = 2Z_1$  to  $Z_o = Z_1$  was 0.12 s. The bus voltage of the A-phase is shown in Figure 10a. The difference between the waveform before 0.12 s and the waveform after 0.12 s was not notable. Figure 10b shows the A-phase DC-link capacitor voltages. The voltage ripple of these capacitors was 8 V during the entire process ( $u_\alpha = 8$  V). Figure 10c shows the A-phase floating capacitor voltages. The transient process only lasted for a short period of time (approximately 0.01 s). After that, the floating capacitor voltages quickly returned to the steady state. These waveforms also meet the voltage ripple requirements and are in good agreement with the abovementioned theoretical analysis.

The output voltage of each phase during a resistive–inductive load transient is shown in Figure 11a, and the FFT result of the A-phase output voltage is shown in Figure 11b. THD = 1.96%, and the start time was 0.12 s. There was no significant change in the output voltage of each phase after 0.12 s. The output current of each phase under the same resistive–inductive load transient is shown in Figure 12. Similarly, the transient process only lasted for a short period of time. The output current of each phase quickly changed

from the initial steady state to a new steady state. Thus, there is no need to worry about the overvoltage problem or the overcurrent problem.



**Figure 8.** (a) The output voltage of each phase under the resistive–inductive load condition. (b) The FFT result of the A-phase output voltage.



**Figure 9.** (a) The output current of each phase under the resistive–inductive load condition. (b) The FFT result of the A-phase output current.

To test the presented three-phase SCMLI more rigorously, a special load with a temporary three-phase unbalanced disturbance is given. For each phase,  $Z_o = 2Z_1$ . A disturbance load  $R_d = 100 \Omega$  was only added to the A-phase when  $0.8 \text{ s} < t < 0.85 \text{ s}$ . Under this condition, Figure 13a shows the A-phase bus voltage, and there was no obvious change in the waveform when  $0.8 \text{ s} < t < 0.85 \text{ s}$  or  $t > 0.85 \text{ s}$ . Figure 13b shows the A-phase DC-link capacitor voltages. Similarly, the transient process only lasted for a short period of time (approximately 0.01 s). During this transient process,  $u_{C_{dc2}}$  was momentarily larger than 104 V, and  $u_{C_{dc1}}$  was momentarily smaller than 96 V. After that, the DC-link capacitor volt-

ages were limited to 96–104 V, as before. Figure 13c shows the A-phase floating capacitor voltages. During the same transient process,  $u_{C2}$  was momentarily larger than 105 V. After that, the floating capacitor voltages quickly returned to the steady state.

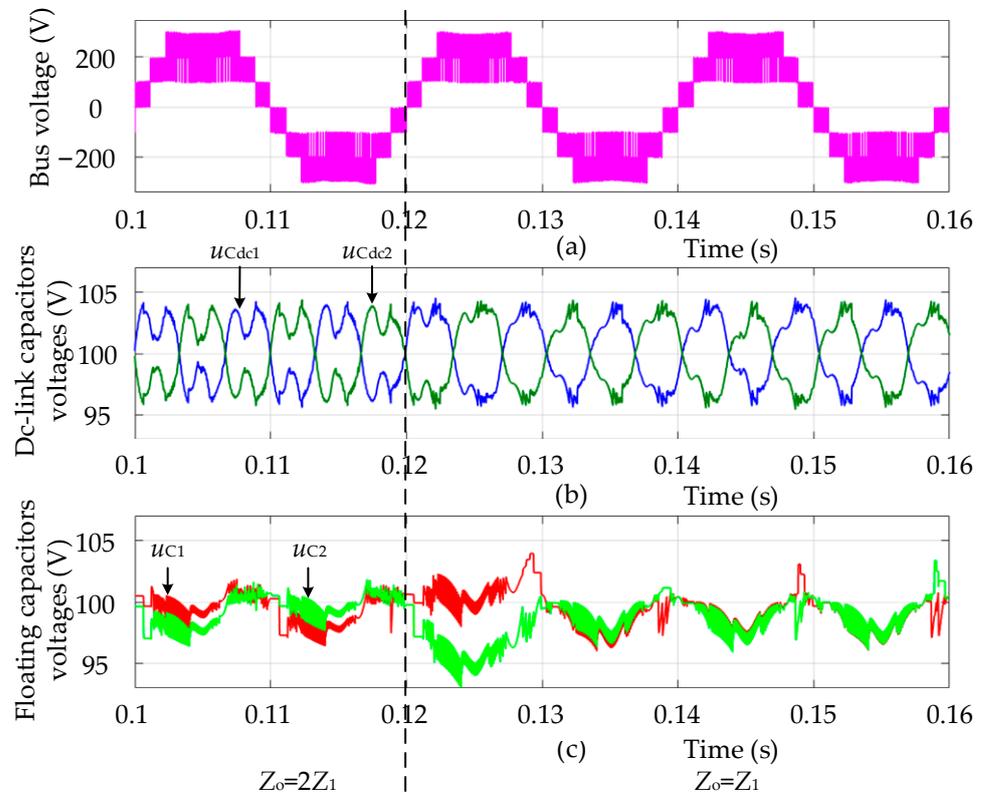


Figure 10. (a) The bus voltage, (b) DC-link capacitor voltages and (c) floating capacitor voltages of the A-phase during a resistive–inductive load transient.

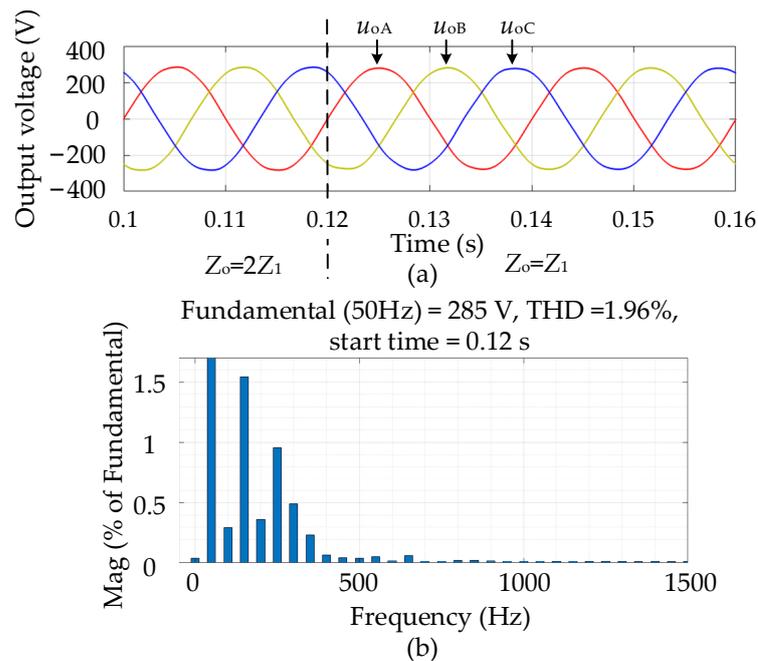


Figure 11. (a) The output voltage of each phase during a resistive–inductive load transient. (b) The FFT result of the A-phase output voltage.

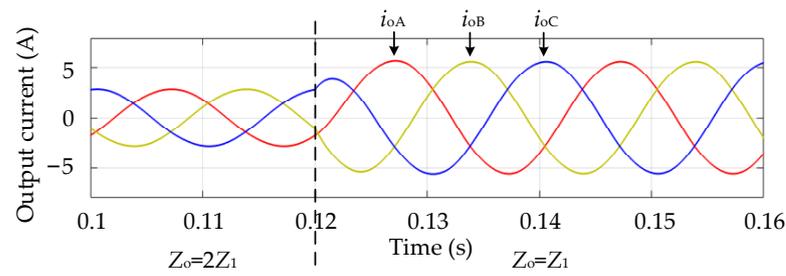


Figure 12. The output current of each phase during a resistive–inductive load transient.

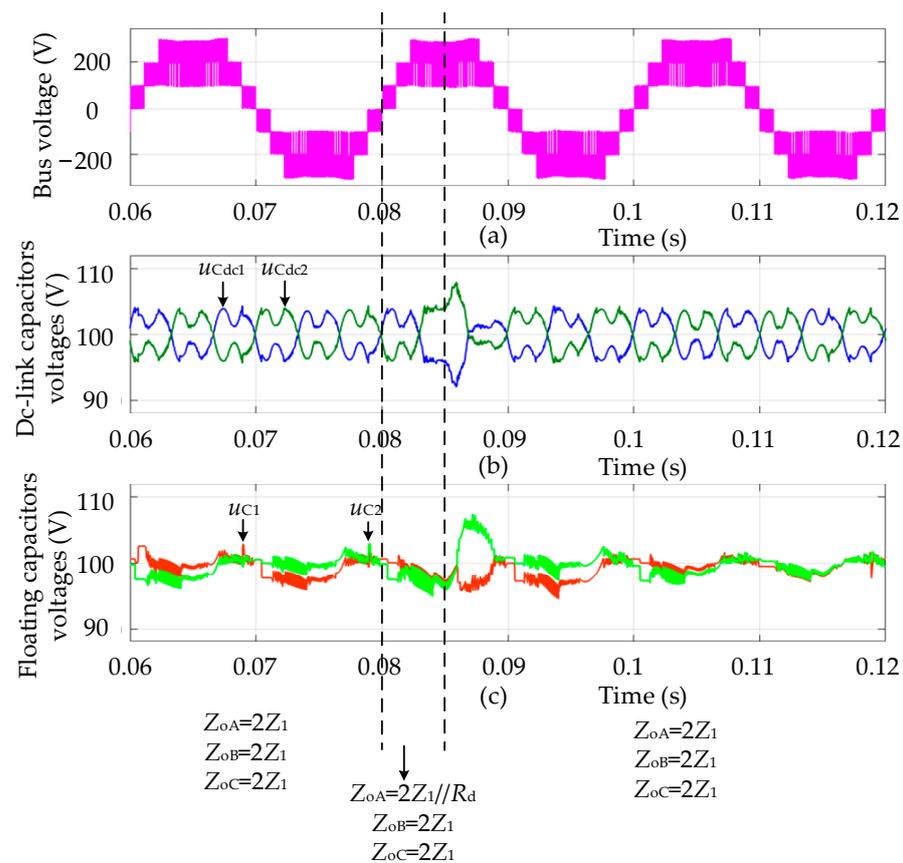


Figure 13. (a) The bus voltage, (b) DC-link capacitor voltages and (c) floating capacitor voltages of the A-phase when the disturbance load was added to the A-phase.

When the disturbance load was added to the A-phase, the output voltage of each phase was as shown in Figure 14a, and the FFT result of the A-phase output voltage was as shown in Figure 14b. THD = 3.28%, and the start time was 0.08 s. The change in the output voltage of each phase during the transient process was small.

When the disturbance load was added to the A-phase, the output current of each phase was as shown in Figure 15. The amplitude of the A-phase output current  $i_{oA}$  increased because of the disturbance load when  $0.8 \text{ s} < t < 0.85 \text{ s}$ . After that ( $t > 0.85 \text{ s}$ ), the A-phase output current  $i_{oA}$  quickly returned to the steady state. As for  $i_{oB}$  and  $i_{oC}$ , the disturbance load had no effect because it was only added to the A-phase.

All these observed waveforms in the three-phase four-wire system are in good agreement with the theoretical analyses, confirming the feasibility of the proposed three-phase SCMLI in the three-phase four-wire system.

The recorded efficiency of different topologies is shown in Figure 16. The efficiency decreased with increasing output power. Compared with [27,30], the proposed topology

has greater efficiency. The efficiency of the proposed topology is similar to that of [31]. As shown in Figure 17, the share of total conduction loss was larger than that of switching loss. This is because the switching frequency was at a normal level. Furthermore, the share of switching loss increased with decreasing output power. Therefore, decreasing the switching frequency can be adopted to improve the efficiency of the proposed topology when the output power is lower than 800 W.

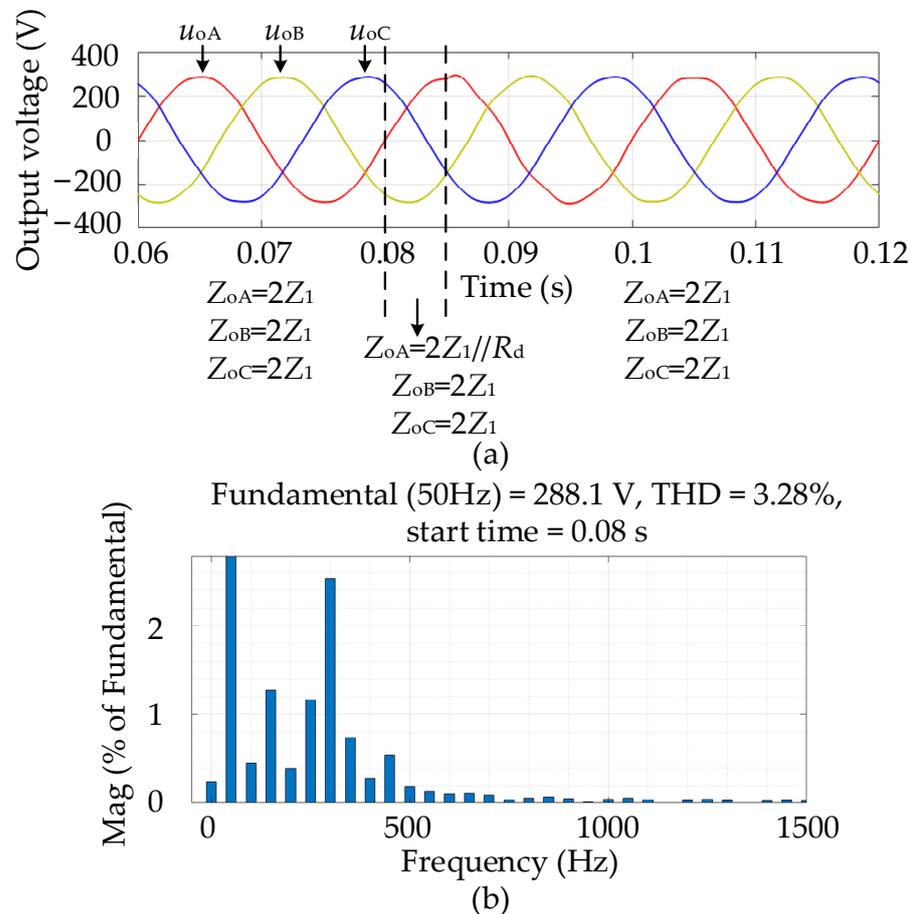


Figure 14. (a) The output voltage of each phase when the disturbance load was added to the A-phase. (b) The FFT result of the A-phase output voltage.

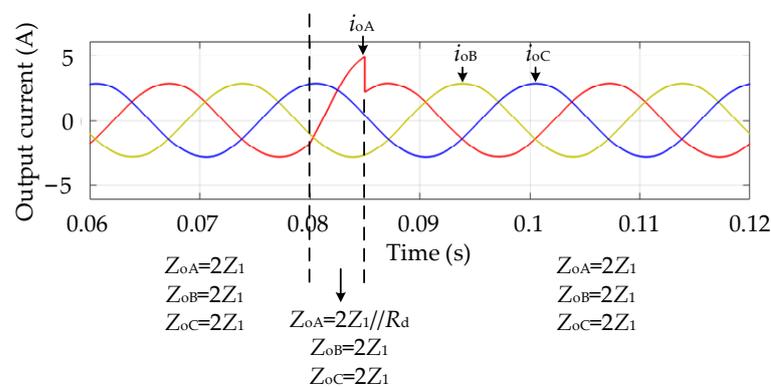


Figure 15. The output current of each phase when the disturbance load was added to the A-phase.

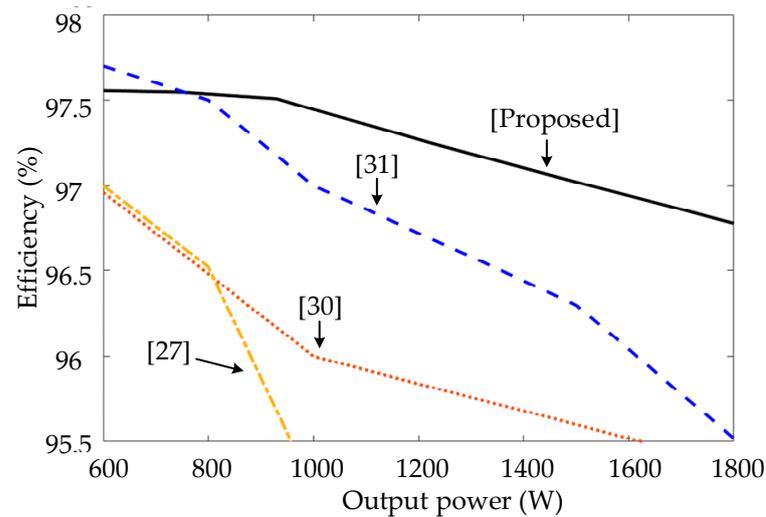


Figure 16. Recorded efficiency of different topologies.

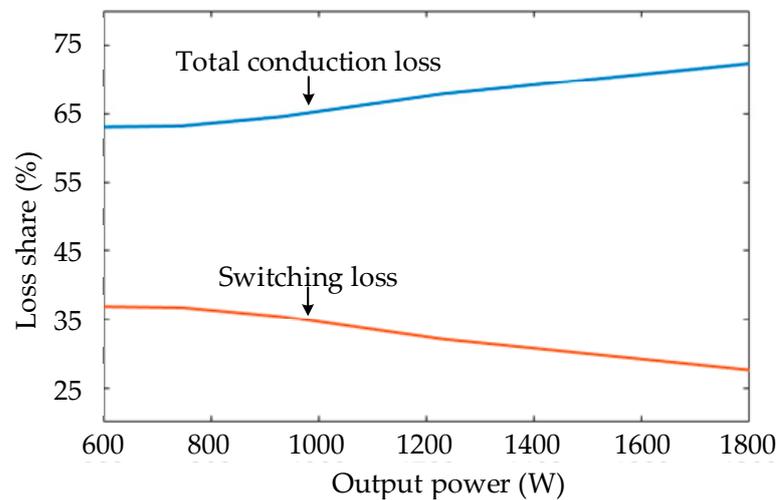


Figure 17. The share of switching loss and total conduction loss.

### 7.1.2. Performance in Three-Phase Three-Wire System

To test the performance of the proposed three-phase SCMLI in a three-phase three-wire system, the same resistive–inductive load transient is given. The A-phase bus voltage is shown in Figure 18a. Because  $u_{NO}$  was not always equal to 0, the bus voltage had more voltage levels. The resistive–inductive load transient had no effect on the bus voltage. Figure 18b shows the DC-link capacitor voltages of the A-phase. The voltage ripple of these capacitors was 10 V. Figure 18c shows the floating capacitor voltages of the A-phase. They changed from 98–101 V to 96–104 V. All these waveforms met the voltage ripple requirements during the entire process.

The output voltage of each phase during a resistive–inductive load transient is shown in Figure 19a, and the FFT result of the A-phase output voltage is shown in Figure 19b. THD = 0.90%, and the start time was 0.12 s. Even in the first period after 0.12 s, the waveform quality of each phase output voltage satisfied the requirement. The output current of each phase under the same resistive–inductive load transient is shown in Figure 20. The transient process only lasted for a short period of time. The output current of each phase quickly changed from the initial steady state to a new steady state.

The problem of neutral-point voltage imbalance became more serious for traditional SCMLIs in the three-phase three-wire system. In contrast, these observed waveforms were in line with expectations, confirming that the proposed three-phase SCMLI achieves good

performance in a three-phase three-wire system and there is no problem of neutral-point voltage imbalance.

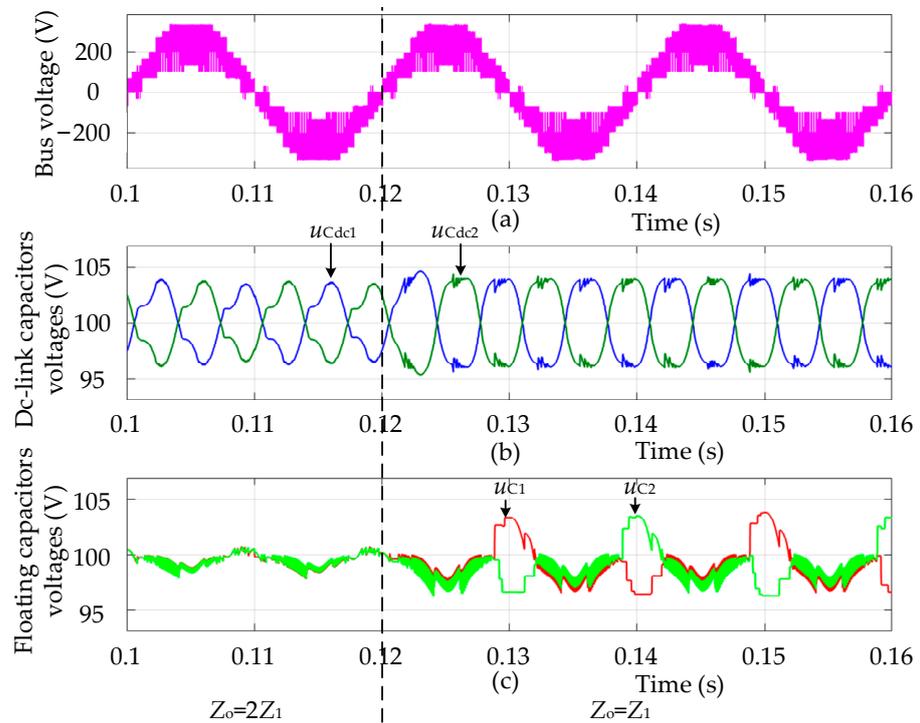


Figure 18. (a) The bus voltage, (b) DC-link capacitor voltages and (c) floating capacitor voltages of the A-phase during a resistive-inductive load transient.

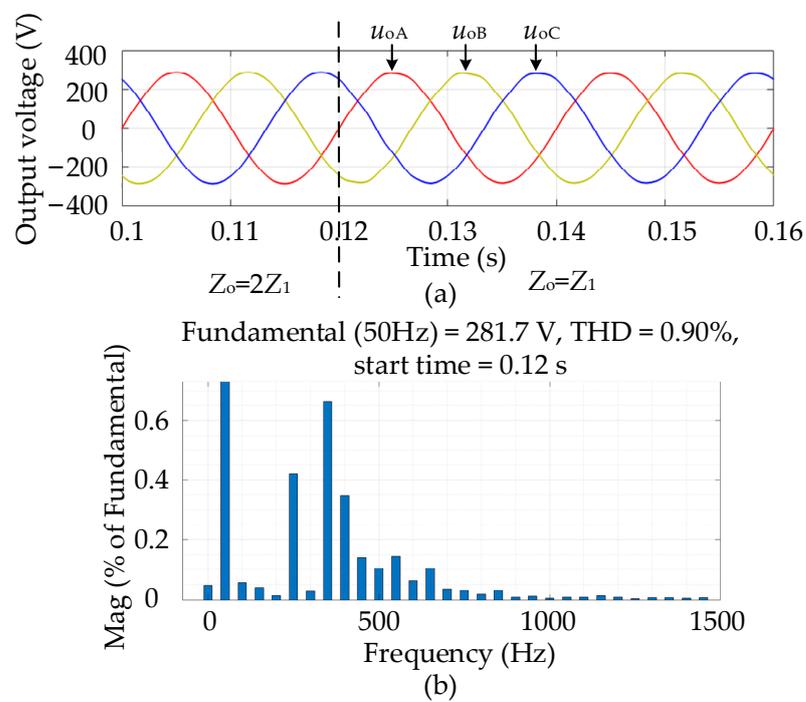


Figure 19. (a) The output voltage of each phase during a resistive-inductive load transient. (b) The FFT result of the A-phase output voltage.

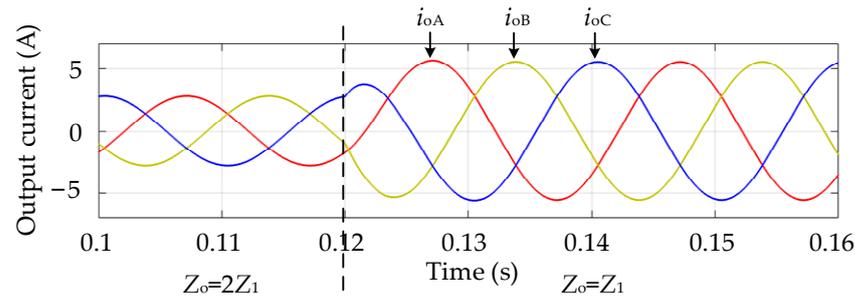


Figure 20. The output current of each phase during a resistive–inductive load transient.

7.2. Comparison

To better illustrate the advantages of the proposed topology, a comprehensive comparison with other up-to-date SCMLIs in various aspects is shown in Table 4. The main advantages of the proposed topology are as follows:

- (1) Less capacitance (200  $\mu\text{F}$ ) is used.

Table 4. Comparison of different topology results.

	[19]	[20]	[26]	[27]	[30]	[31]	[32]	[33]	Proposed Topology
$C_{\text{DC-link}}$	4700	-	-	-	-	-	1000	4700	200
	4700	-	-	-	-	-	1000	4700	200
$C_{\text{floating}}$	4700	6800	4330	1000	2200	2200	1000	4700	200
	4700	3300	2190	1000	2200	/2200	1000	4700	200
$N_{\text{ca\_3p}}$	8	9	9	6	9	6	5	5	8
$TRV_{\text{ca\_3p}}$	4	15	15	3	6	3	4	4	4
$\epsilon_{\text{ca}}$	100%	100%	80%	100%	50%	100%	100%	100%	100%
$N_{\text{DC\_3p}}$	1	3	3	3	3	3	1	1	1
Load condition	40 $\Omega$	50 $\Omega$	42.2 $\Omega$	200 $\Omega$	30 $\Omega$	10 $\Omega$	160 $\Omega$	40 $\Omega$	40 $\Omega$
	100 mH	30 mH	79 mH	200 $\Omega$	30 mH	100 mH	160 $\Omega$	100 mH	100 mH
$m$	1.0	0.9	0.91	1.0	1.0	1.0	1.0	1.0	0.95
Suffering from imbalance	yes	no	no	yes	yes	yes	yes	yes	no
$A_{\text{boost}}$	1.5	6	4	2	2	2	1.5	1.5	1.5
$N_{\text{level}}$	7	13	9	9	9	9	7	7	7
$N_{\text{sd}}$	10	15	12	11	11	10	9	9	13
$TSV_{\text{sw}}$	9	33	24	12	10	11	8	8	11

$C_{\text{DC-link}}$  is the DC-link capacitance ( $\mu\text{F}$ ).  $C_{\text{floating}}$  is the floating capacitance ( $\mu\text{F}$ ).  $N_{\text{ca\_3p}}$  is the number of capacitors in the three-phase applications.  $TRV_{\text{ca\_3p}}$  is the total rated voltage of capacitors (Vdc) in the three-phase applications.  $\epsilon_{\text{ca}}$  is the share of the floating capacitors voltages that are used to generate the top voltage level.  $N_{\text{DC\_3p}}$  is the number of DC sources in the three-phase applications.  $N_{\text{level}}$  is the number of voltage levels.  $N_{\text{sd}}$  is the number of power switches and diodes in each phase.  $TSV_{\text{sw}}$  is the total standing voltage of switches ( $V_{\text{dc}}$ ) in each phase.

In most SCMLIs, the required capacitance is usually greater than 2000  $\mu\text{F}$ , thus increasing the volume and cost of the system. The capacitance used in [27,32] was 1000  $\mu\text{F}$ , but the load impedance ( $>150 \Omega$ ) was much larger than that of other SCMLIs. The required capacitance increases with decreasing load impedance. The cost of capacitors increases with higher rated voltage, making the advantage of reduced capacitance in the proposed topology more obvious.

- (2) There is no problem of neutral-point voltage imbalance.

The DC-link converter brings the problem of neutral-point voltage imbalance to [19,27,30–33]. The self-balancing characteristic of these SCMLIs self-regulates the average neutral point voltage to a certain value (usually half the DC-link voltage). However, the self-balancing time is long, and the neutral-point voltage may drift excessively. Additional hardware or software measures need to be taken to solve this problem. Regarding software

measures, there is little research about this problem in SCMLIs. Hardware measures, such as adding additional components to the system, increase the volume and cost of the system.

- (3) Good performance is achieved in not only the three-phase four-wire system but also the three-phase three-wire system.

Most traditional three-phase SCMLIs [19,32,33] suffer from the problem of neutral-point voltage imbalance, which becomes more serious in the three-phase three-wire system. Owing to the advantage above, the proposed topology can be adopted in more applications.

- (4) Only one DC source is used as a three-phase topology.

The methods used in [20,26,27,30,31] all represent single-phase topologies. In the three-phase applications, three DC sources are required for such topologies. This advantage of the proposed topology reduces the complexity and cost of the system.

- (5) All floating capacitors are used to generate the top voltage level.

Not all floating capacitors were used to generate the top voltage level in [26,30]. The voltages of these floating capacitors are underused. This advantage of the proposed topology reduces the demand for capacitors.

Furthermore, the proposed topology is simple. Thirteen power switches are used in each phase, and the sum of their voltage stresses is only  $11 V_{dc}$ , which reaches the average level of other SCMLIs. Two DC-link capacitors and two floating capacitors in each phase are used, and the sum of their rated voltages is  $4 V_{dc}$ , which is not larger than that of the other three-phase SCMLIs. The proposed topology can generate seven voltage levels under different kinds of load conditions.

## 8. Conclusions

A novel three-phase SCMLI with reduced capacitance and balanced neutral-point voltage was proposed in this paper. Good performance was achieved in not only the three-phase four-wire system but also the three-phase three-wire system. Only one DC source was used in the three-phase topology. A comprehensive comparison with other recently presented SCMLIs in various aspects was made, and simulation results under different kinds of load conditions were given. All observed waveforms were in good agreement with the theoretical analyses, confirming the feasibility of the proposed three-phase SCMLI.

**Author Contributions:** Conceptualization, Z.X.; methodology, Z.X.; software, Z.X.; validation, Z.X. and Z.H.; formal analysis, Z.X.; investigation, Z.X.; resources, Z.X.; data curation, Z.X.; writing—original draft preparation, Z.X. and Z.H.; writing—review and editing, Z.X. and Z.H.; visualization, Z.X.; supervision, H.D.; project administration, H.D.; funding acquisition, H.D. All authors have read and agreed to the published version of the manuscript.

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## Nomenclature

$u_N$	Rated voltage of capacitors.
$V_{dc}$	Input DC voltage.
$f_s$ and $T_s$	Switching frequency and switching period.
$A_c$	Amplitude of the carrier waveform.
$u_{ref}$	Reference voltage.
$u_{bus}$	Bus voltage.
$R_{dc1}, R_{dc2}, R_1$ and $R_2$	Equivalent resistance of the devices.
$R_0$ and $C_0$	It is assumed that $R_{dc1} = R_{dc2} = R_1 = R_2 = R_0$ and $C_{dc1} = C_{dc2} = C_1 = C_2 = C_0$ .
$R_{eq}$ and $C_{eq}$	Equivalent resistance and equivalent capacitance of the charging topology.
$i_s$	Current that flows through the DC source in the charging topology.

$u_{Cd1}, u_{Cd2}, u_{C1}, u_{C2}$	Voltage of capacitors.
$i_{Cd1}, i_{Cd2}, i_{C1}, i_{C2}$	Current of capacitors.
$u_{Cdc1}(0), u_{Cdc2}(0), u_{C1}(0), u_{C2}(0)$	Initial voltage of capacitors.
$u_{eq}(0)$	Initial voltage of the equivalent capacitor.
$u_{\alpha}, u_{\beta}, u_{\gamma}$	Adjustable parameters that represent the requirements of selecting the appropriate control strategy.
$i_{bus}$	Bus current that flows through the filter inductor.
$t_{ldt}$	The longest discharging time of floating capacitors.
$t_c$	Minimum duration of 0.5 $V_{dc}$ voltage level.
$m$	Modulation index.
$A_{boost}$	Voltage gain.
$t_{start}$ and $t_{end}$	Start time and end time of the longest discharging time.
$Z_{MN}$	Total impedance between point M and point N (can be calculated by the filter parameter and the load condition).
$t_{begin}$ and $t_{finish}$	End time of the first approach I and Start time of the next approach I.
$k$	A parameter that satisfies the equation $kT_s = t_{finish} - t_{begin}$ .
$P_{con1}$	Conduction loss of the power switches.
$i_{si}, r_{si}$ , and $V_{si}$	Current, internal resistance and voltage drop of the $i$ th switch.
$N_{swi}$	Number of power switches.
$f_o$ and $T_o$	Frequency and period of the output voltage.
$P_{con2}$	Conduction loss that comes from DC-link and floating capacitors.
$i_{Ci}$ and $r_{Ci}$	Current and internal resistance of the $i$ th capacitor.
$N_{cap}$	Number of capacitors.
$P_{con3}$	Conduction loss of the output filters.
$i_{Lfi}$ and $r_{Lfi}$	Current and internal resistance of the $i$ -th filter inductor.
$i_{Cfi}$ and $r_{Cfi}$	Current and internal resistance of the $i$ -th filter capacitor.
$N_{fil}$	Number of filters.
$P_{off(i,j)}$	Switching loss caused by the $j$ -th turning OFF process of the $i$ -th switch.
$V_{off(i,j)}$ and $I_{off(i,j)}$	Voltage after the $j$ -th turning OFF process of the $i$ -th switch and current before the $j$ -th turning OFF process of the $i$ -th switch
$P_{on(i,j)}$	Switching loss caused by the $j$ -th turning ON process of the $i$ -th switch.
$V_{on(i,j)}$ and $I_{on(i,j)}$	Voltage before the $j$ -th turning ON process of the $i$ -th switch and current after the $j$ -th turning ON process of the $i$ -th switch.
$P_{sw}$	Total switching loss.
$N_{on(i)}$ and $N_{off(i)}$	Number of $i$ -th switch turning ON processes and turning OFF processes.
$\eta$	Overall efficiency of the proposed topology.
$P_o$	Output power.
$Z_o$	Load impedance.
$Z_1$	Load condition that is adopted in this paper.
$R_d$	A disturbance load that is only added to the A-phase temporarily.

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