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K-Band Hetero-Stacked Differential Cascode Power Amplifier with High Psat and Efficiency in 65 nm LP CMOS Technology

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Abstract: A K-band complementary metal-oxide-semiconductor (CMOS) differential cascode power amplifier is designed with the thin-oxide field effect transistor (FET) common source (CS) stage and thick-oxide FET common gate (CG) stage. Use of the thick-oxide CG stage affords the high supply voltage to 3.7 V and enables the high output power. Additionally, simple analysis shows that the gain degradation due to the low cut-off frequency of the thick-oxide CG FET can be compensated by the high output resistance of the thick-oxide FET if the inter-stage node is neutralized. The measured results of the proposed power amplifier demonstrate the saturated output power of the 23.3 dBm with the 31.3% peak power added efficiency (PAE) at 24 GHz frequency. The chip is fabricated in 65-nm low power (LP) CMOS technology and the chip size including all pads is 700 µm × 630 µm.

Keywords: power amplifier; CMOS; K-band; stacked power amplifier; cascode amplifier

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1. Introduction

Rapid scaling of CMOS technology enables the mm-wave transceiver design including 5G mobile communications and automotive radar applications. Despite many advantages of the CMOS process, such as high-density integration of radio frequency (RF) and digital building blocks and low-cost mass manufacturing capability, the output power degradation due to the low breakdown voltage of highly scaled CMOS devices is a serious weakness for the design of RF power amplifiers. Accordingly, various design approaches for CMOS power amplifiers have been studied to achieve high efficiency and output power. Series voltage or parallel current combining techniques are essential to obtain high output power. Another approach to increase the output power is to stack the FETs for high voltage swing [1]. The larger the number of cascoded transistors increase, the higher the supply voltage can be used. Accordingly, the maximum output power also increases. However, the available number of stacked FETs is not unlimited due to breakdown issues in the common gate (CG) stage [2].

This paper presents a K-band differential power amplifier using the hetero-stacked cascode structure adopting two different gate oxide thicknesses. The common source (CS) stage uses a normal field effect transistor (FET) with the shortest gate length available from the process for high current driving capability, and the CG stage uses the thick-oxide FET for the high voltage swing. Though the hetero-stacked cascode power amplifier (PA) has been used for low GHz applications in a single-ended fashion [3], the PA above the X-band has not adopted this structure because of gain and efficiency degradation due to the low cut-off frequency of the thick-oxide FET. This work shows that the high gain as well as the high output power can be achieved near the cut-off frequencies of the thick CG FET by neutralizing the inter-stage node for the hetero-stacked cascode amplifier.

2. High Frequency Gain of the Neutralized Hetero-Stacked Cascode Amplifier

The thick-oxide common gate (CG) field effect transistor (FET) used in the cascode amplifier can enhance the output power by allowing a high supply voltage without multi-stage stacking. However, as the operation frequency increases, the efficiency and gain tend to more rapidly decrease because of the lower inter-stage pole frequency due to the smaller transconductance of the thick-oxide CG FET than the thin-oxide CG FET. But, examining the maximum available gain (MAG) of the cascode amplifier, neutralizing the inter-stage capacitances can surprisingly mitigate the effect of the cut-off frequency of the CG FET on the MAG.

Figure 1a shows the hetero-stacked cascode power amplifier with a shunt inductor neutralization. The MAG of the neutralized cascode cell can be derived based on the small signal equivalent half circuit of the cascode cell shown in Figure 1b. The value of L_{neu} for compensating C_{gs2} is determined by the resonance condition. For the differential amplifier design in mm-wave range, the stability of the common source (CS) FET is enforced by using the cross-coupled capacitor C_{neu}, which achieves infinite isolation between the input and output of the CS FET as in [4]. Assuming the perfect neutralization as explained in [4], we simplified the analysis to calculate the MAG of the cascode cell ignoring C_{gd1}. At first, the available source power (P_{avs}) is given by (Equation (1)).

$$P_{avs} = \frac{I_g{}^2 R_{g1}}{2} \tag{1}$$

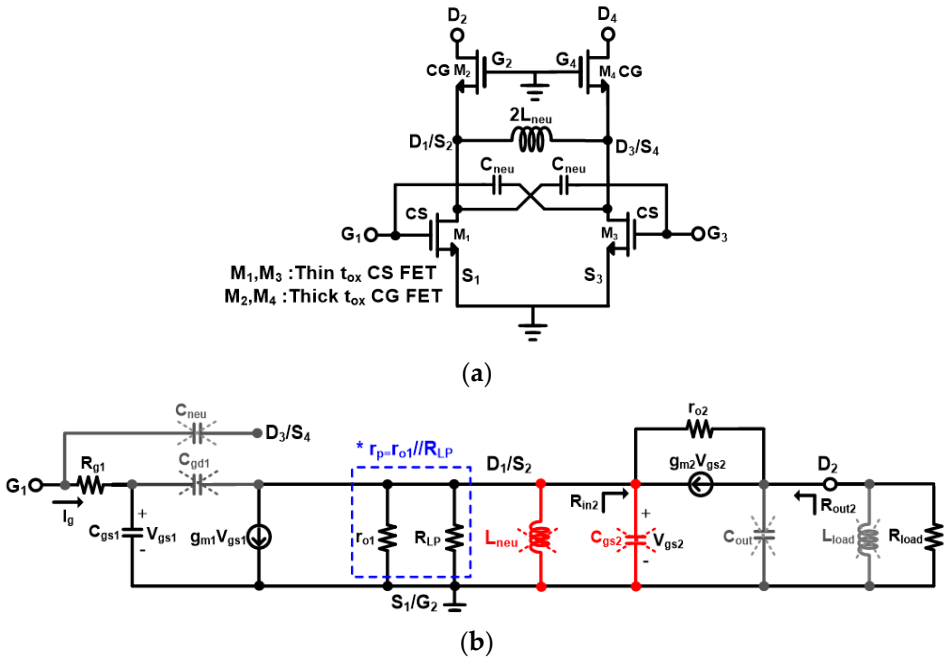

Figure 1. Hetero-stacked cascode power amplifier with a shunt inductor neutralization. The resistance R_{LP} is a parallel equivalent resistance of the inductor L_{neu} at the neutralizing frequency. (**a**) Simple differential hetero-stacked cascode cell schematic. (**b**) Small signal equivalent half circuit.

Assuming the shunt neutralization at the input of the CG FET, the output resistance of the cascode cell is given by (Equation (2)) [5]. Under the conjugate matching condition at the output, the input resistance R_{in2} of the CG FET is determined by (Equation (3)) as explained in [5].

$$R_{out2} = (r_{o2} + r_p(1 + g_{m2}r_{o2})) \approx g_{m2}r_p r_{o2} \tag{2}$$

$$R_{in2} = \frac{r_{o2} + R_{out2}/2}{1 + g_{m2}r_{o2}} = \frac{r_{o2}}{1 + g_{m2}r_{o2}} + \frac{r_p}{2} \approx \frac{1}{g_{m2}} + \frac{r_p}{2} \tag{3}$$

In (Equations (2) and (3)), the resistance r_p is a parallel equivalent resistance combining r_{o1} and R_{LP}. Then the available output power (P_{avo}) is given by (Equation (4)). The input current of the CG FET from the output current of the CS FET can be determined by current division between R_{in2} and r_p. Additionally, the output resistance R_{out2} and the load resistance R_{load} equally share the output current of the cascode cell under conjugate matching condition, a half of the output current of CG FET is delivered to R_{load}. In (Equation (5)), the P_{avo} is expressed in terms of the input current instead of the voltage V_{gs1} since the available source power is expressed using the input current I_g. The P_{avo} in (Equation (6)) is obtained by using (Equations (2) and (3)) for R_{out2} and R_{in2} in (Equation (5)) at the neutralizing frequency f_0.

$$P_{avo} = \frac{1}{2}\left(\frac{1}{2}g_{m1}V_{gs1}\frac{r_p}{R_{in2}+r_p}\right)^2 R_{out2} \tag{4}$$

$$= \frac{1}{8}\left(\frac{g_{m1}I_g}{2\pi f_0 C_{gs1}}\frac{r_p}{R_{in2}+r_p}\right)^2 R_{out2} \tag{5}$$

$$= \frac{1}{2}{I_g}^2\left(\frac{f_{t1}}{f_0}\right)^2\frac{{g_{m2}}^3{r_p}^3 r_{o2}}{\left(2+3g_{m2}r_p\right)^2} \tag{6}$$

Introducing the quality factor Q_{int} (=$2\pi f_0 C_{gs2} r_p$) at the inter-stage node excluding R_{in2}, the final P_{avo} is obtained as follows.

$$P_{avo} = \frac{1}{2}{I_g}^2\left(\frac{f_{t1}}{f_0}\right)^2\left(\frac{Q_{\mathrm{int}}f_{t2}}{f_0}\right)^3\frac{r_{o2}}{\left(2+3Q_{\mathrm{int}}(f_{t2}/f_0)\right)^2} \tag{7}$$

In (Equation (7)), f_{t1} and f_{t2} are cut-off frequencies of CS and CG FET given by $g_{m1}/2\pi C_{gs1}$ and $g_{m2}/2\pi C_{gs2}$, respectively. The final P_{avo} (Equation (7)) is expressed using the cut-off frequency of FETs and neutralization frequency to evaluate and compare the effect of neutralization in terms of the cut-off frequency of the CG FET.

The resistance R_{LP} is a parallel equivalent resistance of the neutralizing inductor L_{neu} given by

$$R_{LP} = R_{LS}(1+{Q_L}^2) = \frac{2\pi f_0 L_{neu}}{Q_L}\left(1+{Q_L}^2\right) \approx \frac{Q_L}{2\pi f_0 C_{gs2}} \tag{8}$$

where Q_L is the quality factor of the neutralizing inductor. As seen in (Equation (8)), R_{LP} decreases as the operation frequency increases, considering that the available maximum Q factor of the inductor in CMOS process is limited. Finally, *MAG* is obtained as the ratio of P_{avo} and P_{avs} as follows.

$$MAG = \left(\frac{f_{t1}}{f_0}\right)^2\left(\frac{Q_{\mathrm{int}}f_{t2}}{f_0}\right)^3\frac{r_{o2}/R_{g1}}{\left(2+3Q_{\mathrm{int}}(f_{t2}/f_0)\right)^2} \tag{9}$$

When the operation frequency satisfies the following condition,

$$f_0 << Q_{\mathrm{int}}f_{t2} \tag{10}$$

The *MAG* at the neutralizing frequency can be approximated as (Equation (11)).

$$MAG \approx \left(\frac{f_{t1}}{f_0}\right)^2\left(\frac{Q_{\mathrm{int}}f_{t2}}{f_0}\right)\frac{r_{o2}}{9R_{g1}} \tag{11}$$

The result of (Equation (11)) implies that the *MAG* of the neutralized cascode cell is linearly proportional to f_{t2}, unlike the quadratic dependence on f_{t1} of the CS FET. This behaviour is valid regardless of the gate lengths of CG FETs. It means that the effect of f_{t2} on the total gain of the cascode cell appears relatively smaller than f_{t1}. Especially, the

high output resistance of the thick-oxide CG FET additionally compensates the low cut-off frequency of its own. Since the cut-off frequency and the output resistance of CMOS FET are inversely and proportionally dependent on the gate length, the overall gain of the cascode cell using the thick-oxide CG stage is almost comparable to that using all thin-oxide FETs around the neutralizing frequency while the condition (Equation (10)) holds. In fact, the node Q factor Q_{int} initially increases with neutralizing frequency because the resistance r_p is dominated by r_{o1} at low frequencies. However, as the frequency goes high, the resistance r_p gradually decreases with the neutralizing frequency due to the relation (Equation (8)). Therefore, Q_{int} eventually saturates to the constant value and gain compensation by neutralization is relaxed.

The MAGs of two cascode cells based on (Equation (9)) are compared in Figure 2 as a function of the neutralizing frequency using extracted equivalent circuit parameters of two cascode cells using the same widths for CS/CG FETs and bias current conditions. In the relatively low frequency, the hetero-stacked cascode cell shows the higher gain up to 1.7 dB compared to the normal cascode cell because of the sufficient compensation by the Q_{int} and high output resistance of thick-oxide CG FET. As neutralization frequency increases, the MAGs become similar and finally the normal cascode cell shows a higher gain above 90 GHz.

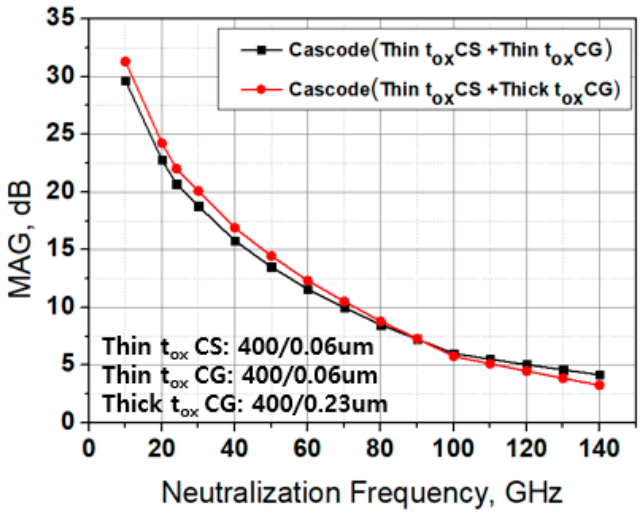

Figure 2. Calculated MAG using extracted equivalent circuit parameters according to the neutralization frequency (thin-oxide FET CS + thin/thick-oxide FET CG).

3. MAG Simulation Verification

Figure 3 shows the schematic of the proposed differential hetero-stacked cascode power amplifier composed of the thin-oxide common source (CS) field effect transistor (FET), thick-oxide common gate (CG) FET, and neutralization inductor L_{neu}. The differential architecture is chosen for easy neutralization compared to the single-ended structure and an additional capacitive neutralization for the CS stage.

According to the accurate simulation, the hetero-stacked cascode cell without neutralization shows the higher gain below 19 GHz because of the higher output resistance of the thick-oxide CG FET, and the inter-stage pole is negligible at low frequencies as shown in Figure 4a. However, the maximum available gain (MAG) of the hetero-stacked cascode cell without inductive neutralization is lower than that of the normal cascode cell by 3.5 dB at 24 GHz. Adopting neutralization at 24 GHz for both cascode cells, the hetero-stacked cascode shows the higher MAG up to 34 GHz and 1.5 dB higher MAG than normal cascode cell at 24 GHz as shown in Figure 4b.

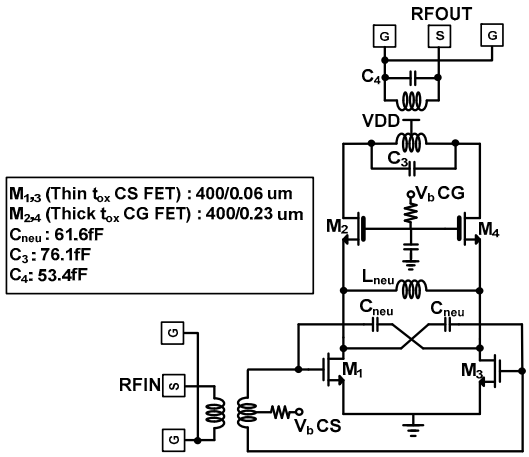

Figure 3. Schematic of the proposed hetero-stacked cascode power amplifier.

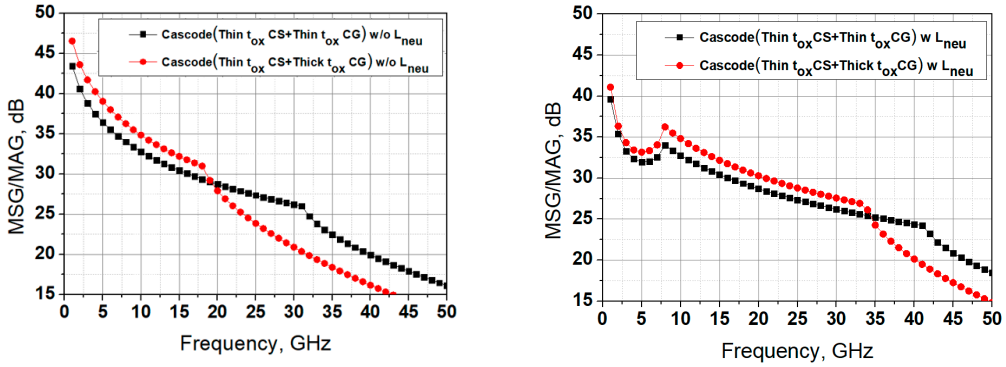

Figure 4. Simulated MSG/MAG of the cascode cells (thin-oxide FET CS + thin/thick-oxide FET CG). (**a**) Without L neutralization. (**b**) With L neutralization at 24 GHz.

Figure 5 shows the simulation results of the MAGs when neutralization is performed at every frequency to confirm the previous analysis. Results of Figure 5 consider all parasitics of passive networks using full-wave electromagnetic simulation. Increasing neutralization frequency by reducing the value of L_{neu} of the same component Q_L-value, the gain cross-over frequency is found to be approximately 60 GHz, which is slightly lower than the predicted in Figure 2. It is because the simple small signal model presented by Figure 1b ignores additional parasitic capacitances of the real cascode cells. However, surprisingly, the hetero-stacked cascode cell shows the higher gain than the normal cascode cell even beyond the cut-off frequency about 40 GHz of the thick-oxide CG FET. This result shows that the low cut-off frequency of thick-oxide FET is compensated by its high output resistance.

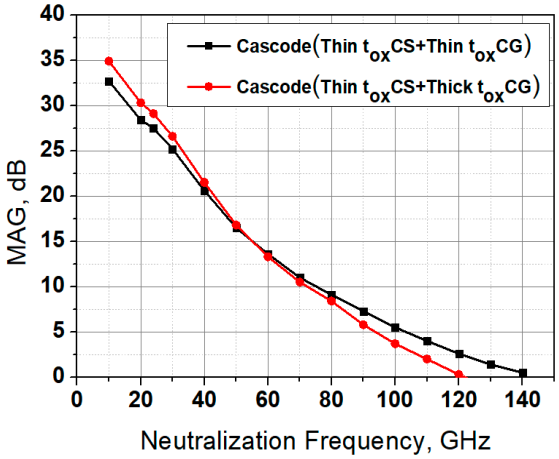

Figure 5. Simulated MAG according to neutralization frequency (thin-oxide FET CS + thin/thick-oxide FET CG).

4. Measurement Results

The chip microphotograph is shown in Figure 6. The chip size is 0.7 × 0.63 mm^2 including all pads. The proposed PA is fabricated using 65-nm low power (LP) CMOS technology with 0.57 mA/um current density and 1-poly 8-metal layers. The supply voltage is 3.7 V and DC power dissipation is 466 mW under quiescent condition.

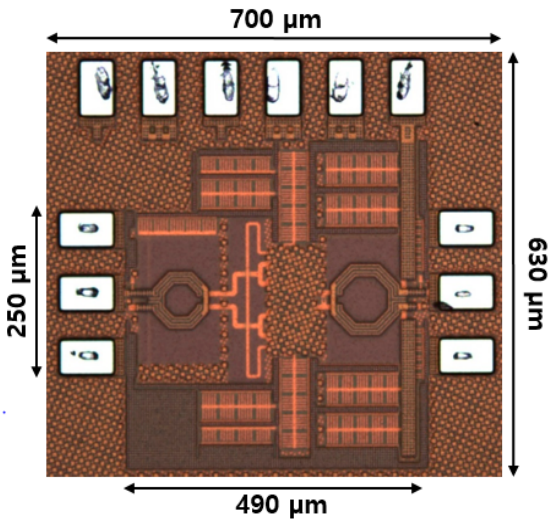

Figure 6. Chip microphotograph.

Measured and simulated S-parameters are plotted in Figure 7a. The measured small signal gain is 14.6 dB and the input return loss is −9.4 dB for 24 GHz. Figure 7b shows the measured power gain, output power, and power added efficiency (PAE) of the proposed PA with a 24 GHz 1-tone continuous wave (CW) signal. The large signal measurement results demonstrate 15.4 dB gain, saturated output power of 23.3 dBm, output 1-dB compression point of 20.8 dBm, and peak PAE of 31.3% at 24 GHz. The large signal performance versus different frequencies is shown in Figure 7c from 22 GHz to 28 GHz.

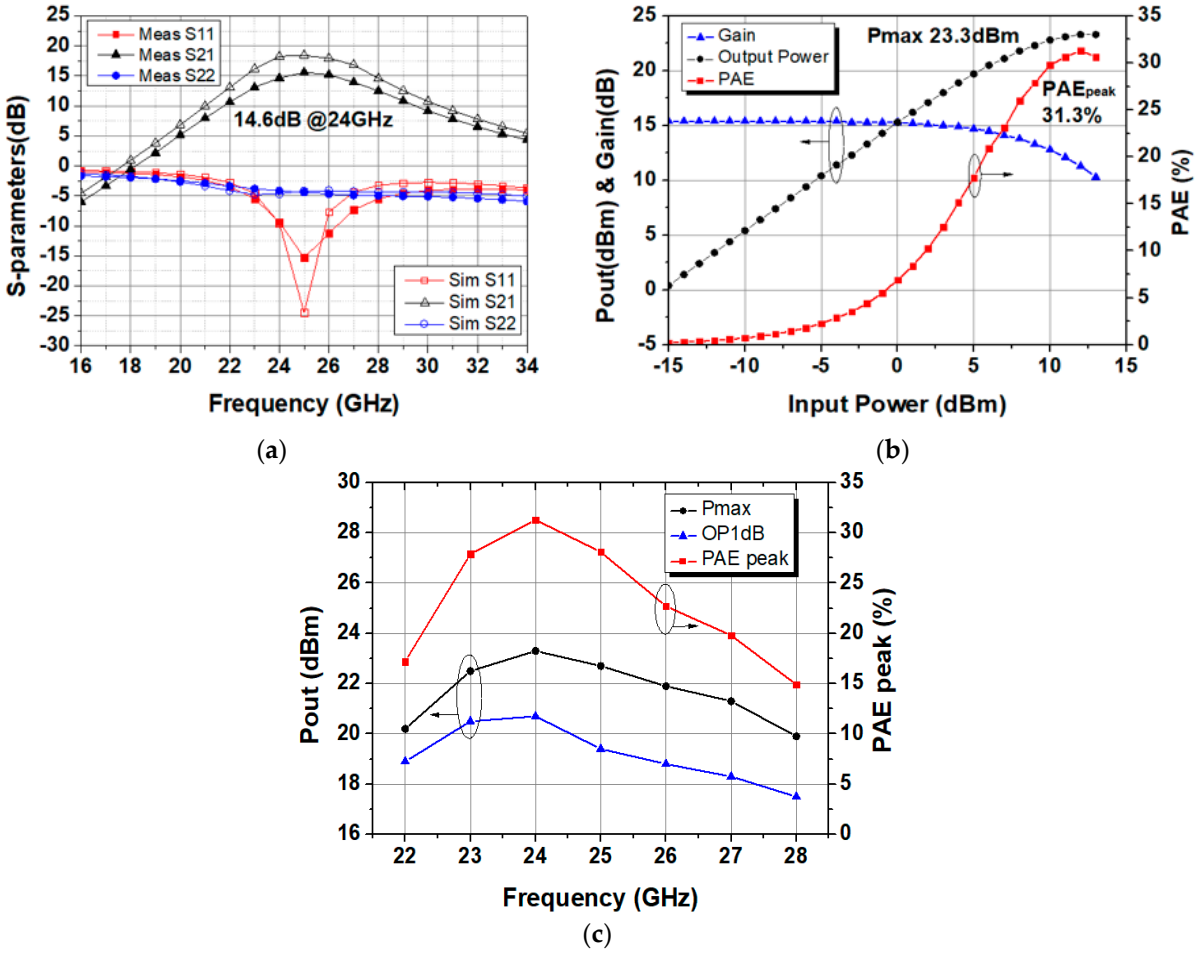

Figure 7. Measurement results of the proposed PA. (**a**) Measured and simulated S-parameters. (**b**) Measured large-signal characteristics with 1-tone signal at 24 GHz. (**c**) Measured large-signal characteristics vs. frequency of proposed PA.

Performance comparison with recent state-of-art K-band CMOS PAs is shown in Table 1.

Table 1. Performance comparison table.

Ref	Process	Freq. (GHz)	Gain (dB)	P_{sat} (dBm)	PAE_{peak} (%)	OP_{1dB} (dBm)	Structure	Power Combining	P.D. * (mW/mm^2)
[6]	90 nm CMOS	24	17.4	25.6	32.8	23.6	1-stage Cascode	2-way	905.4 **
[7]	40 nm CMOS	27	22.4	15.1	33.7	13.7	3-stage (Cascode + CS)	1	140.7
[8]	90 nm CMOS	21	26.9	20.4	17.3	18.5	2-stage Cascode	1	148.2 **
[9]	65 nm CMOS	23.5	10.2	26.1	19.3	23.9	1-stage Cascode	4-way	636.5 **
[10]	90 nm CMOS	24	14.1	24.4	28	21.7	1-stage Cascode	2-way	523.6 **
[11]	90 nm CMOS	24	11.5	21.7	16.7	18.9	1-stage Stacked	2-way	547.8 **
[12]	65 nm CMOS	24	9.1	14.7	42.6	13.9	1-Stage CS	1	268.3
This work	65 nm LP CMOS	24	15.4	23.3	31.3	20.8	1-stage Cascode	1	1745.3

* Power density is denoted as P.D. (P_{sat}/chip area); ** With pads.

Though the higher output powers were reported in [6,9,10], they were obtained utilizing the parallel power combining techniques for unit amplifiers. Since the proposed hetero-stacked cascode power amplifier only used a unit amplifier and N-way combining can be used for more output power.

5. Conclusions

In this paper, a K-band hetero-stacked cascode CMOS PA with high saturated output power and efficiency is presented. The PA is fabricated in 65-nm low power (LP) CMOS process stacking the thin-oxide field effect transistor (FET) and thick-oxide FET for cascode configuration with neutralization. The hetero-stacked cascode structure can enhance the output power by using a high supply voltage compared to the normal cascode structure. But using a hetero-stacked cascode in the mm-wave range, the high frequency gain degradation occurs due to low cut-off frequency of the thick-oxide common gate (CG) FET. If the inductive neutralization is applied to the inter-stage of the hetero-stacked cascode cell as used in this work, the high frequency gain degradation can be compensated by high output resistance of the thick-oxide CG FET. Additionally, this work analyses the effect of inter-stage neutralization on the gain improvement of the cascode cell. The analysis shows that the proposed cascode amplifier provides a comparable gain to the normal cascode amplifier near the cut-off frequency of the thick-oxide CG FET. The proposed cascode structure is advantageous to easily enhance the output power without gain degradation and complicated power combining techniques in the mm-wave range.

Author Contributions: Conceptualization, K.-J.C. and B.-S.K.; methodology, S.-K.K.; software, J.-H.P.; validation, K.-J.C. and S.-K.K.; formal analysis, K.-J.C., J.-H.P., and B.-S.K.; investigation, K.-J.C.; resources, J.-H.P.; data curation, K.-J.C. and B.-S.K.; writing—original draft preparation, K.-J.C.; writing—review and editing, K.-J.C. and B.-S.K.; visualization, B.-S.K.; supervision, B.-S.K.; project administration, B.-S.K.; funding acquisition, B.-S.K. All authors have read and agreed to the published version of the manuscript.

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