Article

Power Conversion Using Analytical Model of Cockcroft–Walton Voltage Multiplier Rectenna

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Abstract: A voltage multiplier rectenna is a combination of a voltage multiplier rectifier and an antenna used for the conversion of AC to DC. It is an essential part of the system of RF energy harvesting. Conventional rectennas are characterized by low conversion efficiency. This study presents an analytical novel mode designed for RF energy harvesting systems to study the voltage and current output of rectifier stages for efficiency optimization. The design contains a voltage multiplier rectification circuit with seven stages. The Schottky diode HSMS 285-C was selected for the circuit modeling voltage multiplier circuit. Advanced Design System (ADS) simulation was used to validate the equations of the theoretical model solved with MATLAB code. The fabricated system was tested for an input power range of 10 μ W to 100 mW; the maximum output power is 0.2577 mW with maximum efficiency of 29.85%.

Keywords: AC–DC power converter; Cockcroft–Walton; rectenna; rectifier; RF energy harvesting; voltage multiplier

1. Introduction

Wireless communication has been growing rapidly over the last few years and has become an essential part of people's daily lives. The importance of wireless communication lies in enabling users to be connected anywhere at any time. However, wireless networks are also known to emit a large amount of electromagnetic energy. Most recent works are trying to use this energy [1,2]. The radio frequency (RF) harvesting system is a basic unit in wireless power transmission [3–6]. The scientific and technological advancements associated with the use of RF energy harvesting technology has become more effective. There are different external ambient RF energy sources in this modern technology, with different resonance frequencies radiating RF signals in all directions. Some of those sources are television (TV), radio broadcast, mobile phone stations, cellular phones, and wireless local area network transceivers (LAN) [7]. RF energy harvesting system focuses on the continuous assembling of RF energy from ambient sources to provide necessary DC power to low-power devices [8]. RF harvesting system consists of a receiving circuit that receives the RF signal and converts it back to a DC signal. Rectennas are used as receivers in the RF harvesting system [9] by converting RF power, P_{RF} into DC power, P_{DC} at a certain

frequency. The energy harvesting design has been proposed [10], as illustrated in Figure 1, which shows the schematic diagram of 43 RF energy harvester. This shows the connection of the antenna to an LC matching circuit, which is connected to a voltage multiplier rectifier. The antenna comprises a voltage source (V_a), a radiation resistance (R_a), which produces an antenna current I_a . The LC impedance matching is located between the antenna and the rectifier. The impedance matching circuit contains passive elements such as capacitive or inductive reactance. The matching network results in a current, I_L which passes through the resistance of voltage multiplier rectifier (R_L) resultant in voltage (V_L). The function of matching circuit is ensuring that maximum power is transferred from the antenna to the rectifier circuit. In the absence of the matching circuit, the RF power captured by the harvester antenna will be reflected, thus little power is realized at the rectifier. Several factors affect the efficiency of the RF harvesting system, these factors include [11]: The antenna's efficiency, where the gain becomes smaller with decrease in size, and the power efficiency of voltage multiplier. The RF to DC conversion efficiency is described as the ratio of the DC output power (P_{out}) to the RF input power (P_{in}), where RF power is the power received by the antenna, and the DC power is the output power between terminals of the load resistor which is attached to the output of voltage multiplier. Where RF power is the power received by the antenna, and the DC power is the output power calculated between terminals of the load resistor attached to the output of voltage multiplier. The voltage multiplier (η) conversion efficiency can be found in (1):

$$\eta = \frac{\text{DC output power } (P_{out})}{\text{RF input power } (P_{in})} \quad (1)$$

where P_{RF} is the RF input power in the rectifying circuit. Reflected RF power is the dissipated power between the source and the voltage multiplier. Thus, some rectennas have low-efficiency (<15%) due to the small output power P_{out} produced by the rectifier. An analytical model to study the relations of the output voltage and current during different modes produced a good performance with good accuracy [12–16]. The parameters were designed without detaching the parasitic effects; consequently, the quantitative effect in the parasitic elements on the wireless RF harvester was not studied. This study presented the quantifiable effect of the rectifier elements on the performance of RF energy harvesters, with the effect of components which are used for impedance matching network. By studying the matching circuit quantitatively, the effect of each element on the performance of the harvester circuits tuned to improve the efficiency of the RF energy harvesting circuit. However, the model assumes steady-state conditions. To demonstrate the design, a harmonic simulation is used, besides a physical model fabrication. The key contribution in this paper is the design of an improved Cockcroft–Walton voltage multiplier rectifier based on an analytical model that can be used for power conversion applications. Further studies have been conducted on the voltage multiplier rectifier circuit by various authors [17–27].

Figure 1. Schematic diagram of receiving rectenna.

2. Methodology of Designing the Rectenna

2.1. Linearized Analysis of Voltage Multiplier

The analytical model of a rectifying antenna is based on the linearization concept. The accurate techniques for determining the output results of rectifying circuits were given by the design. Figure 2 shows an RF harvester realized at 930 MHz by [28]. V_S is the input voltage, R_A is the antenna resistance, and R_L is the load. After designing the linearized circuit as in Figure 2, the value of the output voltage V_L is calculated using nodal analysis. The voltages at node V_{IN} , V_D and V_L , are as shown in Figure 3.

Figure 2. Radio frequency (RF) harvesting system using an HSMS-285C at 930 MHz [28].

Figure 3. A linearized model of the RF power harvester.

2.2. Analytical Model of Cockcroft–Walton Voltage Multiplier Rectenna

Design consideration of the rectifying antenna is illustrated in this section for Cockcroft–Walton voltage multiplier circuit, as shown in Figure 4. The capacitor and resistor load values were calculated using the tuning tool in ADS software, as shown in Figure 4. The values of capacitors are selected based on the frequency value. The values of the L-network can be calculated using the Smith chart tool in ADS software.

Figure 4. Tuning tool for finding values of capacitors in the voltage multiplier rectifier circuit.

The network schematic in Figure 5 shows the parameters of the matching network, where Z_s is the impedance of the antenna, which is 50Ω . Since the rectifier is a nonlinear circuit and its impedance value changes as a function of frequency and input power level, an input power value of 10 dBm was chosen since it has the best efficiency for seven stages, as stated in [29]. The network response was displayed by simulated real (red line) and imaginary (blue line) parts of the input impedance as a function of frequency. A matching network was designed to transform the impedance of the antenna (50Ω) to the impedance of the voltage multiplier. The matching network consists of 8.33 nH and a 1.135 pF for inductor and capacitor, respectively. The capacitor was placed in parallel with the ports of the antenna, while the inductor was placed in series with the voltage multiplier. From the response of the network shown in Figure 5, it is clear that the proposed matching circuit will match the voltage multiplier impedance with the source at 900 MHz.

Figure 5. Smith chart utility for finding elements of the matching circuit.

The design parameters for the proposed design are summarized in Table 1.

Table 1. Design parameters of the design for $f_r = 900$ MHz.

Design Parameters	Cockcroft–Walton Voltage Multiplier Circuit
Matching circuit parameters	$L = 8.33$ nH $C = 1.135$ pF
The used diodes	Seven Schottky diodes of HSMS-285C
Number of capacitors	15 capacitors
Arrangement of capacitors	The capacitors and diodes are arranged in series

The original circuit, as shown in Figure 6, consists of the antenna, impedance matching and voltage multiplier. The main reason for choosing 7 stages of voltage multiplier is that the parasitic effect of the capacitor of each stage was increased, which accumulates and leads to a decrease in voltage gain [30–32]. The circuit was converted to a linearized circuit by replacing the diodes, the capacitor and inductor with their impedances, as shown in Figure 7. In general, the diode impedance is R_D , capacitor impedance is $-jXC$, and inductor impedance is jXL . $X_{C1} - X_{C14}$ are the reactance with a value of 0.3 pF. X_{CL} is the reactance with a value of 100 pF load capacitor. R_L is the load resistance of the voltage multiplier [20].

Figure 6. Rectenna design parameters in Cockcroft–Walton voltage multiplier circuit.

Figure 7. Linearized model of Cockcroft–Walton voltage rectenna.

To simplify the circuit and obtain the values of the output voltage and current (V_{out}) and (I_{out}), respectively, the circuit was divided into two modes, in which mode 1 and mode 2 were the negative and positives peaks, respectively.

- (1) **MODE 1:** During the negative half cycle of the first stage, when the first diode, D_1 , is ON state, the I_{d1} will pass through the diode D_1 . D_2 is OFF at this stage, and the circuit behaves as an OPEN circuit. While in the second stage, D_1 and D_3 are in the ON state, while D_2 and D_4 are turned off. During stage three, D_1 , D_3 and D_5 are turned to the ON state, while D_2 , D_4 and D_6 are turned OFF. Until stage seven, “ D_1 , D_3 , D_5 , D_7 , D_9 , D_{11} and D_{13} ” are turned ON, while “ D_2 , D_4 , D_6 , D_8 , D_{10} , D_{12} and D_{14} ” are turned OFF. Mode 1 is illustrated in Figure 9.
- (2) **MODE 2:** The same procedure is described in mode 2 since it represents the positive half cycle of the circuit. During the first stage, D_2 is in the ON state while D_1 is in the OFF state (the circuit is OPEN, and the diode D_1 is OFF). During the second stage, D_2 and D_4 are turned ON while D_1 and D_3 are turned OFF. Until stage seven, “ D_2 , D_4 , D_6 , D_8 , D_{10} , D_{12} and D_{14} ” are turned ON and “ D_1 , D_3 , D_5 , D_7 , D_9 , D_{11} and D_{13} ” are turned OFF. Mode 2 is represented in Figure 8.

The output voltage for each stage can be found during the positive peak mode when the diodes (D_2 – D_{14}) are ON since the output voltage for each stage can be found at the end of each stage. An equation was derived for each stage, which results in a total of seven equations. As shown in Figure 10, the nodes “ V_2 , V_4 , V_6 , V_8 , V_{10} , V_{12} , and V_{14} ” refer to the output voltage for stages 1, 2, 3, 4, 5, 6 and 7, respectively. Noting that V_{14} represents the output voltage of the circuit.

Figure 8. The linearized design of Cockcroft–Walton during positive peak.

Figure 9. The linearized design of Cockcroft–Walton during negative peak.

Figure 10. Verification result for the mathematical expression of Cockcroft–Walton voltage multiplier using MATLAB.

For linear circuit elements, the rule is $V = I \times Z$, where V , I and Z are all complex variables. Impedances are added in series and in parallel in the same way as resistors, i.e., $Z_{series} = Z_1 + Z_2$, $Z_{parallel} = Z_1 || Z_2 = (Z_1 \times Z_2) \div (Z_1 + Z_2)$

By applying Kirchhoff voltage law (KVL) and Kirchhoff current law (KCL) on the seven stages, Equations (2)–(8) were derived.

$$V_2 = V_s + I_s(-jX_c + Z_D) \quad (2)$$

$$V_4 = \frac{V_2(-jX_c + Z_D) + jX_c V_1}{Z_D} \quad (3)$$

$$V_6 = \frac{V_4(-jX_c + Z_D) + jX_c V_3}{Z_D} \quad (4)$$

$$V_8 = \frac{V_6(-jX_c + Z_D) + jX_c V_5}{Z_D} \quad (5)$$

$$V_{10} = \frac{V_8(-jX_c + Z_D) + jX_c V_7}{Z_D} \quad (6)$$

$$V_{12} = \frac{V_{10}(-jX_c + Z_D) + jX_c V_9}{Z_D} \quad (7)$$

$$V_{14} = \frac{V_{12}(-jX_c + Z_D) + jX_c V_{11}}{Z_D} \quad (8)$$

where V_s is the voltage source with a value of 0.762 V at 10 dBm.

jX_L is the inductor impedance; its value is equal to $2\pi fL \Omega$;

jX_C is the capacitor impedance; its value is equal to $1/(2\pi fC) \Omega$;

Z_D is the impedance of the diode represented in the model by R_D and $-jX_D$; its value can be calculated using equations of diodes' impedance.

The same principle applies to the values of the nodes output voltages for stages 1–7 in the first mode (V_1 – V_{13}), as shown in Equations (9)–(15):

$$V_1 = V_s + I_s(Z_D) \quad (9)$$

$$V_3 = \frac{V_1(-jX_c + Z_D) + jX_c V_s}{Z_D} \quad (10)$$

$$V_5 = \frac{V_3(-jX_c + Z_D) + jX_c V_2}{Z_D} \quad (11)$$

$$V_7 = \frac{V_5(-jX_c + Z_D) + jX_c V_4}{Z_D} \quad (12)$$

$$V_9 = \frac{V_7(-jX_c + Z_D) + jX_c V_6}{Z_D} \quad (13)$$

$$V_{11} = \frac{V_9(-jX_c + Z_D) + jX_c V_8}{Z_D} \quad (14)$$

$$V_{13} = \frac{V_{11}(-jX_c + Z_D) + jX_c V_{10}}{Z_D} \quad (15)$$

Based on the previous equations, a general rule for n stages can be found from Equations (2)–(15);

$$V_n = \frac{V_{(2n-2)}(-jX_c + Z_D) + jX_c V_{(2n-3)}}{Z_D} \quad (16)$$

The output current for any stage (I_n) can be found based on Equation (17);

$$I_n = \frac{V_n}{R_n} \quad (17)$$

where R_n is the load resistance. An increase in the number of stages will result in an increase in the value of the output voltage and a decrease in the value of the output current at the same time. For the mathematical expression of Cockcroft–Walton voltage Equations (2)–(15) were used for the simulation using MATLAB code as shown in Figure 10. The equations were written in MATLAB with input parameters for capacitors, frequency, Z_D , jXL , jXC , input voltage and current V_s , I_s , respectively. Values of V_1 to V_7 were obtained using Equations (9)–(15). The value of the output voltage is 1.50 V, and the value of output power is 57.1 μ W for a load of resistance 50 K Ω . For the proposed circuit, the seven stages model has the best performance since it has a high ability to give the best output voltage. For the proposed design at the frequency of 900 MHz, the output voltage deteriorated after stage seven, as previously mentioned in earlier studies [32]. The reason for this trend is the increasing parasitic effect of the capacitors in each stage, which accumulates and leads to decreasing voltage gain [33].

3. Simulation Results of Cockcroft–Walton Multiplier Voltage Rectifier

HSMS-285x was selected because it has the largest efficiencies at the lowest powers due to its low turn-on voltage. The arrangement of the capacitors is in series with diodes. For rectified voltage applications, seven stages circuit has the best performance; for the frequency of 900 MHz, the output voltage declined from the seventh stage that was observed in recent works. The reason for this voltage deterioration is the increasing parasitic effect of the capacitors of each stage, which results in a decrease in the voltage gain.

Figure 11 shows the circuit design of the seven stages Cockcroft–Walton voltage multiplier rectenna. The circuit consists of an antenna (that generates a signal at 900 MHz), which is represented with an AC source in ADS, seven stages of rectifier circuit and load circuit.

Figure 11. Simulation of the proposed design using Advanced Design System (ADS) software.

Figure 12 illustrates the simulation results for the proposed design before and after adding the matching network. The value of the input voltage (V_{in}) is 0.762 V, and the output voltage before adding matching circuit is 2.384 V. The value of the output voltage after adding the matching network is 4.629 V. It was observed that the output is not accurately DC voltage; it is mostly an AC signal with a DC offset voltage. The increase in the output voltage is due to the addition of a matching circuit that operates as a detector for the circuit to confirm a good transformation of the power from the antenna to voltage multiplier.

The function of the voltage multiplier rectifier circuit is to increase the output voltage value, as shown in Figure 12. While in Figure 13, it is observed that the output current decreases after seven stages (with a value of 1.468×10^{-3} mA) before adding the matching network. The output current increased after adding the matching circuit due to the decrease of the dissipated output power as a result of the influence of the matching circuit.

Figure 14 illustrates that at 900 MHz, the input power rises to 64.8 μ Watt, which is the power received by the antenna. It also observed that the output power decreased after the seventh stage to 1.7 μ Watt. The dissipated power will increase by increasing the number of stages and elements. Using a matching circuit will increase the value of power to 29 μ Watt, which is a positive indicator of the importance of adding the matching circuit to increase

the efficiency of the voltage multiplier by decreasing the dissipated power as illustrated as well in [34,35].

Figure 12. Output voltage of Cockcroft-Walton voltage multiplier circuit.

Figure 13. Current results of Cockcroft-Walton voltage multiplier circuit.

Figure 14. Power results of Cockcroft-Walton voltage multiplier circuit.

Figure 15 shows the result of the simulation for the output voltage for stages V_{in} – V_7 .

These results clearly show that there is an increase in the value of the V_{out} for every stage until the eighth stage, where the output voltage is almost the same due to the parasitic effect of the constituent capacitors of each stage. This trend continues until the increment becomes negligible. The results for Cockcroft–Walton voltage multiplier are presented in Table 2. It is observed that the output power increased for all the power input values. Based on equation 18, the output current increased, leading to an increment in the ripple voltage:

$$V_{ripple} = \frac{I_o \times \left(N^2 + \frac{N}{2}\right)}{8fC} \quad (18)$$

where I_o is the output current, N is the number of voltage multiplier stages, f is the resonance frequency, and C is the value of the capacitor. As a smaller ripple voltage is preferable, a smaller output current ensures that the output voltage signal is closer to the DC line.

Figure 15. Output voltages with the number of stages of Cockcroft–Walton rectenna.

Table 2. The simulated results for Cockcroft–Walton voltage multiplier circuit.

Pin (dBm)	Input Power (Watt)	Output Voltage (V)	Output Current (A)	Output Power (Watt)	Ripple Voltage (V)
−20	8.42×10^{-7}	0.248	1.290×10^{-7}	1.59×10^{-8}	4.703×10^{-6}
−15	6.95×10^{-7}	0.334	1.437×10^{-7}	2.39×10^{-8}	5.239×10^{-6}
−10	2.37×10^{-6}	0.448	4.241×10^{-7}	9.49×10^{-8}	1.546×10^{-5}
−5	7.67×10^{-6}	0.691	1.259×10^{-6}	4.35×10^{-7}	4.590×10^{-5}
0	1.65×10^{-5}	0.879	6.712×10^{-6}	2.95×10^{-6}	2.447×10^{-5}
5	4.49×10^{-5}	2.51	1.116×10^{-5}	1.40×10^{-5}	4.069×10^{-4}
10	6.48×10^{-5}	4.629	1.253×10^{-5}	2.90×10^{-5}	4.568×10^{-4}
15	9.71×10^{-4}	11.06	4.250×10^{-5}	2.35×10^{-4}	1.550×10^{-3}
20	4.22×10^{-3}	17.84	1.233×10^{-4}	1.09×10^{-3}	4.450×10^{-3}

4. Fabrication of Cockcroft–Walton Multiplier Voltage Rectifier

EAGLE software, which is a schematic software used for PCB design, was used to design the voltage multiplier rectifier circuits for the purpose of rectifier prototyping. Figure 16 shows the circuit schematic diagram with the computed distance between the voltage rectifier elements. The dimension of the Cockcroft–Walton rectifier circuit is 45×18 mm, as shown in Figure 17. The components of the circuit, such as the SMA connector, matching circuit, Schottky diodes, series capacitors and the output terminals, are highlighted in the diagram. Roger 5880 was chosen for ground plane prototyping

because of its advanced capabilities to boost the output voltage, as indicated by previous studies [22]. The mounting soldering technique was used to fix the elements of the voltage multiplier rectifier.

Figure 16. Schematic diagram of Cockcroft–Walton voltage multiplier rectifier designed with EA-GL software.

Figure 17. The fabricated Cockcroft–Walton voltage multiplier rectifier.

Figure 18 illustrates the testing setup for the proposed circuit. The circuit is connected to an RF signal generator, while its terminals are connected to the multimeter terminals to read the output values. The values of output voltage and current are 4.86 V and 68.73 μ A, respectively.

Figure 18. Testing and measurements setup for Cockcroft–Walton multiplier circuit.

5. Results and Discussion

The output voltage was investigated by carrying out an analysis of the power input for the proposed design using the input power ranging from -20 dBm to 20 dBm. The values of the analytical, simulated, and measured output voltages are presented in Figure 19 for the rectifier models at $10\text{ K}\Omega$ resistance load. As observed in the figure, the output power increased as the value of the input power increased.

Figure 19. Output voltage versus input power for Cockcroft-Walton voltage multiplier rectifier.

As clearly shown in Table 3, there is a good correlation between the analytical, simulation and experimental results of the prototype. The minor difference in the output values, 4.86%, 4.88% and 9.77% for voltage, current, and power, respectively, is due to the change in the input power of the rectifier during the testing process due to internal inductance and the voltage drop across diodes.

Table 3. Summarized results for Cockcroft-Walton voltage multiplier at 10 dBm.

Module	Analytical Results	Simulation Results	Experimental Results
Output voltage	4.051 V	4.629 V	4.860 V
Output current	69.31 μ A	65.46 μ A	68.73 μ A
Output power	0.2142 mW	0.242 mW	0.2362 mW

The effect of the matching circuit is illustrated to prove its ability to decrease the reflected power between the antenna and voltage multiplier rectifier by increasing the value of output power of the circuits at the range of input power. The output voltage increased by 64.02%. As the load resistance increases, the output DC voltage also increases. The rate of increase of the output voltage was higher at the lower value of resistance, as illustrated in [36]. Figure 20 shows the output voltage versus load resistance at 900 MHz. The efficiency is summarized in Figure 21 for power input range -20 to 20 dBm. Higher power input results in higher efficiency [17–21,23,24].

Figure 20. Simulated and measured output DC voltage versus the load resistance for the proposed design.

Figure 21. Efficiency curve of Cockcroft-Walton voltage multiplier.

Table 4 shows a comparison of this study with previous advanced research results that were conducted around 900 MHz frequency. The comparison is based on the circuit design and its output results. In [37], a six-stage Dickson multiplier was designed using Schottky diode to achieve a maximum output power of 50.28 mW, while a maximum output voltage of 1.6 V resulted in an efficiency of 54% by [38]. In [39,40], a good output was achieved, but the circuit's profile was large, while other studies achieved less output voltage and efficiency. Holistically, compared to other studies, the proposed rectenna displays superior output voltage, power, and efficiency with a smaller size.

Table 4. Comparison of related project's performance.

Ref.	Circuit Design	Output Voltage and Current	Power	Efficiency
[37]	Six stages voltage multiplier (Dickson) is combined with coupled square microstrip antenna	Output voltage of 2.78 V	Received power is 50.28 mW	-
[38]	Five stages voltage multiplier is combined with a T-shaped monopole antenna	The output voltage is 1.6 V	Input power density of 80 W/cm ²	Efficiency is 54%
[39]	Ten-stages voltage multiplier RF energy harvesting circuit	Output voltage range of 5–36.489 V	-	-
[41]	Nine stages of voltage doubler combined with matching circuit	Output voltage is 1.732 V, and output current is 0.1814 mA	Power level is 0.5206 dBm.	-
[42]	Seven-stage voltage doubler integrated with E-shaped microstrip antenna	Output voltage is 2.513 V, and output current is 25 μ A	-	-
[43]	Nine stages of Greinacher voltage double combined with matching circuit	Output voltage is 1.732 V, and output current is 0.1814 mA	-	-
[44]	RF energy harvester was designed by fine-tuning an L-matching network-	-	-	The circuit achieved maximum power efficiencies of 10.9%, 30.7%, and 55.2% for input powers of −30 dBm, −20 dBm and −10 dBm
[40]	Seven-stage rectifier. A Villard configuration is chosen based on HSMS 2850 Schottky diodes. The size has a large profile (190 × 33 mm)	Voltages of 9.17 V and 3.78 V are obtained at 900 MHz and 550 MHz	-	-
[35]	RF- DC circuit converter, which contains from 3 stages voltage multiplier (Dickson) based on HSMS 285	The design has an inductor in series with the input capacitance. The proposed design provides 19.43 μ W output power and around 1 V output voltage	-	-
[45]	Three-stage Dickson rectifier circuit with HSMS-285C Schottky diode.	Output voltage is 5.16 V	-	Maximum 77% efficiency
This work	A proposed voltage multiplier rectifier circuit is developed using Schottky diodes	The output voltage range is (0.756–17.58) V	The maximum output power is 0.2577 mW	Maximum efficiency is 29.85%

6. Conclusions

Since the effects of major parasitic elements on a wireless RF harvester performance are known, wireless RF harvesters capable of harvesting low ambient RF power levels can be realized. This study presents a novel analytical model for Cockcroft–Walton voltage multiplier for harvesting applications. The fabrication and testing of the complete RF energy harvesting system were discussed. The proposed design was tested at an input power level of −20 to 20 dBm with a resonance frequency of 900 MHz. A linearized mathematical model was also built for the voltage multiplier rectifier circuit. There is good agreement between the results of the developed mathematical expression and the simulation, indicating a good fit of the model. The minor difference between simulation and measurement results from the soldering effects when mounting the elements to the PCB and the nonlinearity characteristics of the diode. The results and discussion show that the designed rectifier circuit operates well at the targeted frequency and is suitable for use as an RF energy harvester.

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