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Review

Modulation Methods for Direct and Indirect Matrix Converters: A Review

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Abstract: Matrix converters (MCs) allow the implementation of single-stage AC/AC power conversion systems (PCS) with inherent bidirectional power flow capability. By avoiding the typical DC-link capacitor, MCs have the potential to achieve higher power density with a more reliable operation and less maintenance when compared with conventional two-stage AC/DC/AC PCS. For these reasons, matrix converters have been receiving significant attention from the academic sector but have not yet been implemented on a large industrial scale. This article reviews the Direct Matrix Converter (DMC) and the Indirect Matrix Converter (IMC) along with the respective actual and most important modulation methods. Simulation results are provided to validate the theoretical analysis and to get a deep insight about the implementation of space vector modulation (SVM) and respective switching pattern generator.

Keywords: matrix converter; AC/AC converter; power electronic converter; motor drive; space vector modulation; bidirectional switch; current commutation; soft switching; zero voltage switching; zero current switching

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1. Introduction

Matrix converters (MCs) are one of the most attractive families of converters in the power electronics field [1]. The matrix converter is a set of controlled bidirectional power switches that connects a voltage source directly to a load without using any DC-link or other energy storage element [2], and therefore it is called the "all-silicon" solution. The development of this converter started in 1980 with the research of Venturini and Alesina [3,4]. They were the first to use the label "matrix converter" and introduced the circuit arrangement including a detailed mathematical model to describe the low-frequency operation of the converter [5]. An extensive review of the milestones in research on matrix converters is presented in [6]. This converter has some very attractive characteristics [5,7]:

- high-power dense circuit,
- frequency decoupling between AC input and output voltage,
- input and output currents with sinusoidal waveform,
- full regenerative operation, and
- adjustable input power factor.

These characteristics are the reason for the present tremendous interest in matrix converters, as they allow obtaining a compact solution for a four-quadrant frequency converter [8–10]. As concluded in [11–13], the MC can achieve higher power densities when compared with equivalent two-stage power conversion solutions. Thus, it is expected that the application areas of the matrix converter are to be expanded, given its advantages of energy saving and size reduction [14]. Recently, several isolated AC-DC matrix converters [15] have been proposed for photovoltaic microinverters [16] and string inverters [17], battery energy storage systems (BESS) [10], on-board chargers (OBC) for electric vehicles (EVs) with vehicle-to-grid (V2G) functionality [18], power factor correction (PFC) rectifier

for data centers and telecommunication equipment [19], and uninterruptible power supply (UPS) [20]. However, the focus of this article will be on the non-isolated AC-AC matrix converter topologies and respective modulations.

Since the 1980s, several modulation methods were developed to control the matrix converter, also known as the Direct Matrix Converter (DMC). Therefore, in this work the Matrix Converter and the Direct Matrix Converter designations will be used indistinctly. More recently, the Indirect Matrix Converter (IMC) has been gaining recognition since maintaining the same input–output performance of the conventional matrix converter but with a simpler topology [9]. Figure 1 shows the landscaping of the main force-commutated three-phase AC-AC converters [2], where the DMC and the IMC are obviously included.

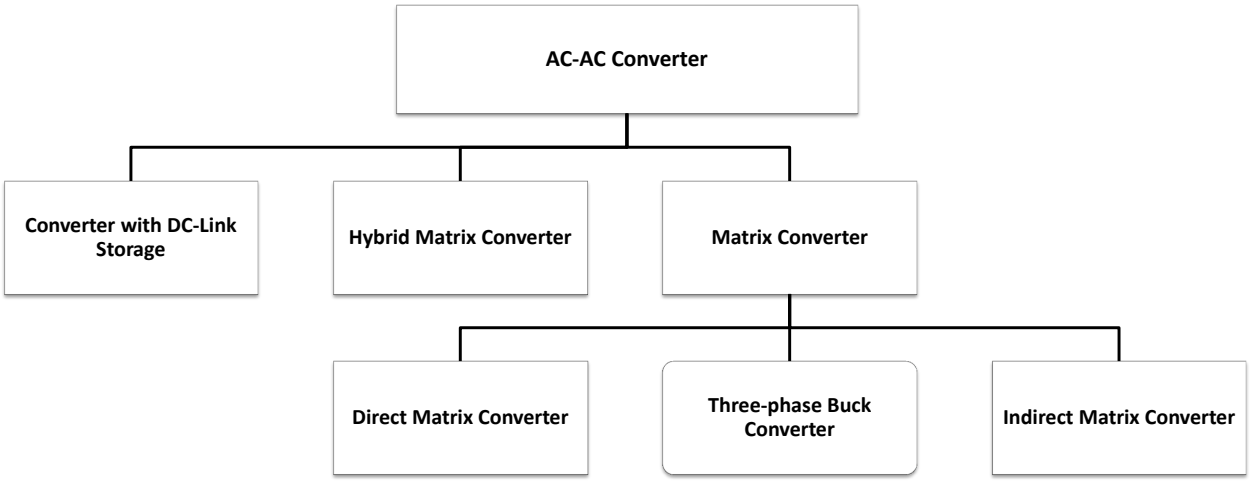


Figure 1. Landscape of three-phase AC-AC converters.

The world's first commercial matrix converter was introduced in 2005 by Yaskawa, the Japanese drive manufacturer, with the product label "Varispeed AC" [6]. The AC7 MC has two voltage classes (230 V and 480 V) and was made available in power levels ranging from 9 to 114 kVA [21]. The DMC topology is realized with Fuji Electric's 1200 V RB-IGBTs [6]. This industrial drive allows full regenerative operation and supports 150% overload. The maximum total harmonic distortion of the input current is 7%. Applications such as lifts, hoists, conveyors, and escalators can benefit from the inherent regeneration capability [22].

Later in 2006, Fuji Electric Systems introduced the FRENIC-Mx series of matrix converters (230 V and 480 V voltage classes) with power levels ranging from 15 to 45 kW [22]. Similar to Yaskawa, Fuji also employs the DMC topology for this series [6] that is promoted for application with significant energy saving potential associated with the full regeneration capability.

The FSDrive-MX1S medium-voltage MC was launched in 2007 by Yaskawa with input voltages of 3.3 kV and 6.6 kV, and power rating from 200 to 6000 kVA [21]. The same standard power cell based on DMC is used both for the 3.3 kV class by connecting three cells in series or the 6.6 kV class by connecting six cells in series [21]. The output line-to-line voltage waveform with three cells in series has 13 levels, which is very close to a sinusoidal wave and significantly reduces the need for filtering. The MC topology simplifies the system which reduces the wiring costs and only occupies one half of the footprint of that occupied by a conventional drive system [21]. The matrix converter efficiency is approximately 98% and the power factor is around 0.95 regardless of operation speed [23].

In 2014, Yaskawa launched the U1000 Industrial Matrix Drive that is a new generation of compact and high efficient motor drive with full regeneration capability. The U1000 is based on the DMC topology and is available in two voltage classes (240 V and 480 V) with power levels ranging from 3.7 to 372 kVA. A low harmonic content (3 to 5%) across a wide load and speed range, and a near unity power factor (above 0.98) at full load, ensure a

clean power at the grid interface. Furthermore, a high reliability with a mean time between failures (MTBF) of 28 years is guaranteed [24].

One can think that the reliability of matrix converters is less than the more traditional industrial drive topologies (e.g., voltage source converter (VSC)) because of the increased number of semiconductors used [22]. Despite the fact that the failure rate for the MC increases due to the higher number of switches, the voltage stress at which the devices are operated is much lower than the VSC topologies [25].

Matrix converters have also been proposed to enhance power quality in the distribution system. The vector switching converter (VeSC) is a reduced version of the DMC topology that can be used in a dynamic voltage restorer (DVR) to compensate both balance and unbalanced sags when supplying sensitive loads [26,27].

Despite all the important benefits associated to the matrix converters and the extensive research over the last forty years, such topologies are still not widely used in the industry. Yaskawa Electric is the sole drive manufacturer with commercial products based on MCs. Thus, the MC is one of the most investigated but less industrial applied converter topologies [6]. The 86% maximum input-to-output voltage transfer ratio for sinusoidal modulation and the limited capability to compensate reactive power have been limiting the MC adoption to compete with the conventional solutions based on VSC [6]. Furthermore, the lack of monolithic bidirectional semiconductors in the market [28], associated with the need of complex strategies for the commutation of the bidirectional power switches, which normally requires a control system based on FPGA [29,30], are challenges that still need to be overcome in order to make the matrix converters a mainstream solution for the power electronics market.

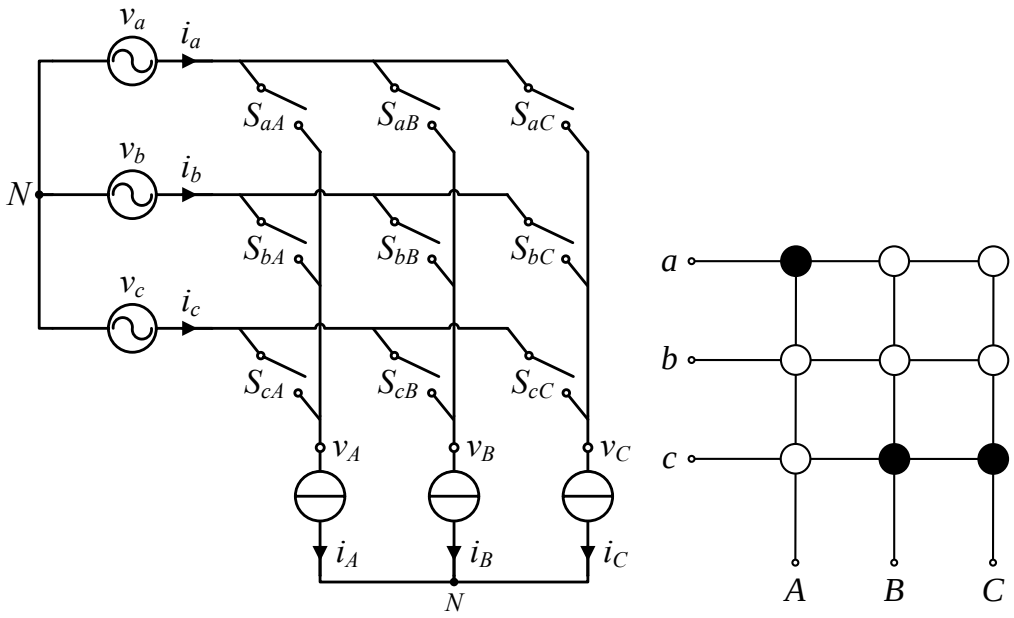
In this article, the Direct Matrix Converter and the Indirect Matrix Converter will be presented along with a review of the respective actual and most important technical solutions. This work contributes to the field by providing a large overview of the modulation methods. To this end, a selection of published works related to matrix converters and modulation techniques is reviewed. Recommendations pertaining to the technological implementation are also highlighted in this article.

2. Direct Matrix Converter

The Direct Matrix Converter [31] is a single-stage topology composed by a set of $m \times n$ bidirectional power switches to connect a m-phase voltage source to a n-phase load [1]. The 3Φ-3Φ MC is the preeminent topology as it connects a three-phase voltage source (e.g., electric grid) with a three-phase load (e.g., motor) [32]. The power circuit is made of nine bidirectional switches distributed in three sets of three [33]. Each group can also be designated as a switching cell (SwC). Therefore, with this arrangement it is possible to connect any of the input phase a, b, or c to any of the output phase A, B, or C, as represented in Figure 2a. The schematic diagram is similar to a matrix, with the rows consisting of the three input phases (a, b, and c), the columns consisting of the three output phases (A, B, and C), and the bidirectional switches making the connection between the rows and columns, which are symbolized with circles in Figure 2b.

The matrix converter operation can be described by a mathematical equation using the concept of switching function [34]. The switching function, S_{jK}, can be described as the modeling of the device connecting input phase j to output phase K. When the device is *closed*, the result of the switching function is *1*, and when the device is *open*, the result of the switching function is *0*. Therefore, the switching function of a single device is defined as [35]

$$S_{jK}(t) = \begin{cases} 1, & S_{jK} \text{ closed} \\ 0, & S_{jK} \text{ open} \end{cases} \qquad j = \{a, b, c\}, \qquad K = \{A, B, C\} \tag{1}$$



(**a**) (**b**)

Figure 2. Direct Matrix Converter topology. (**a**) Schematic diagram. (**b**) Symbol.

2.1. Mathematical Model

In order to develop a modulation method for the MC, a mathematical model must be first derived.

The source and load voltages referenced to the input neutral, "*n*" in Figure 2a, can be formulated as the following vectors:

$$\mathbf{v_i} = \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix}, \qquad \mathbf{v_o} = \begin{bmatrix} v_A \\ v_B \\ v_C \end{bmatrix}. \tag{2}$$

Due to the lack of a DC-link capacitor, the matrix converter transfer power between source and load instantaneously. Therefore, it is possible to formulate a transfer function relating the electrical parameters on one side with the corresponding parameters on the other side [33]. Using this principle, the relationship between load and source voltages can be described as

$$\left.\begin{array}{c} \begin{bmatrix} v_A \\ v_B \\ v_C \end{bmatrix} = \begin{bmatrix} S_{aA} & S_{bA} & S_{cA} \\ S_{aB} & S_{bB} & S_{cB} \\ S_{aC} & S_{bC} & S_{cC} \end{bmatrix} \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} \\ \mathbf{v_o} = \mathbf{T}(S_{jK})\mathbf{v_i} \end{array}\right\} \tag{3}$$

where $\mathbf{T}(S_{jK})$ is the instantaneous transfer matrix that represents the state of the converter switches [1] and is defined as

$$\mathbf{T}(S_{jK}) = \begin{bmatrix} S_{aA} & S_{bA} & S_{cA} \\ S_{aB} & S_{bB} & S_{cB} \\ S_{aC} & S_{bC} & S_{cC} \end{bmatrix}. \tag{4}$$

Each row of $\mathbf{T}(S_{jK})$ denotes the status of the devices linked on the same output phase, and each column denotes the status of the devices linked on the same input phase [33].

Using the same principle, the following relationship can also be used to relate the source and load currents:

$$\left.\begin{array}{c} \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} = \begin{bmatrix} S_{aA} & S_{aB} & S_{aC} \\ S_{bA} & S_{bB} & S_{bC} \\ S_{cA} & S_{cB} & S_{cC} \end{bmatrix} \begin{bmatrix} i_A \\ i_B \\ i_C \end{bmatrix} \\ \mathbf{i_i} = \mathbf{T}(S_{jK})^T \mathbf{i_o} \end{array}\right\} \quad (5)$$

where $\mathbf{T}(S_{jK})^T$ is the transpose matrix of $\mathbf{T}(S_{jK})$.

By considering that the bidirectional power switches work with a switching frequency much higher than the frequencies of the input voltages and output currents, the high-frequency (HF) harmonics in (3) and (5) can be neglected [35]. Then, an output voltage of variable amplitude and low frequency (LF) can be produced by adjusting the duty cycle of the devices using their respective switching functions [1]. The local-averaged value of a switching function S_{jK} corresponds to the duty cycle of the device, and it is defined as d_{jK}:

$$0 \leq d_{jK} \leq 1, \qquad j = \{a, b, c\}, \qquad K = \{A, B, C\} \quad (6)$$

The low-frequency equivalents of (3) and (5) are

$$\overline{\mathbf{v}}_\mathbf{o} = \overline{\mathbf{T}}(d_{jK})\mathbf{v_i} \quad (7)$$

$$\overline{\mathbf{i}}_\mathbf{i} = \overline{\mathbf{T}}(d_{jK})^T \mathbf{i_o} \quad (8)$$

respectively, where

$$\overline{\mathbf{T}}(d_{jK}) = \begin{bmatrix} d_{aA} & d_{bA} & d_{cA} \\ d_{aB} & d_{bB} & d_{cB} \\ d_{aC} & d_{bC} & d_{cC} \end{bmatrix} \quad (9)$$

is the LF instantaneous transfer matrix that represents the duty cycle of the converter switches. The $\overline{\mathbf{T}}(d_{jK})^T$ is the transpose matrix of $\overline{\mathbf{T}}(d_{jK})$.

Equations (3) and (5) give the instantaneous relationships between input and output quantities and are the basis of all modulation methods [1,36]. The output voltages and the input currents can be derived based on the input voltages, load parameters, and the switching states defined by the modulation method. In the same way, Equations (7) and (8) can be used to compute the low-frequency components of input and output quantities and modeling the matrix converter operation.

2.2. Possible Switching States

Contrary to the conventional VSCs, matrix converters do not have intrinsic freewheeling paths. For this reason, a safe transition between the allowed states of a switching cell is more complex to achieve. Ideally, the commutation between the bidirectional switches should occur instantaneously and simultaneously in order to satisfy the restriction in (10). However, in practice, this is not possible due to propagation delays in the command circuits and finite switching times of the power semiconductors. For a more clear explanation, the basic commutation circuit of a switching cell is illustrated in Figure 3. Three bidirectional switches connect ideal voltage sources to the output phase *K* that feeds an *RL* load.

There are two basic rules for the safe commutation between the switches in the switching cell:

- the simultaneous connection of two devices to the same output line must be averted to prevent short circuit of the input voltage sources, and
- one device must always be conducting to establish a path for the inductive load current in order to prevent overvoltages.

If these rules are not followed, line-to-line short circuits or overvoltages can destroy the converter. These constraints can be expressed by

$$S_{aK} + S_{bK} + S_{cK} = 1, \qquad K = \{A, B, C\}. \tag{10}$$

With these constraints, the 2^9 different switch combinations that the 3Φ-3Φ matrix converter appears to have are reduced to only 27 allowed switching states [35]. Figure 4 summarizes the allowed switch states that are subdivided into three groups [37]. Each of these switch combinations is characterized by a three-letter code that denotes to which input line the respective output phase is connected (see Figure 2b). For example, "*abb*" denotes that the output phases *A*, *B*, and *C* are, respectively, connected to input lines *a*, *b*, and *b*.

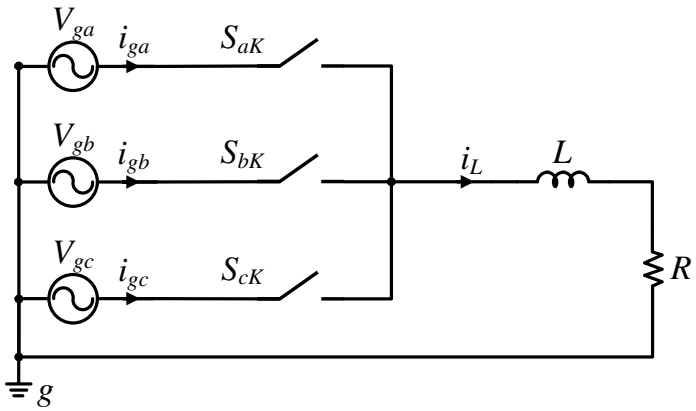


Figure 3. Basic commutation circuit of a switching cell with an *RL* load.

Each switching state of the matrix converter specifies one output voltage and one input current space vector. These vectors can be called voltage (current) Switching Space Vectors (SSV) [38]. Therefore, the MCs synthesize the output voltage (input current) vector from the input voltages (output currents). According to the characteristics of the SSVs associated with each switching state, the 27 allowed switching states are clustered into three groups as shown in Figure 4:

- *Group I*: six switching states establish a path between each output phase and a different input phase. These SSVs have constant amplitudes. Voltage SSVs rotate at the input frequency ω_i, and current SSVs rotate at the output frequency ω_o [39];
- *Group II*: eighteen switching states where two output phases are connected to one input phase, and the third output phase is connected to one of the other input phases. These voltage (current) SSVs have fixed directions, regularly spaced 60° apart in the $\alpha\beta$ frame [1]. For this reason, these SSVs are called "stationary vectors". The magnitude of these voltage (current) SSVs varies with the input voltage phase angle and the output current phase angle, respectively [40]. The magnitude of output voltage vectors can go up to $2/\sqrt{3} \cdot V_{env}$ where V_{env} is the instantaneous value of the rectified input voltage envelope [1];
- *Group III*: three combinations where all three output phases are connected to the same input phase. These SSVs produce null output voltage and input current vectors (i.e., located at the origin of the $\alpha\beta$ frame) and for this reason they will be named "zero vectors".

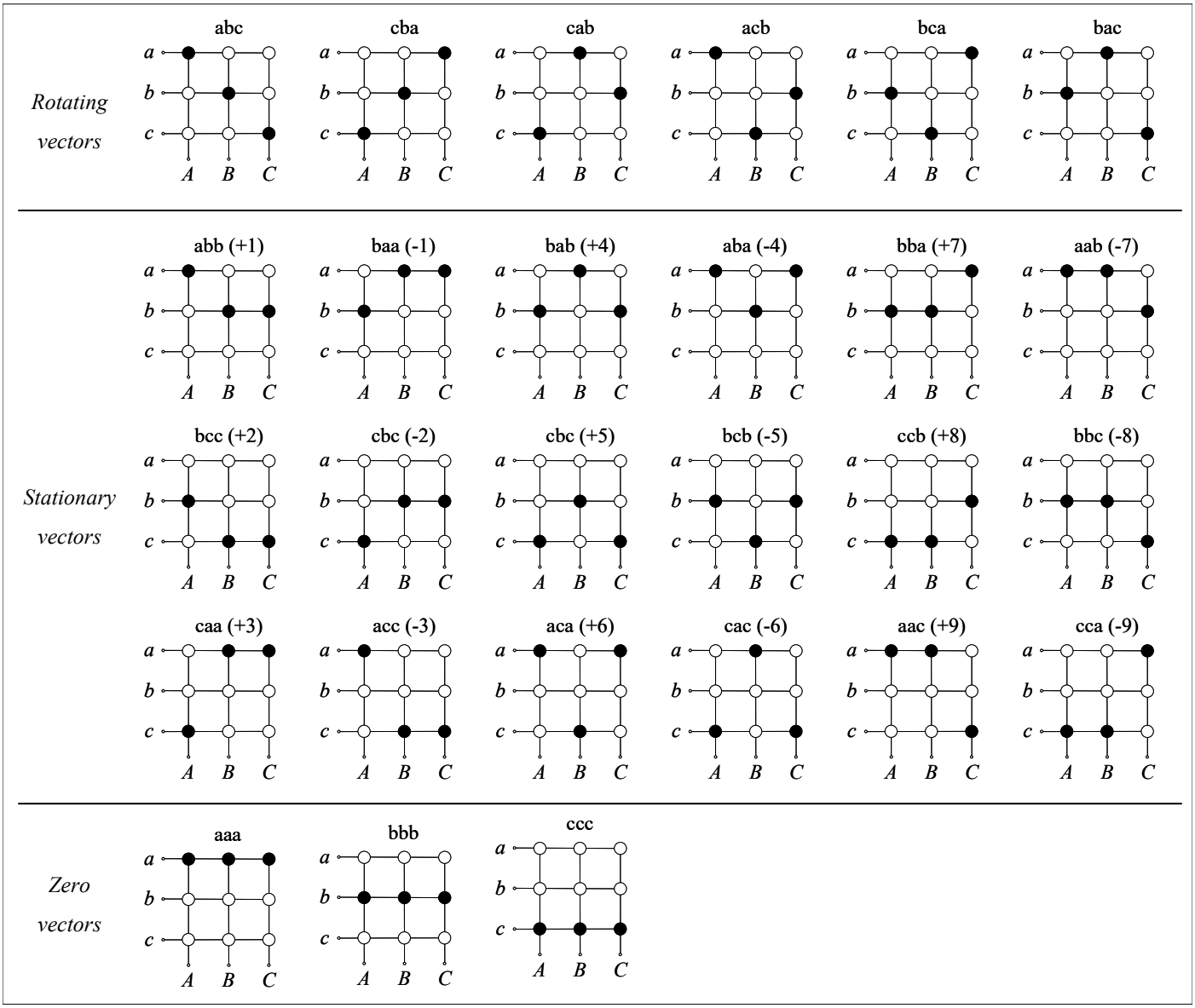


Figure 4. The 27 allowed switch states in a matrix converter.

2.3. Review of Modulation Techniques for DMC

The modulation technique used to control the bidirectional switches has a direct impact on the performance and efficiency of the matrix converter [41]. Several modulation techniques were proposed for the MC since the original control theory proposed by Gyugyi and Pelly in 1976 [42]. The modulation of the matrix converter has evolved from complicated modulation expressions based on transfer function approaches to modern space vector modulation [43]. Figure 5 shows a summary of modulation techniques for MCs.

The Venturini modulation, also known as the AV Method or the direct transfer function approach, was the first important technique to be proposed for the DMC. It was a result of the Alesina and Venturini works published in 1980 [3,4]. Although this technique was more effective than traditional control methods, the maximum voltage transfer ratio was limited to $q = 0.5$. By the end of the 1980s, these two researchers proposed in [44,45] an improved control algorithm by adding a harmonic component to the output reference voltage. This optimum AV modulation, also known as the OAV Method, improved the maximum voltage transfer ratio to 0.866 (or $\sqrt{3}/2$). As demonstrated in [46], this is the theoretical limit to achieve sinusoidal input and output current with complete input power factor control.

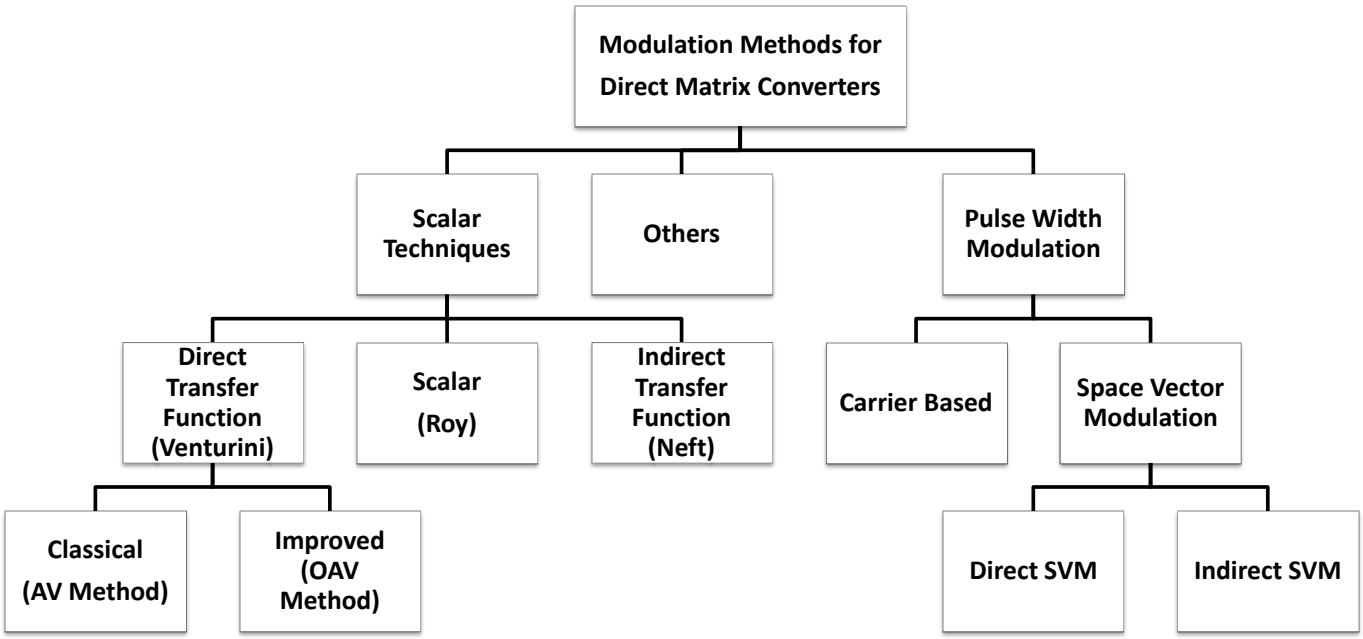


Figure 5. Classification of matrix converter (MC) modulation techniques.

The "fictitious DC-link" was proposed by Rodriguez in 1983 as a new concept to modulate the DMC [47]. With this indirect method, the matrix converter is divided in a rectifier stage and an inversion stage, allowing increasing the maximum voltage transfer ratio above the 0.866 limit of other methods [1]. The research works [48,49] of Ziogas et al. published in 1985–1986 allow increasing the maximum voltage transfer ratio to 1.053 with the trade-off of low-frequency current harmonic distortion [1]. The experimental validation of the indirect modulation principle can be found in [50].

In 1989, Roy developed the scalar modulation algorithm [51], which uses the instantaneous voltage ratio of specific input phase voltages to generate the switch command signals. The main disadvantage of this algorithm is that it needs an accurate measuring of the instantaneous input voltages to do a comparison between their relative magnitudes [1].

Apart from the scalar techniques presented above, the PWM techniques are a very important solution for the control of the MCs. The carrier-based modulation is the simplest approach of this category and came from the modulation of conventional converts [36]. Some works with this modulation technique are reported, for example, in [52,53].

The application of space vector modulation (SVM) to a matrix converter is conceptually the same as the well-known SVM for voltage source inverters (VSI). However, it is more complicated as SVM has to be applied simultaneously to modulate both the output voltage and the input current. In 1989, as a result of investigations done by Huber and Borojevic [54], the first space vector modulation method was proposed for the matrix converters. This was accomplished by combining the principles of indirect transfer function approach with the basis of SVM, resulting in the Indirect Space Vector Modulation (ISVM). The matrix converter is considered as an imaginary two-stage converter: a rectification stage that establishes a fictitious DC-link and an inverter stage that generates the reference output voltages. Each of these stages is controlled using the space vector modulation procedures. The final modulation can then be obtained by merging the two independent space vector modulations. The ISVM was further investigated and is among others treated in [35,55].

In 1993, Casadei et al. proposed in [56] a different approach to SVM for MCs. Instead of looking to the matrix converter as a two-stage converter with fictitious DC-link, the authors represent all the switch combinations in the stationary $\alpha\beta$ frame and then apply the known space vector approach to modulate simultaneously the output voltage and input current. Therefore, it is commonly known as Direct Space Vector Modulation (DSVM) and has

a more explicit relation with the direct power conversion process [46]. The DSVM was further investigated and is among others treated in [57,58].

Other modulation techniques, such as model predictive control [59–61], sliding mode vector control [62], direct torque control [63], direct voltage control [64], analytic signal combined with smooth interpolation [65], and Petri Net [66] were proposed for the control of MCs.

Nowadays, the SVM approach is perhaps the most used and investigated modulation strategy for the MCs [41]. Although the direct and indirect SVM approaches are apparently different, it has been proved in [67] that both can be regarded as one unified SVM method. Therefore, in this work will be explored the DSVM and it will be simply named by SVM as it is the conventional space vector modulation approach.

2.4. Space Vector Modulation for DMC

The SVM has advantages with respect to other strategies [56,67]:

- prompt perception of the necessary commutation process;
- reach the maximum voltage transfer ratio without 3rd harmonic component injection;
- independent control of the input and output power factor;
- minimize the effective switching frequency in each cycle, which reduces the switching losses
- minimize harmonic content; and
- straightforward digital implementation.

2.4.1. Switching Space Vectors

The foundation of space vector modulation lies on the instantaneous space vector depiction of input and output voltages and currents on the $\alpha\beta$ reference frame [58]. The instantaneous output voltage space vector is

$$\overline{v}_o = \frac{2}{3}\left(v_{AB} + \underline{a}v_{BC} + \underline{a}^2 v_{CA}\right) = v_o e^{j\alpha_o} \tag{11}$$

where $\underline{a} \equiv e^{j\frac{2\pi}{3}}$, v_o, and α_o are the amplitude and angle of $\overline{v}_o$. The instantaneous input current space vector is

$$\bar{i}_i = \frac{2}{3}\left(i_a + \underline{a}i_b + \underline{a}^2 i_c\right) = i_i e^{j\beta_i} \tag{12}$$

where i_i and β_i are the amplitude and angle of $\bar{i}_i$, respectively. Using the same transformation, the voltage space vector of the input is

$$\overline{v}_i = \frac{2}{3}\left(v_a + \underline{a}v_b + \underline{a}^2 v_c\right) = v_i e^{j\alpha_i} \tag{13}$$

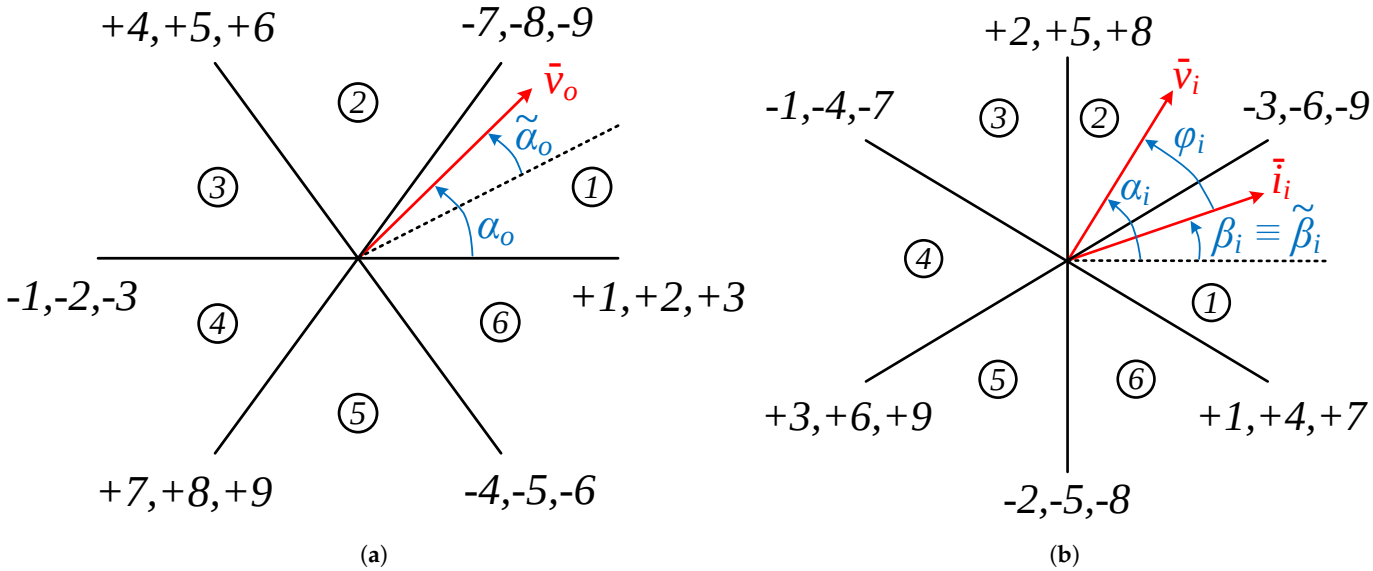
where v_i and α_i are the amplitude and angle of $\overline{v}_i$.

As the output voltage and input current SSVs of Group I are rotating in the $\alpha\beta$ frame, they cannot be effectively used to reconstruct the reference vectors [58]. For this reason, in a SVM strategy, only the stationary and zero vectors are used. Table 1 summarizes the switching arrangements of 3Φ-3Φ matrix converter used in direct SVM.

Output voltage and input current SSVs are represented in the $\alpha\beta$ frame, as shown in Figure 6a,b. Each sector is numbered from 1 to 6 and represents the space between the two adjacent SSVs.

Table 1. Switching arrangements of 3Φ-3Φ MC employed in direct space vector modulation (SVM).

Switch Config.	A	B	C	v_{AB}	v_{BC}	v_{CA}	i_a	i_b	i_c	v_o	α_o	i_i	β_i
$+1$	a	b	b	v_{ab}	0	$-v_{ab}$	i_A	$-i_A$	0	$2/\sqrt{3}\cdot v_{ab}$	0	$2/\sqrt{3}\cdot i_A$	$-\pi/6$
-1	b	a	a	$-v_{ab}$	0	v_{ab}	$-i_A$	i_A	0	$-2/\sqrt{3}\cdot v_{ab}$	0	$-2/\sqrt{3}\cdot i_A$	$-\pi/6$
$+2$	b	c	c	v_{bc}	0	$-v_{bc}$	0	i_A	$-i_A$	$2/\sqrt{3}\cdot v_{bc}$	0	$2/\sqrt{3}\cdot i_A$	$\pi/2$
-2	c	b	b	$-v_{bc}$	0	v_{bc}	0	$-i_A$	i_A	$-2/\sqrt{3}\cdot v_{bc}$	0	$-2/\sqrt{3}\cdot i_A$	$\pi/2$
$+3$	c	a	a	v_{ca}	0	$-v_{ca}$	$-i_A$	0	i_A	$2/\sqrt{3}\cdot v_{ca}$	0	$2/\sqrt{3}\cdot i_A$	$7\pi/6$
-3	a	c	c	$-v_{ca}$	0	v_{ca}	i_A	0	$-i_A$	$-2/\sqrt{3}\cdot v_{ca}$	0	$-2/\sqrt{3}\cdot i_A$	$7\pi/6$
$+4$	b	a	b	$-v_{ab}$	v_{ab}	0	i_B	$-i_B$	0	$2/\sqrt{3}\cdot v_{ab}$	$2\pi/3$	$2/\sqrt{3}\cdot i_B$	$-\pi/6$
-4	a	b	a	v_{ab}	$-v_{ab}$	0	$-i_B$	i_B	0	$-2/\sqrt{3}\cdot v_{ab}$	$2\pi/3$	$-2/\sqrt{3}\cdot i_B$	$-\pi/6$
$+5$	c	b	c	$-v_{bc}$	v_{bc}	0	0	i_B	$-i_B$	$2/\sqrt{3}\cdot v_{bc}$	$2\pi/3$	$2/\sqrt{3}\cdot i_B$	$\pi/2$
-5	b	c	b	v_{bc}	$-v_{bc}$	0	0	$-i_B$	i_B	$-2/\sqrt{3}\cdot v_{bc}$	$2\pi/3$	$-2/\sqrt{3}\cdot i_B$	$\pi/2$
$+6$	a	c	a	$-v_{ca}$	v_{ca}	0	$-i_B$	0	i_B	$2/\sqrt{3}\cdot v_{ca}$	$2\pi/3$	$2/\sqrt{3}\cdot i_B$	$7\pi/6$
-6	c	a	c	v_{ca}	$-v_{ca}$	0	i_B	0	$-i_B$	$-2/\sqrt{3}\cdot v_{ca}$	$2\pi/3$	$-2/\sqrt{3}\cdot i_B$	$7\pi/6$
$+7$	b	b	a	0	$-v_{ab}$	v_{ab}	i_C	$-i_C$	0	$2/\sqrt{3}\cdot v_{ab}$	$4\pi/3$	$2/\sqrt{3}\cdot i_C$	$-\pi/6$
-7	a	a	b	0	v_{ab}	$-v_{ab}$	$-i_C$	i_C	0	$-2/\sqrt{3}\cdot v_{ab}$	$4\pi/3$	$-2/\sqrt{3}\cdot i_C$	$-\pi/6$
$+8$	c	c	b	0	$-v_{bc}$	v_{bc}	0	i_C	$-i_C$	$2/\sqrt{3}\cdot v_{bc}$	$4\pi/3$	$2/\sqrt{3}\cdot i_C$	$\pi/2$
-8	b	b	c	0	v_{bc}	$-v_{bc}$	0	$-i_C$	i_C	$-2/\sqrt{3}\cdot v_{bc}$	$4\pi/3$	$-2/\sqrt{3}\cdot i_C$	$\pi/2$
$+9$	a	a	c	0	$-v_{ca}$	v_{ca}	$-i_C$	0	i_C	$2/\sqrt{3}\cdot v_{ca}$	$4\pi/3$	$2/\sqrt{3}\cdot i_C$	$7\pi/6$
-9	c	c	a	0	v_{ca}	$-v_{ca}$	i_C	0	$-i_C$	$-2/\sqrt{3}\cdot v_{ca}$	$4\pi/3$	$-2/\sqrt{3}\cdot i_C$	$7\pi/6$
0_a	a	a	a	0	0	0	0	0	0	0	–	0	–
0_b	b	b	b	0	0	0	0	0	0	0	–	0	–
0_c	c	c	c	0	0	0	0	0	0	0	–	0	–



(**a**) (**b**)

Figure 6. Stationary vectors representation in $\alpha\beta$ frame. (**a**) Output voltage SSVs. (**b**) Input current SSVs.

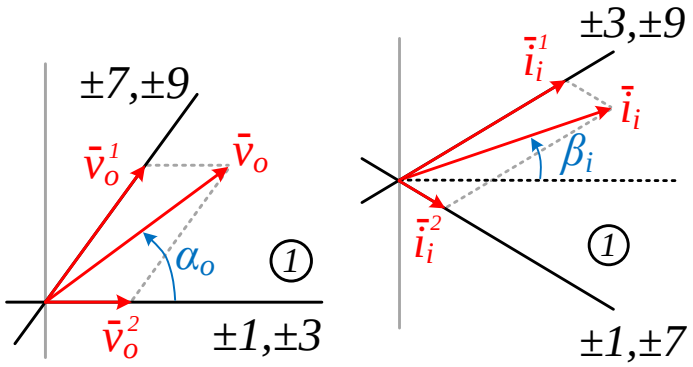
2.4.2. Vector Synthesis

The SVM modulation can inherently reach complete control of both $\overline{v}_i$ and φ_i [35,55,56] that are reference quantities. Let us take Figure 7a,b to explain the modulation principle. $\overline{v}_i$ is set by the input voltage source and its angle α_i can be determined via measurement. Then, the phase angle β_i of $\bar{i}_i$ can be defined as

$$\beta_i = \alpha_i - \varphi_i. \tag{14}$$

Obviously, unitary input power factor can be obtained by aligning vector $\bar{i}_i$ with $\overline{v}_i$.

The SVM modulation is realized by picking four stationary vectors that are applied during adequate time intervals inside the period T_s.



(**a**) (**b**)

Figure 7. Modulation principle of (**a**) $\bar{v}_o$ and (**b**) $\bar{i}_i$.

It will be assumed that both $\bar{v}_o$ and $\bar{i}_i$ are lying in sector 1 without loss of generality. In Figure 7a, $\bar{v}_o^1$ and $\bar{v}_o^2$ represent the components of $\bar{v}_o$ alongside the two SSVs. In Figure 7b, $\bar{i}_i$ is also decomposed into $\bar{i}_i^1$ and $\bar{i}_i^2$ alongside the current SSVs. The switching arrangements able to synthesize the components of $\bar{v}_o$ and $\bar{i}_i$ are

$$\bar{v}_o^1: \quad \pm 7, \pm 8, \pm 9; \qquad \bar{v}_o^2: \quad \pm 1, \pm 2, \pm 3; \tag{15}$$

$$\bar{i}_i^1: \quad \pm 3, \pm 6, \pm 9; \qquad \bar{i}_i^2: \quad \pm 1, \pm 4, \pm 7. \tag{16}$$

To generate $\bar{v}_o$ and $\bar{i}_i$ at the same time, the common switching states ±7, ±9, ±1, and ±3 are employed. Only one of the switching arrangements with same number and opposite signs is applied [38]. The ones with higher voltage values are selected [56]. Based on these rules, the four switching arrangements for each combination of output voltage sector (K_V) and input current sector (K_I) can be determined as shown in Figure 8 [68].

$\bar{v}_o$ and $\bar{i}_i$ are then synthesized by time averaging of each of the four stationary vectors during the switching sequence. As mentioned above, both $\bar{v}_o$ and $\bar{i}_i$ are generated by applying the stationary vectors according to proper duty cycles. They are determined using the phase of output voltage vector reference ($\tilde{\alpha}_o$) and the phase of input current vector reference ($\tilde{\beta}_i$) as follows [57]:

$$\delta^I = \frac{2}{\sqrt{3}}\, q\, \frac{cos(\tilde{\alpha}_o - \pi/3)\, cos(\tilde{\beta}_i - \pi/3)}{cos\varphi_i} \tag{17}$$

$$\delta^{II} = \frac{2}{\sqrt{3}}\, q\, \frac{cos(\tilde{\alpha}_o - \pi/3)\, cos(\tilde{\beta}_i + \pi/3)}{cos\varphi_i} \tag{18}$$

$$\delta^{III} = \frac{2}{\sqrt{3}}\, q\, \frac{cos(\tilde{\alpha}_o + \pi/3)\, cos(\tilde{\beta}_i - \pi/3)}{cos\varphi_i} \tag{19}$$

$$\delta^{IV} = \frac{2}{\sqrt{3}}\, q\, \frac{cos(\tilde{\alpha}_o + \pi/3)\, cos(\tilde{\beta}_i + \pi/3)}{cos\varphi_i} \tag{20}$$

where $q = |\bar{v}_o|/(\sqrt{3}|\bar{v}_i|)$ is the voltage transfer ratio. As shown in Figure 6, $\tilde{\alpha}_o$ and $\tilde{\beta}_i$ used in (17)–(20) are angles determined respecting to the bisecting line of the corresponding sector. They differ from α_o and β_i according to the output voltage and input current sectors [57]. $\tilde{\alpha}_o$ and $\tilde{\beta}_i$ have the following limits:

$$-\frac{\pi}{6} < \tilde{\alpha}_o < +\frac{\pi}{6}, \qquad -\frac{\pi}{6} < \tilde{\beta}_i < +\frac{\pi}{6}. \tag{21}$$

The duty cycle of the zero vectors—δ^{0a}, δ^{0b}, and δ^{0c}—is calculated in order to complete the switching period, i.e., at a fixed sampling:

$$\delta^{0a} + \delta^{0b} + \delta^{0c} = 1 - (\delta^{I} + \delta^{II} + \delta^{III} + \delta^{IV}). \tag{22}$$

Consequently, the duty cycles for the switching arrangements are restricted by the subsequent constraints:

$$\begin{aligned} \delta^{0a}, \delta^{0b}, \delta^{0c} &\geq 0 \\ \delta^{I}, \delta^{II}, \delta^{III}, \delta^{IV} &\geq 0. \end{aligned} \tag{23}$$

Considering (17)–(23), and assuming balanced supply voltages and output voltages, the maximum voltage transfer ratio is given by [58]

$$q <= \frac{\sqrt{3}}{2}|cos\varphi_i|. \tag{24}$$

		K_V													
		1 or 4					2 or 5					3 or 6				
K_I	1 or 4	(1,1) (4,4)	+9	−7	−3	+1	(4,2) (1,5)	+6	−4	−9	+7	(1,3) (4,6)	+3	−1	−6	+4
		(4,1) (1,4)	−9	+7	+3	−1	(1,2) (4,5)	−6	+4	+9	−7	(4,3) (1,6)	−3	+1	+6	−4
	2 or 5	(5,1) (2,4)	+8	−9	−2	+3	(2,2) (5,5)	+5	−6	−8	+9	(5,3) (2,6)	+2	−3	−5	+6
		(2,1) (5,4)	−8	+9	+2	−3	(5,2) (2,5)	−5	+6	+8	−9	(2,3) (5,6)	−2	+3	+5	−6
	3 or 6	(3,1) (6,4)	+7	−8	−1	+2	(6,2) (3,5)	+4	−5	−7	+8	(3,3) (6,6)	+1	−2	−4	+5
		(6,1) (3,4)	−7	+8	+1	−2	(3,2) (6,5)	−4	+5	+7	−8	(6,3) (3,6)	−1	+2	+4	−5
			I	II	III	IV		I	II	III	IV		I	II	III	IV

Figure 8. Selection of switching arrangements for each set of K_V and K_I.

2.4.3. Switching Pattern

The four general switching arrangements along with the zero vectors can be organized within the switching period T_s. This switching configuration sequence that defines the turn-on and turn-off sequence of the switches is commonly named switching pattern [58]. Different switching patterns have different impact on the efficiency and conducted emissions of the MC. This way, the arrangement of the three zero voltage vectors introduces a degree of freedom that can be used to enhance the modulation [41,67].

In the first works regarding SVM, only one zero vector placed at the end of the switching period was used [56]. For this reason, this switching pattern is considered a single-sided modulation. At the cost of only a slight increment in the number of Branch-Switch-Over (BSO) per switching period, double-sided modulation has become the prevalent strategy, as it allows a better harmonic performance at both input and output side of MC [37]. From the use of three zero vectors in each cycle period arises a switching pattern with 12 BSOs [58]. It

can be verified that among all possible switching sequences there is only one pattern where only one switching commutation for each change of the output voltage occurs. Table 2 shows the switching sequence for the first half of the period T_s as a function of the sum of K_V and K_I. In the other half of the period, the sequence order is reversed. δ^{01}, δ^{02}, and δ^{03} are the duty cycles of the three zero states that are used in the switching pattern.

Table 2. Switching sequence for the first half of T_s.

$K_V + K_I$	Switching Sequence						
Even	δ^{01}	δ^{III}	δ^{I}	δ^{02}	δ^{II}	δ^{IV}	δ^{03}
Odd	δ^{01}	δ^{I}	δ^{III}	δ^{02}	δ^{IV}	δ^{II}	δ^{03}

These zero states correspond to different zero vectors that should be selected according to the input current sector as represented in Table 3.

Table 3. Zero states to select according the input current sector.

K_I	δ^{01}	δ^{02}	δ^{03}
1, 4	δ^{0c}	δ^{0a}	δ^{0b}
2, 5	δ^{0b}	δ^{0c}	δ^{0a}
3, 6	δ^{0a}	δ^{0b}	δ^{0c}

The resultant switching sequence of output voltages in the time domain is shown in Table 4.

Table 4. Switching sequence of output voltages according to the input current sector.

K_I	Output Voltages
1, 4	c a b b a c
2, 5	b c a a c b
3, 6	a b c c b a

Assuming that both the $\overline{v}_o$ and $\bar{i}_i$ are in sector 1, the corresponding general double-sided switching pattern is as shown in Figure 9.

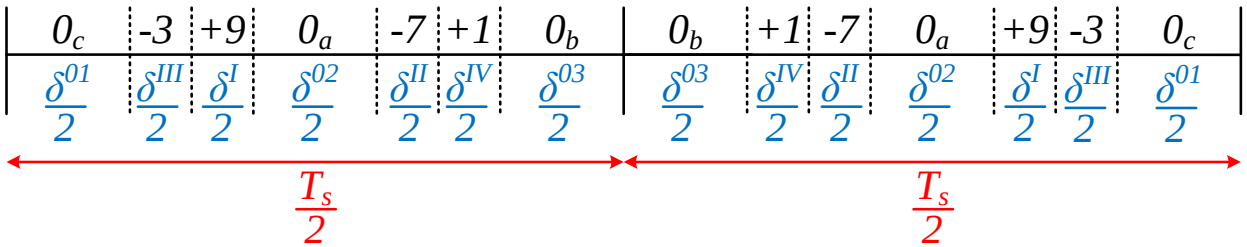


Figure 9. General double-sided switching pattern in a switching period T_s with $K_V = K_I = 1$.

The input current ripple depends on the switching frequency seen from the input and on the values of the input filter parts [69]. For a given input filter, the only way to reduce the input current ripple is to increase the switching frequency. The input switching frequency can be determined by the number of breaks in the MC input current which corresponds to a zero-vector [69]. There are two degrees of freedom when constructing the switching pattern due to the three zero switching states. These two degrees of freedom can be used to suppress one or two zero states, which affects the number of BSO in a period T_s, leading to a two-zero or one-zero switching pattern. The different switching patterns were assessed in [41] in order to investigate their effect in the power losses and in the harmonics

of input and output current. Table 5 shows the different switching strategies and their switching frequencies according to the zero states represented in Figure 9.

Table 5. Strategies for zero switching states and respective switching frequencies.

Strategy Number	Defining Equation	Switching Frequency
1	$\delta^{01} = \delta^{03} = 0$	$f_s = 8/T_s$
2	$\delta^{01} = \delta^{02} = 0$	$f_s = 8/T_s$
3	$\delta^{02} = \delta^{03} = 0$	$f_s = 8/T_s$
4	$\delta^{01} = \delta^{03}$, $\delta^{02} = 0$	$f_s = 10/T_s$
5	$\delta^{01} = \delta^{02}$, $\delta^{03} = 0$	$f_s = 10/T_s$
6	$\delta^{02} = \delta^{03}$, $\delta^{01} = 0$	$f_s = 10/T_s$
7	$\delta^{01} = \delta^{02} = \delta^{03}$	$f_s = 12/T_s$

Strategies 1–3 are defined by a single zero state for the period $T_s/2$ and thus have eight BSOs [70]. Strategy 1 was proposed in [71] and is commonly known as Low-Distortion modulation method. This strategy employs only the zero configuration in the middle of half period (δ^{02} in Figure 9), and therefore the switches of one branch do not alter their states (in this case, the first branch of Figure 2a).

Strategies 4–6 employ two zero states for each half of the switching pattern and have 10 BSOs. Strategy 4 was proposed in [69] and raises the switching frequency on the input side to 60% compared to strategies 2 and 3. Among all different strategies, the lower harmonic content on the input current is reached with Strategy 4.

Strategy 7 applies all the three-zero states in each switching pattern, with the same duty cycles, and thus has 12 BSOs. In the same way, a three-zero switching pattern can raise the switching frequency on the input voltage source in 25% compared to a two-zero switching pattern. Among these seven strategies, the lower harmonic content on the output current is reached with Strategy 7.

An optimal modulation strategy regarding output current ripple was proposed in [41]. This strategy is based on the calculation of the optimal duty cycles of the zeros states to achieve the minimum *rms* value of the output current ripple in each switching period. As the efficiency is also better than the Strategy 7, the optimal modulation must be chosen when the output current quality is a necessity.

In sum, Strategy 4 should be chosen if the input current quality or efficiency are the most important requirements. Conversely, if the output current quality is a priority then optimal modulation should be preferred [41].

3. Indirect Matrix Converter

The "fictitious DC-link" was proposed in 1983 by Rodriguez for the control of Direct Matrix Converter [47]. Considering this approach, Holtz and Boelkens [72] proposed in 1989 a new topology that physically implements the direct MC with indirect modulation to explore the "fictitious DC-link" idea through the reorganization of the DMC switches [73,74]. For this reason, it is called Indirect Matrix Converter and is an alternative to the DMC, as it provides the same advantages and drawbacks [9]. Figure 10 shows the schematic of the IMC topology.

The IMC is composed by two stages: the source and the load side converter [75]. The source converter is a three-phase to single-phase (3Φ-1Φ) MC composed of six bidirectional switches. This converter operates as a Current Source Rectifier (CSR) to synthesize sinusoidal input currents and keeps a constant average voltage at the DC bus. The load side converter is a conventional three-phase VSI composed of six unidirectional switches that generate the output voltages. The dual bridges together employ 18 power switches and 18 diodes like in the direct matrix converter. Nevertheless, this topology is easier to realize as a standard six-pack power module for the inverter stage can be employed versus the exclusive use of bidirectional switches in the direct MC. The IMC also turns possible a

reduction in the amount of active switches on the source side converter to only three if no bidirectional power flow is required [76].

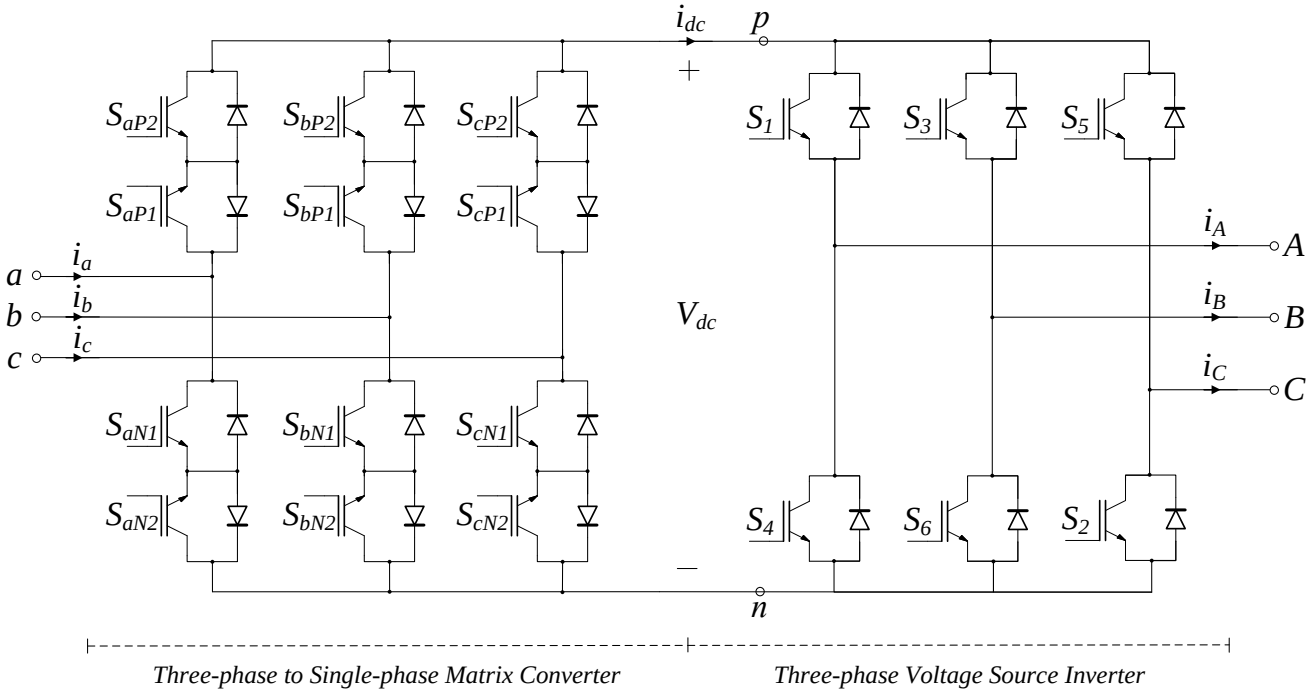


Figure 10. Indirect matrix converter topology.

3.1. Review of Modulation Techniques for IMC

The existence of two stages in the IMC allows the employment of conceptually different control techniques that take advantage of the decoupling present in the conversion process. The synchronization of the CSR and VSI modulations is required to ensure power balance and sinusoidal input currents, as there are not any energy storage element between the dual bridges [77].

Several modulation techniques were proposed for the indirect MC, but most research on IMC has been done using pulse width modulation [78], space vector modulation [79], or predictive control [80].

In 1995, Huber et al. [35] formulated the ISVM for the DMC. Then, Jussila in [81] extensively investigated and applied the ISVM to the IMC.

Due to the current interest and high performance of this modulation, the main aspects of the ISVM for controlling the indirect MC will be presented in the next section.

3.2. Space Vector Modulation for IMC

The indirect SVM for the IMC also makes use of the instantaneous space vector approach to represent the input and output voltages and currents. As the IMC is a two-stage topology, the modulation for the source and load bridges can be done separately. Then, the duty cycles that result from this analysis can be combined to complete the modulation. In the following, a sufficiently high switching frequency is assumed so that the input current and output voltage reference vectors are kept fixed over the switching period.

3.2.1. Space Vector Modulation of Source Bridge

The switching configurations of the input phases a, b, and c of the source bridge can be described by switching functions sw_a, sw_b, and sw_c, respectively. As described by the restriction in (10), the input phases cannot be short-circuited. In this way, these switching functions can assume only three values:

- 1: connection of the input phase to the DC-bus bar p through the on-state of the upper switch;
- 0: unconnected state when both switches are off; and
- -1: connection of the input phase to the DC-bus bar n through the on-state of the lower switch.

As only one input phase can be connected to each bar at a time, the input switching functions should satisfy

$$sw_a + sw_b + sw_c = 0. \tag{25}$$

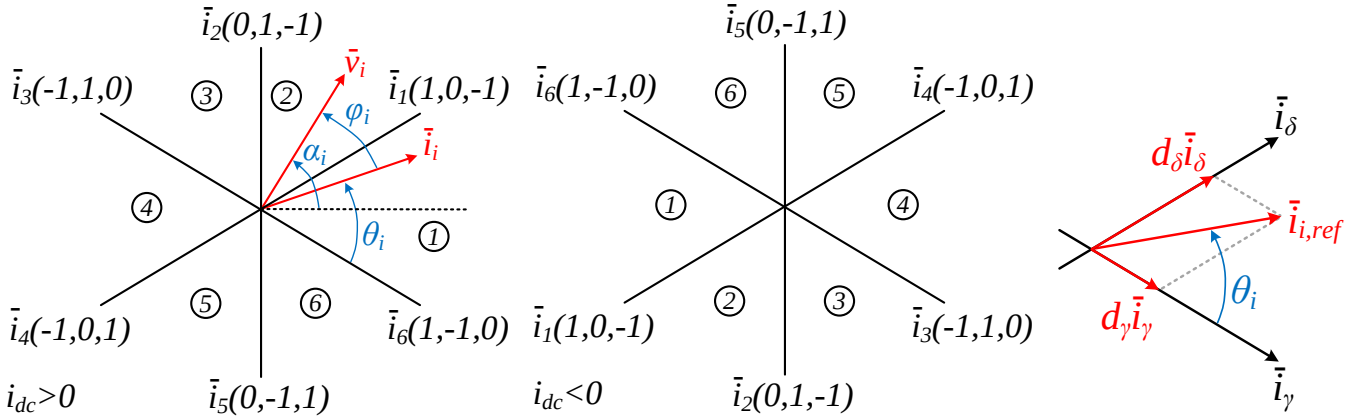
The input currents can be expressed through the switching functions: $i_a = sw_a i_{dc}$, $i_b = sw_b i_{dc}$, and $i_c = sw_c i_{dc}$. Considering this result, (12) can be rewritten to express the instantaneous input current space vector as follows:

$$\bar{i}_i = \frac{2}{3}\left(i_a + \underline{a} i_b + \underline{a}^2 i_c\right) = \frac{2}{3}\left(sw_a + \underline{a} sw_b + \underline{a}^2 sw_c\right) i_{dc} = \overline{sw}_i i_{dc} \tag{26}$$

where i_{dc} is the DC-link current and $\overline{sw}_i$ is the space vector of the source bridge switching functions:

$$\overline{sw}_i = \frac{2}{3}\left(sw_a + \underline{a} sw_b + \underline{a}^2 sw_c\right). \tag{27}$$

If the different associations of sw_a, sw_b, and sw_c are substituted inside (27), one can draw the input current vectors represented in Figure 11a when $i_{dc} > 0$ and in Figure 11b when $i_{dc} < 0$. Each current vector in Figure 11 is denoted by $i_x(sw_a, sw_b, sw_c)$.



(**a**) (**b**) (**c**)

Figure 11. Input current SSVs in $\alpha\beta$ frame when (**a**) $i_{dc} > 0$ and (**b**) $i_{dc} < 0$. (**c**) Generation of input current reference vector $i_{i,ref}$.

As depicted in Figure 11c, $i_{i,ref}$ can be synthesized in one switching period by means of the two adjacent current vectors:

$$\bar{i}_{i,ref} = d_\gamma \bar{i}_\gamma + d_\delta \bar{i}_\delta \tag{28}$$

where the duty cycles of $\bar{i}_\gamma$ and $\bar{i}_\delta$ are d_γ and d_δ, respectively. θ_i is the angle of $i_{i,ref}$ within the actual sector. As proved in [81], the duty cycles d_γ and d_δ are

$$d_\gamma = \frac{|\bar{i}_{i,ref}|}{|i_{dc}|} \sin\left(\frac{\pi}{3} - \theta_i\right) = \sin\left(\frac{\pi}{3} - \theta_i\right) \tag{29}$$

$$d_\delta = \frac{|\bar{i}_{i,ref}|}{|i_{dc}|} \sin(\theta_i) = \sin(\theta_i) \tag{30}$$

as the current ratio $|\bar{i}_{i,ref}|/|i_{dc}|$ is set at unity to not limit the link current i_{dc} that is dependent of the load.

3.2.2. Space Vector Modulation of Load Bridge

The switching states of the output phases A, B, and C of the load bridge can be described by switching functions sw_A, sw_B, and sw_C, respectively. As described by the restriction in (10), the open circuit of the load is not allowed. In this way, these switching functions can assume only two values:

- 1: output phase connected to the DC-bus bar p through the on-state of the upper switch and
- -1: output phase connected to the DC-bus bar n through the on-state of the lower switch.

As at least one output phase must be connected to each bar at a time, the output switching functions should satisfy

$$sw_A + sw_B + sw_C \neq 0. \tag{31}$$

The output phase voltages referenced to the DC-bus's virtual midpoint can be expressed through the switching functions: $v_A = sw_A V_{dc}/2$, $v_B = sw_B V_{dc}/2$, and $v_C = sw_C V_{dc}/2$. Considering this result, the instantaneous output voltage space vector is

$$\overline{v}_o = \frac{2}{3}\left(v_A + \underline{a}v_B + \underline{a}^2 v_C\right) = \frac{2}{3}\left(sw_A + \underline{a}sw_B + \underline{a}^2 sw_C\right)\frac{V_{dc}}{2} = \overline{sw}_o\frac{V_{dc}}{2} \tag{32}$$

where V_{dc} is the DC-bus voltage and $\overline{sw}_o$ is the space vector of the load bridge switching functions:

$$\overline{sw}_o = \frac{2}{3}\left(sw_A + \underline{a}sw_B + \underline{a}^2 sw_C\right). \tag{33}$$

If the different associations of sw_A, sw_B, and sw_C are substituted inside (33), one can draw the output voltage vectors represented in Figure 12a. The zero vectors $\overline{v}_{0+}$ and $\overline{v}_{0-}$ are generated by connecting all output phases to the bar p or to the bar n, respectively. Each voltage vector in Figure 12 is denoted by $v_x(sw_A, sw_B, sw_C)$.

As depicted in Figure 12b, $v_{o,ref}$ can be synthesized in one switching period by means of the two adjacent voltage vectors:

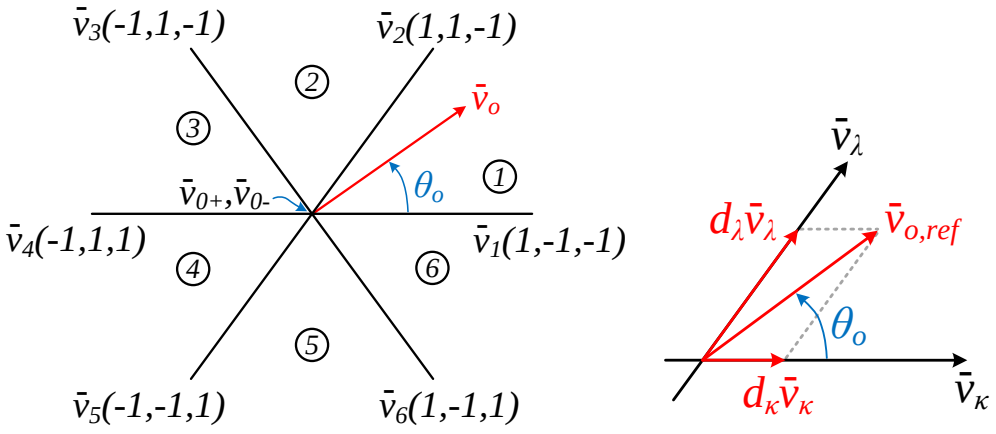
$$\overline{v}_{o,ref} = d_\kappa \overline{v}_\kappa + d_\lambda \overline{v}_\lambda \tag{34}$$

where the duty cycles of $\overline{v}_\kappa$ and $\overline{v}_\lambda$ are d_κ and d_λ, respectively. θ_o is the angle of the reference voltage vector within the actual sector. As proved in [81], the duty cycles d_κ and d_λ are

$$d_\kappa = \frac{|\overline{v}_{o,ref}|\sqrt{3}}{V_{dc}}\sin\left(\frac{\pi}{3} - \theta_o\right) = m\sin\left(\frac{\pi}{3} - \theta_o\right) \tag{35}$$

$$d_\lambda = \frac{|\overline{v}_{o,ref}|\sqrt{3}}{V_{dc}}\sin(\theta_o) = m\sin(\theta_o) \tag{36}$$

where m denotes the modulation index that ranges from zero to unity.



(**a**) (**b**)

Figure 12. (**a**) Output phase voltage SSVs in $\alpha\beta$ frame. (**b**) Generation of the output voltage reference vector $v_{o,ref}$.

3.2.3. Combination of Source and Load Bridges

As shown in Figure 10, the source and load bridges are coupled to each other through the fictitious DC-link. As proved in [81], the output voltage is synthesized by applying the load bridge states during source bridge states. In this way, the resulting four active voltage vectors—$\overline{v}_{\gamma\kappa}$, $\overline{v}_{\delta\kappa}$, $\overline{v}_{\gamma\lambda}$, and $\overline{v}_{\delta\lambda}$—are used to synthesize the output voltage in the modulation period T_s. The duty cycles of the active voltage vectors are

$$d_{\gamma\kappa} = d_\kappa d_\gamma = m\sin\left(\frac{\pi}{3} - \theta_o\right)\sin\left(\frac{\pi}{3} - \theta_i\right), \tag{37}$$

$$d_{\delta\kappa} = d_\kappa d_\delta = m\sin\left(\frac{\pi}{3} - \theta_o\right)\sin(\theta_i), \tag{38}$$

$$d_{\gamma\lambda} = d_\lambda d_\gamma = m\sin(\theta_o)\sin\left(\frac{\pi}{3} - \theta_i\right), \tag{39}$$

$$d_{\delta\lambda} = d_\lambda d_\delta = m\sin(\theta_o)\sin(\theta_i). \tag{40}$$

The duty cycle of the zero vectors $\overline{v}_{0(+,-)}$ is calculated in order to complete the switching period, i.e., at a fixed sampling

$$d_0 = 1 - (d_{\gamma\kappa} + d_{\delta\kappa} + d_{\gamma\lambda} + d_{\delta\lambda}). \tag{41}$$

The modulation index m establishes a straight relation amid the output and input voltages of the IMC. Thus, it is necessary to express the average DC-bus voltage V_{dc} by the input quantities as follows:

$$V_{dc} = \frac{3}{2}|\overline{v}_{i,1}|cos\varphi_{i,1} \tag{42}$$

which can be substituted into (35) and (36) to obtain

$$m = \frac{2}{\sqrt{3}}\frac{|\overline{v}_{o,ref}|}{|\overline{v}_{i,1}|cos\varphi_{i,1}} = \frac{2}{\sqrt{3}}\frac{q_{ref}}{cos\varphi_{i,1}} \tag{43}$$

where q_{ref} is the reference of the input-to-output voltage transfer ratio, $\varphi_{i,1}$ is the fundamental displacement angle between the input current and phase voltage, and it is assumed that $\overline{v}_{o,ref}$ and $\overline{v}_{i,1}$ contain only the fundamental component. In the linear modulation range, $m = [0,1]$, and thus q_{ref} is $\sqrt{3}/2 = 0.866$, which is attained when $cos\varphi_{i,1}$ is unity. This result is coherent with the previously obtained in (24) for the DMC controlled by direct SVM.

With the present modulation, the DC-link voltage v_{dc} produced by the source bridge is always positive. In this way, the diodes of the load bridge are continuously reverse-biased so that the DC-bus is short-circuited. Furthermore, considering that the same performance of the DMC is achieved, it is clear the advantages of the IMC controlled by the indirect SVM.

3.2.4. Switching Pattern

The duty cycles presented in (37)–(41) can be organized in several ways to form the switching pattern. The works in [2,35,70,82,83] present alternatives and comparison of modulation methods that intend to minimize the common-mode voltage, the number of commutations, or the output voltage distortion. The different switching patterns have distinct impact on the harmonics and efficiency of the IMC.

Two alternatives for the switching pattern are presented in [2]. The first strategy allows a zero current switching (ZCS) of the input bridge, and the second strategy allows a zero voltage switching (ZVS) of the output bridge. Considering the higher number of switches in the input bridge and the higher complexity involved in the second strategy, the first strategy is preferable for practical purposes.

In [82], a Conventional SVM (CSVM) is proposed that is very similar to the first strategy presented in [2]. In the CSVM, the duty cycles are organized in order to minimize the number of commutations. Accordingly, only one commutation for each duty cycle transition occurs within this switching pattern. Thus, whereas the ZCS result in eight BSOs, the CSVM produces only six BSOs. Considering the high number of switches of the IMC, this is an important approach to decrease the switching losses and increase the overall conversion efficiency. Moreover, the CSVM has the advantage that can be implemented with simpler logic. For this reason, the CSVM was chosen for this work and will be presented as follows.

The following rules define how the CSVM switching pattern is implemented for the 36 combinations of input and output sectors:

- the source bridge pattern is $\gamma - \delta - \gamma$;
- the load bridge pattern is $\kappa - \lambda - 0 - \lambda - \kappa$ if the sum of K_V and K_I is even;
- the load bridge pattern is $\lambda - \kappa - 0 - \kappa - \lambda$ if the sum of K_V and K_I is odd;
- if K_I is even the output zero vector must be $\overline{v}_{0+}$ (1,1,1) as shown in Figure 12;
- if K_I is odd the output zero vector must be $\overline{v}_{0-}$ (-1,-1,-1) as shown in Figure 12.

Similarly to the switching pattern for the DSVM (see Section 2.4.3), a double-sided symmetric pattern with $\overline{v}_0$ in the center of the modulation period T_s is employed. The resulting duty cycle patterns of the CSVM for the first half of T_s are shown in Table 6. To achieve a symmetric switching pattern, the active vectors order is reversed in the other half of the period.

Table 6. Duty cycle patterns of the conventional SVM (CSVM) for the first half of T_s.

$K_V + K_I$	Duty Cycle Sequence				
Even	$d_{\gamma\kappa}/2$	$d_{\gamma\lambda}/2$	$d_{\delta\lambda}/2$	$d_{\delta\kappa}/2$	$d_0/2$
Odd	$d_{\gamma\lambda}/2$	$d_{\gamma\kappa}/2$	$d_{\delta\kappa}/2$	$d_{\delta\lambda}/2$	$d_0/2$

The number of zero states during a modulation period could be expanded by splitting d_0 into several parts. This strategy can improve the output voltage distortion mainly at low modulation indexes at the cost of higher switching losses, which is an important drawback [81]. A common solution involves the change of the modulation method according to the current operation requirements, as investigated, for example, in [69].

Table 7 shows the switching pattern of the CSVM during T_s. The zero output voltage state is generated by employing the zero vector $\overline{v}_0$ in the load bridge, producing a null DC-link current and $v_{AB} = v_{BC} = v_{CA} = 0$. This output voltage is independent of the DC-bus voltage so the state sw_δ is taken for the source bridge during the zero output

voltage state. The sequence for the output bridge varies in function of the input and output sector numbers.

Table 7. Switching pattern of the CSVM for the switching period T_s.

		Switching State								
		1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**
Input state		sw_γ				sw_δ				sw_γ
Output state	Even ($K_V + K_I$)	sw_κ		sw_λ		sw_κ	sw_0	sw_κ	sw_λ	sw_κ
	Odd ($K_V + K_I$)	sw_λ		sw_κ		sw_λ	sw_0	sw_λ	sw_κ	sw_λ

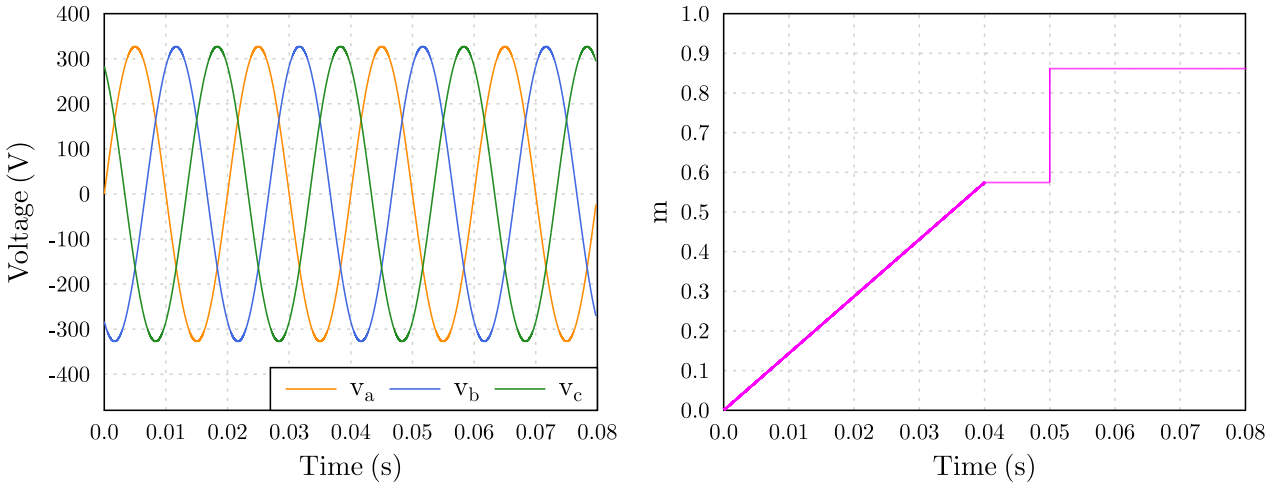
4. Simulation

In order to validate the theoretical analysis and to get a deep insight about the SVM implementation, a simulation workbench was developed. The space vector modulation with the respective switching pattern generator was implemented in MATLAB/Simulink (MLS) [84]. The power circuit was modeled using the circuit simulator GeckoCIRCUITS [85]. Using the available interface between these two simulators, it was possible to perform a complete simulation in both the control/modulation and circuit domains using the parameters listed in Table 8.

Table 8. Parameters used in the simulation.

Parameter	**Value**	**Parameter**	**Value**
V_i	325 V	R	10 Ω
f_i	50 Hz	f_o	100 Hz
f_s	10 kHz	L	30 mH

The reference output frequency was kept constant at 100 Hz and the modulation index was changed according to the curve presented in Figure 13b. The maximum voltage transfer ratio q_{ref} involved in this test is 0.75 which is bellow the limit stated in (24). As a result, the maximum modulation index m used in this simulation is 0.866.



(**a**) (**b**)

Figure 13. (**a**) Input voltages of the DMC controlled by SVM. (**b**) Modulation index.

4.1. Simulation of the SVM for DMC

The power circuit of the DMC modeled for simulation including an *RL* load is represented in Figure 14. As is commonly known, the matrix converter acts as a voltage source at its output and as a current source at its input. For this reason, and due to the high harmonic content of their input current, an input filter is required to interface with the grid and fulfill the standards of electromagnetic compatibility and harmonics. Although, for this first validation we decided to use the same conditions of the theoretical analysis presented above. Thus, an ideal voltage source was directly connected to the DMC input with waveform as depicted Figure 13a.

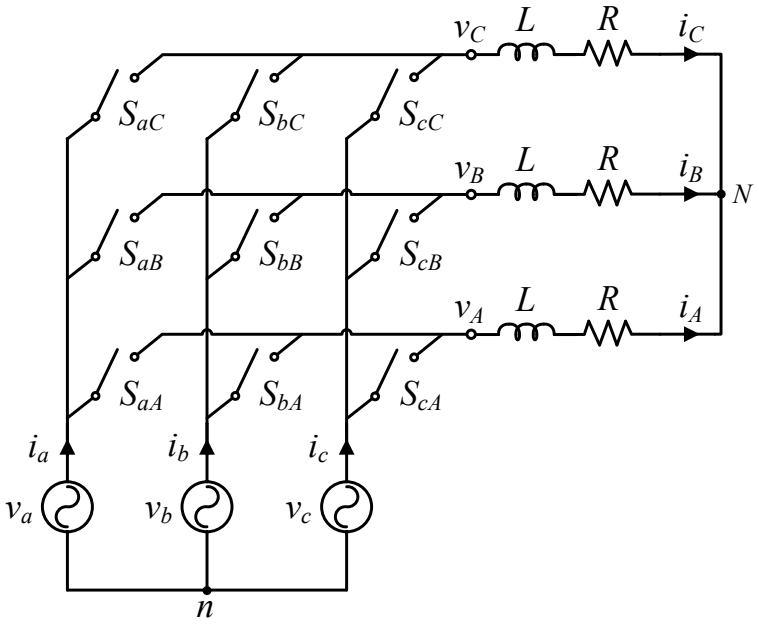


Figure 14. Power circuit of the DMC modeled for simulation.

Figure 15 shows the input currents of the DMC that are supplied by the ideal input voltage source. The magnitude of these currents evolve as a function of the variation in the modulation index. If an appropriately dimensioned low-pass filter is connected between the input voltage source and the DMC, these currents would be nearly sinusoidal.

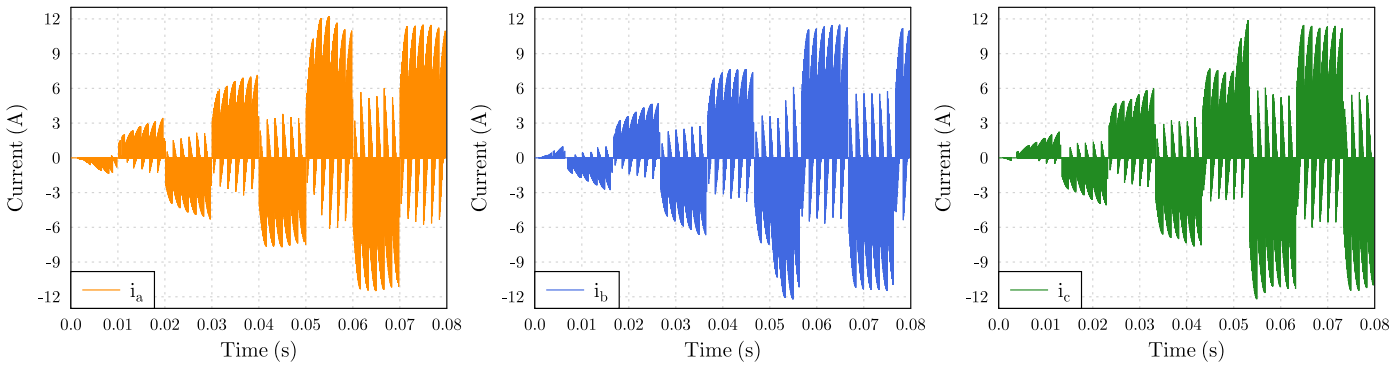


Figure 15. Input currents of the DMC controlled by SVM.

The line and phase voltages at the DMC output are presented in Figures 16 and 17, respectively.

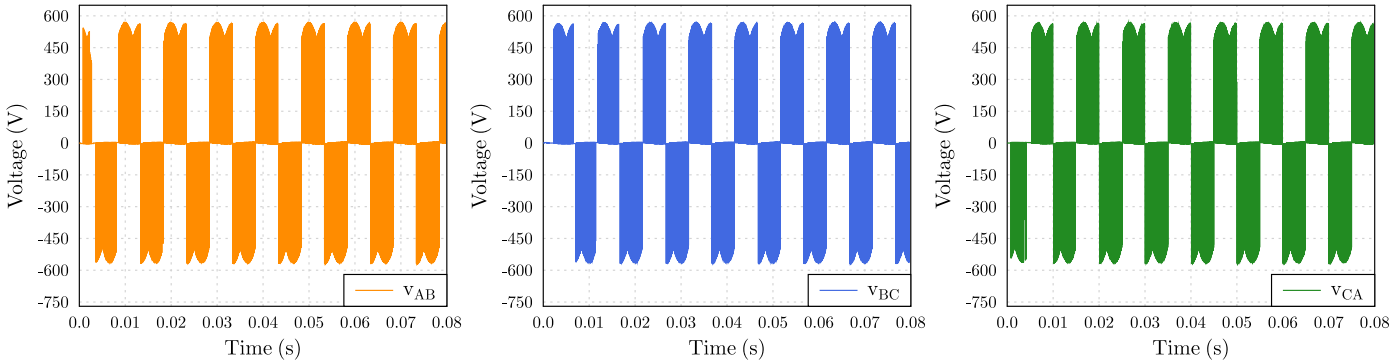


Figure 16. Output line voltages of the DMC controlled by SVM.

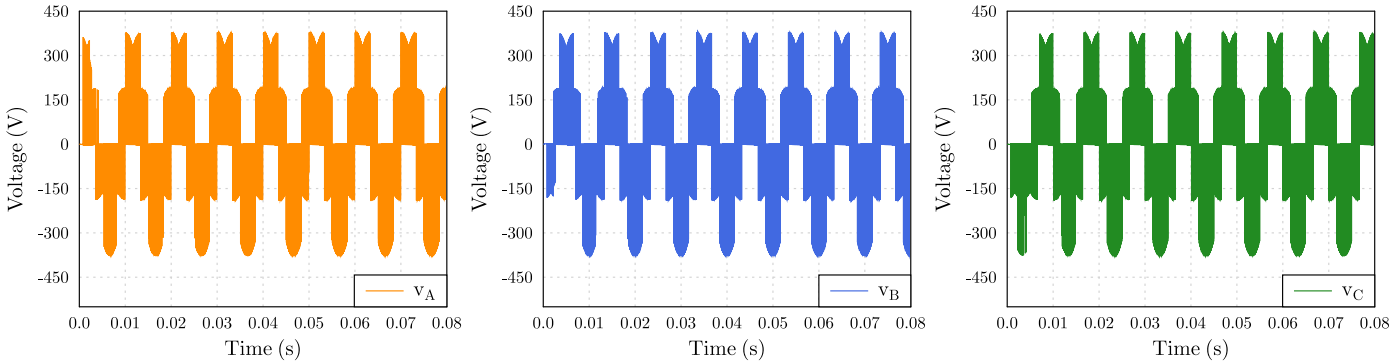


Figure 17. Output phase voltages of the DMC controlled by SVM.

Figure 18 shows the output currents of the matrix converter that circulate in the load. The magnitude of these currents evolves accordingly to the modulation index variation presented in Figure 13b. This load acts as a low-frequency filter and, as a result, the high-frequency components of the output voltages are not present in the output currents. The magnitude of these currents is a function of the load impedance ($2\pi f_o L + R$), the input voltage, and the voltage transfer ratio.

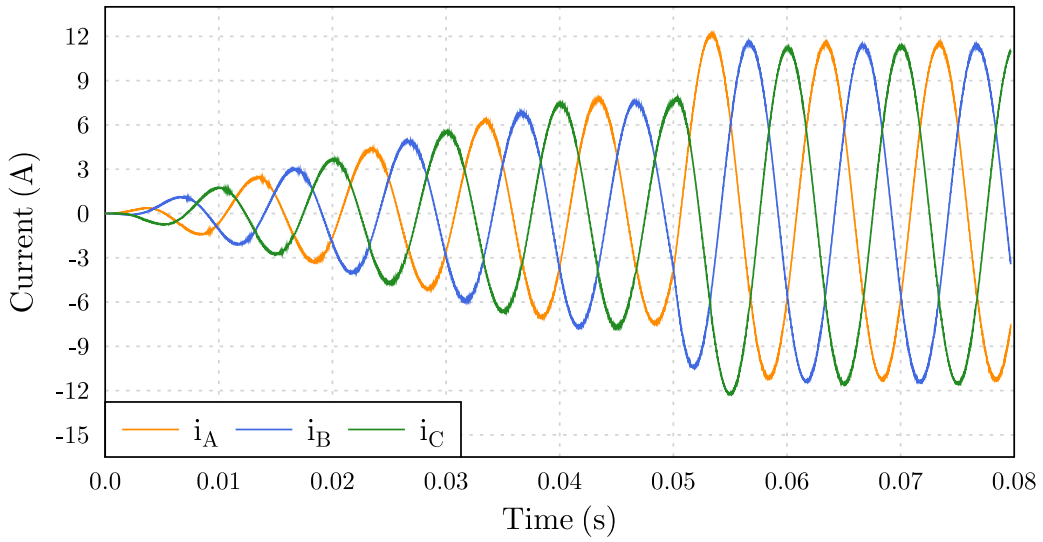


Figure 18. Output currents of the DMC controlled by SVM.

The implementation of the SVM in the developed workbench was very useful to validate the theoretical analysis and to observe the operation of the direct matrix converter.

4.2. Simulation of the SVM for IMC

The power circuit of the IMC modeled for simulation including an *RL* load is represented in Figure 19. The same ideal voltage source was directly connected to the IMC input (see Figure 13a).

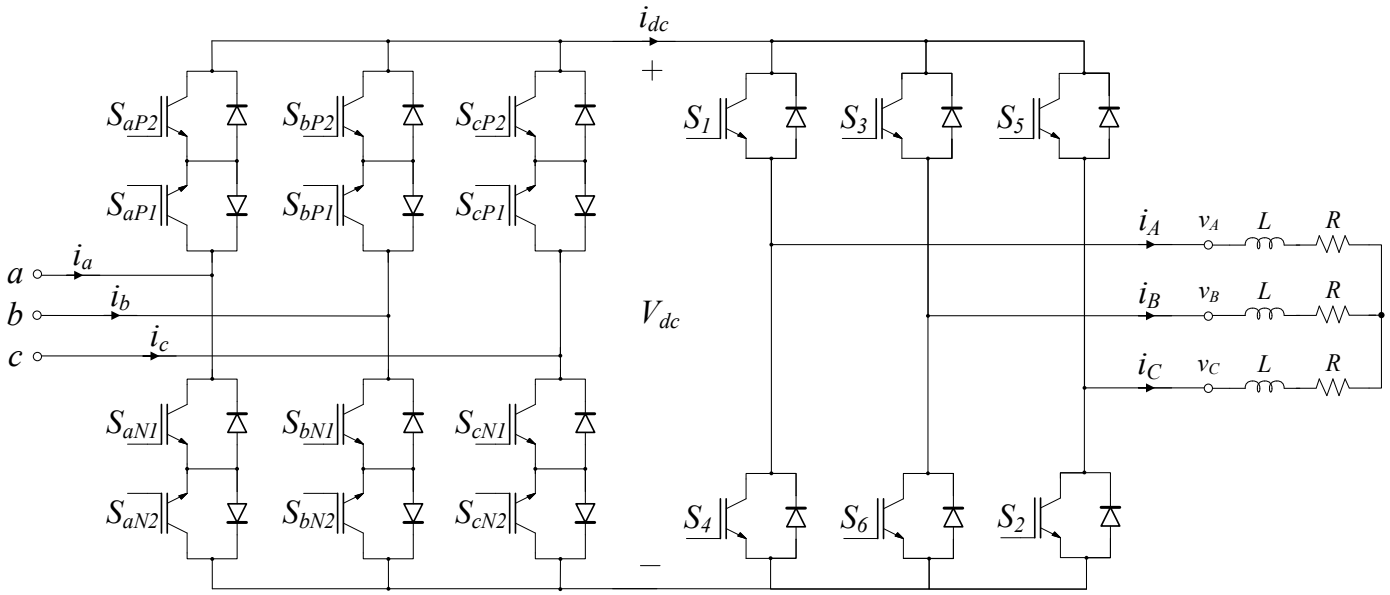


Figure 19. Power circuit of the IMC modeled for simulation.

Figure 20 shows the IMC input currents that are supplied by the ideal input voltage source. The magnitude of these currents evolve according to the modulation index variation. As it is possible to see, a high harmonic content is present in the input current, so an input filter is required to interface with the grid and fulfill the standards of electromagnetic compatibility and harmonics. If an appropriately dimensioned low-pass filter is connected between the input voltage source and the IMC, these currents would be nearly sinusoidal.

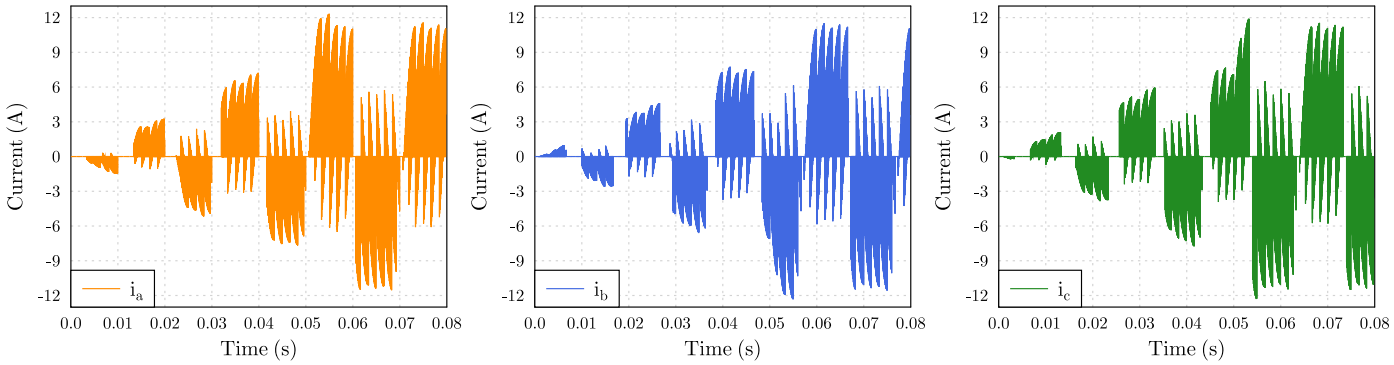
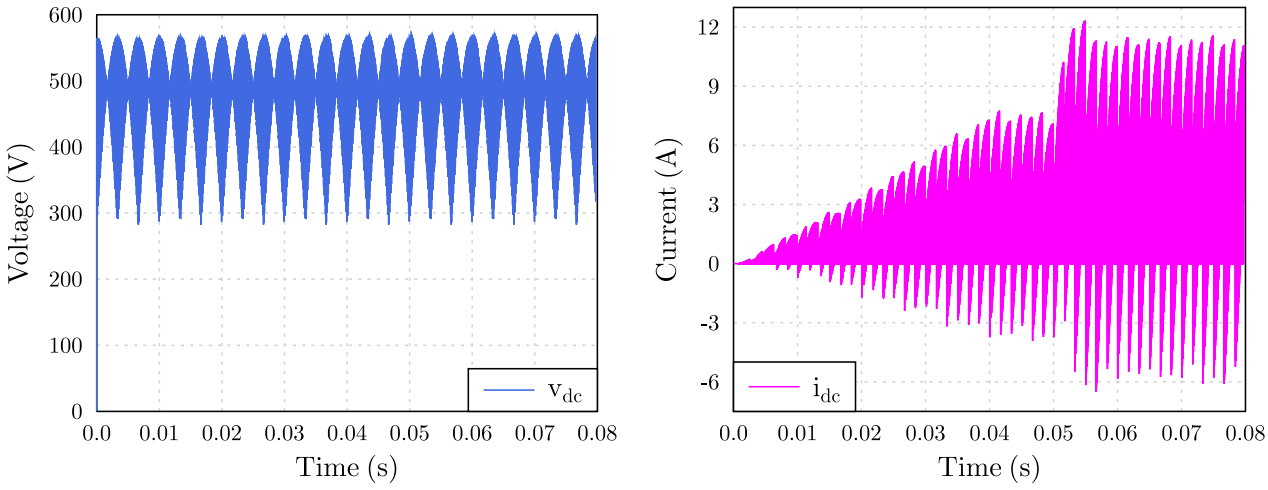


Figure 20. Input currents of the IMC controlled by SVM.

The DC-bus voltage and current are shown in Figure 21. As there is not a capacitor in the DC-link, a fictitious voltage is generated from the IMC input voltage rectification. The average value of this voltage is around 500 V, that is, very near the value that results from (42).



(**a**) (**b**)

Figure 21. DC-link (**a**) voltage and (**b**) current.

The output line and phase voltages at the IMC output are presented in Figures 22 and 23, respectively. For this simulation, the same *RL* load used previously in Section 4.1 was connected in the IMC output.

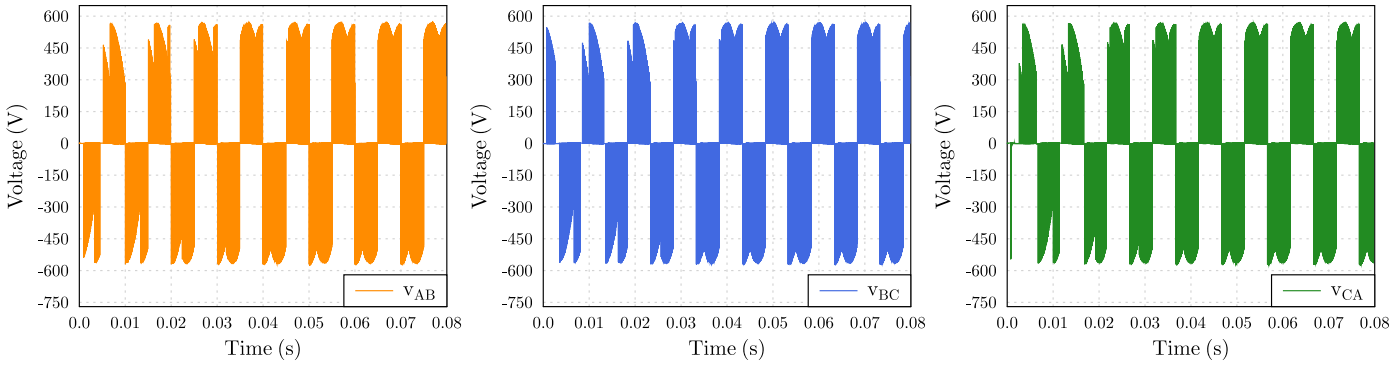


Figure 22. Output line voltages of the IMC controlled by SVM.

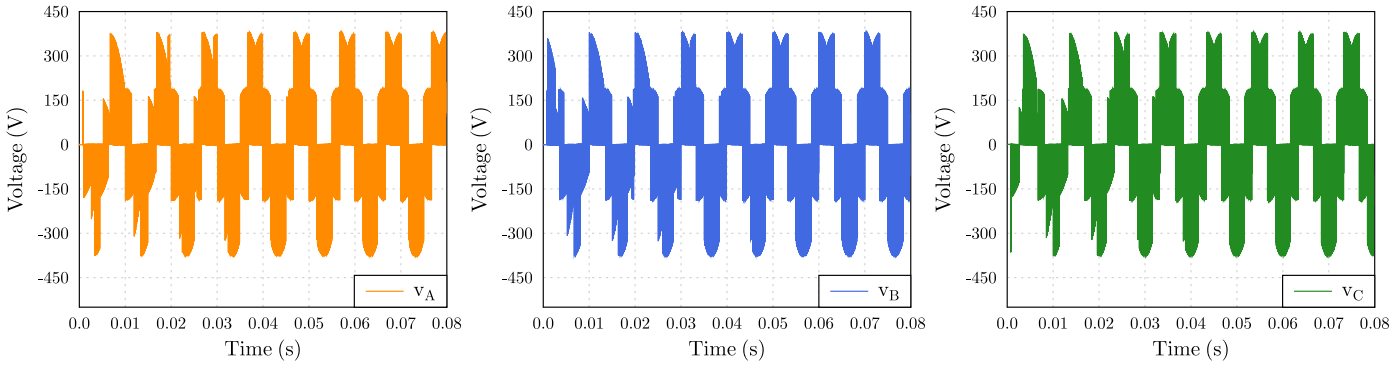


Figure 23. Output phase voltages of the IMC controlled by SVM.

Figure 24 shows the output currents of the MC that circulate in the load. The magnitude of these currents change accordingly to the modulation index variation presented in Figure 13b. The output current is very similar to the previously obtained in Figure 18.

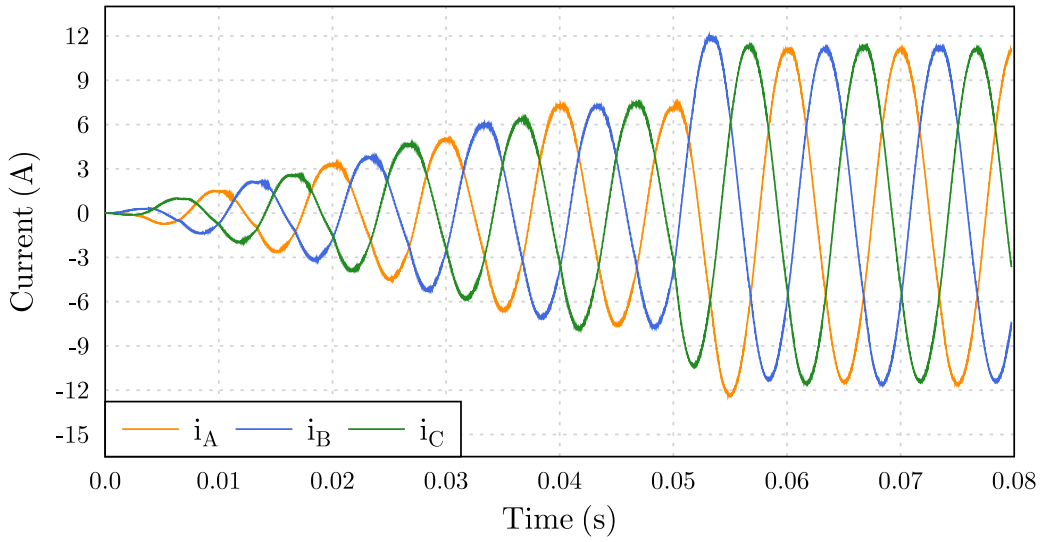


Figure 24. Output currents of the IMC controlled by SVM.

The implementation of the SVM in the developed workbench was very useful to validate the theoretical analysis and to get deep knowledge about the operation of the indirect matrix converter.

5. Conclusions

Matrix converters allow the implementation of single-stage power conversion systems with inherent bidirectional power flow capability. By employing bidirectional switches, MCs can achieve higher power densities when compared with equivalent two-stage power conversion solutions. For that reason, this family of power converters has been receiving significant attention from the academic sector with thousands of research works published over the past forty years. However, just a few commercial products based on MCs are available in the market; Yaskawa Electric is clearly the industrial player with long experience using this technology in motor drive applications.

A detailed review of the Direct Matrix Converter and Indirect Matrix Converter along with the different modulation methods was presented. The Space Vector Modulation is probably the most used modulation strategy for the DMC and IMC due to its low computation requirements and high flexibility. Both topologies are well suited for motor drive applications as demonstrated via simulation results. Besides the capability to synthesize sinusoidal input and output currents with different frequencies, the input power factor can also be adjustable. Furthermore, the inherent full regenerative operation is one of the key characteristics that make the DMC and IMC very attractive to implement a four-quadrant frequency converter with a higher power density when compared with equivalent two-stage power conversion solutions. Thus, it is expected that the application areas of the matrix converter to be expanded, given its advantages of energy saving and size reduction.

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Abbreviations

The following abbreviations are used in this manuscript:

BSO	Branch-Switch-Over
CBC	Current-based Commutation
CSR	Current Source Rectifier
CSVM	Conventional Space Vector Modulation
DMC	Direct Matrix Converter
DSVM	Direct Space Vector Modulation
IMC	Indirect Matrix Converter
ISVM	Indirect Space Vector Modulation
MC	Matrix Converter
MTBF	Mean Time Between Failures
PFC	Power factor correction
SSV	Switching Space Vectors
V2G	Vehicle-to-grid
VSC	Voltage Source Converter
VSI	Voltage Source Inverter
ZCS	Zero Current Switching
ZVS	Zero Voltage Switching

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