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**Abstract:** This paper presents a variable-gain amplifier (VGA) in the 68–78 GHz range. To reduce DC power consumption, the drain voltage was set to 0.5 V with competitive performance in the gain and the noise figure. High-Q shunt capacitors were employed at the gate terminal of the core transistors to move input matching points for easy matching with a compact transformer. The four stages amplifier fabricated in 40-nm bulk complementary metal oxide semiconductor (CMOS) showed a peak gain of 24.5 dB at 71.3 GHz and 3-dB bandwidth of more than 10 GHz in 68–78 GHz range with approximately 4.8-mW power consumption per stage. Gate-bias control of the second stage in which feedback capacitances were neutralized with cross-coupled capacitors allowed us to vary the gain by around 21 dB in the operating frequency band. The noise figure was estimated to be better than 5.9 dB in the operating frequency band from the full electromagnetic (EM) simulation.

**Keywords:** variable-gain amplifier (VGA), E-band; variable-gain; low power consumption; compact layout

# 1. Introduction

For the past few years, automotive radar sensing systems have been massively studied for autonomous cars and relative applications. In addition, a vehicle-to-everything (V2X) system connecting vehicles with vehicles, pedestrians, infrastructure, and networks is believed to another essential technology for future intelligent vehicle applications. Most recently, unified V2X and radar systems operating in E-band (60 GHz–90 GHz) allocated for radar sensing have been reported [1,2].

The unified V2X and radar system demands more advanced radio frequency (RF) frontends to accommodate all requirements for each operation modes. Particularly, receiver frontends need to have very high sensitivity for the sensing mode and large gain tunability for the data link mode. In addition, massive phased-array configuration [3] at mm-wave frequencies requires all function blocks to consume less energy with compact occupying area even for variable-gain amplifiers (VGAs). Obviously, large operating bandwidth performance is mandatory.

This paper presents a variable-gain amplifier (VGA) fabricated in 40-nm CMOS technology in E-band for the unified V2X and radar application. As shown in Figure 1, there are several methods to tune amplifier gain such as the attenuator control technique [4–6], current steering technique [7–11], and digital switching technique [12–14]. Insertion of an attenuator between constant gain blocks provides reliable gain control and wideband operation at the cost of relatively high loss and degradation in the noise performance, particularly in the millimeter-wave frequency band. The current steering technique has the advantages of wide and linear gain control range, low dc power, and simple configuration, but the operating bandwidth would be limited by the current steering circuits. Despite the merit for accurate gain control, the digital switching techniques replying on a lot of transistors for switching are not suitable for low power and beamforming transceivers. In this paper, we adopt a bias current



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**Copyright:** © 2021 by the authors. Licensee MDPI, Basel, Switzerland. This article is an open access article distributed under the terms and conditions of the Creative Commons Attribution (CC BY) license (https:// creativecommons.org/licenses/by/ 4.0/). control technique [15,16] that directly adjusts the transconductance  $(g_m)$  of the transistor by adaptively controlling the gate bias of an amplifying stage. It is advantageous for wide gain range, low power operation, compact design, and wide bandwidth. However, when  $g_m$  varies, input and output impedances of an amplifier vary a lot. Thus, it is hard to maintain good impedance matching for whole gain range. To deal with this issue, we employed the capacitive cross-coupling neutralization technique to improve reverse isolation of each stage of the amplifier [17]. In Section 2, we present the VGA design, followed by the measurement results of the VGA in Section 3. Section 4 concludes this paper.



**Figure 1.** Four topologies of variable-gain amplifiers (VGAs) utilized in millimeter-wave. (**a**) Attenuator control technique, (**b**) current steering technique, (**c**) digital switching technique, and (**d**) bias current control technique.

## 2. Design Approach

Figure 2 shows the circuit schematic of the 4-stage differential VGA. In this work, we aimed to have a compact and low power consumption variable amplifier for the unified V2X-radar phased-array receiver applications in E-band. For the low DC power requirement, we reduced the drain voltage (VD) down to 0.5 V [18]. In order to estimate the performance degradation caused by the lowered VD, a simple simulation for maximum gain and minimum noise figure (NF<sub>min</sub>) was conducted; the results are shown in Figure 3. Note that the drain current was fixed to 10 mA for an N-MOSFET differential pair in this calculation. When VD decreased from 1 V to 0.5 V, the gain and the noise figure degraded by approximately 1.8 dB and 0.3 dB, respectively. Those are believed acceptable for the benefit in the DC power consumption reduction by half. The amplifier consists of four stages of an N-MOSFET differential core to get a high gain and to decrease common mode noise. The total gate width of the core transistors is 34.5  $\mu$ m (1.5  $\mu$ m × 23 fingers) and impedance matching was achieved using low-k transformers for wideband operation.



Figure 2. Schematic of the 4-stage cascade differential VGA.



**Figure 3.** Maximum stable/available gain (MSG/MAG) and NF<sub>min</sub> depending on drain voltage (VD) at 77 GHz.

In the bias current control technique, when  $g_m$  varies, input and output impedances of an amplifier vary a lot. Thus, it is hard to maintain good impedance matching for whole gain range. According to the two-port network theory, input and output reflection coefficients are given by Equations (1) and (2) below

$$\Gamma_{IN} = \frac{Z_{IN} - Z_0}{Z_{IN} + Z_0} = S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1 - S_{22}\Gamma_L},$$
(1)

$$\Gamma_{OUT} = \frac{Z_{OUT} - Z_0}{Z_{OUT} + Z_0} = S_{22} + \frac{S_{12}S_{21}\Gamma_S}{1 - S_{11}\Gamma_S},$$
(2)

where  $\Gamma_{IN}$  and  $\Gamma_{OUT}$  are input and output reflection coefficients, respectively.  $Z_{IN}$  and  $Z_{OUT}$  are input and output impedances, respectively, and  $Z_0$  is the system impedance that is constant. As can be seen, small changes in the input or output impedance can significantly affect the reflection coefficients on the other side, particularly for high gain stage, which can be a serious problem in VGAs based on the bias-control scheme. However, if  $S_{12}$  is low enough, such influences from the other port can be significantly reduced and thus input and output reflection coefficients remain to  $S_{11}$  and  $S_{22}$  of the core N-MOSFETs. In this work, we improve the reverse isolation by applying neutralization to core transistors of the amplifier.

Neutralization has been widely employed to improve reverse isolation and gain of amplifiers by eliminating parasitic gate-drain capacitance ( $C_{gd}$ ) of transistors [15–19]. This unintended feedback path caused by  $C_{gd}$  led to an unstable amplifier and caused signal loss and gain reduction. Each stage of the amplifier was capacitively neutralized with cross-coupling neutralization capacitor ( $C_{nue}$ ) to cancel  $C_{gd}$ . Figure 4 is the small signal equivalent circuit with capacitive neutralization considering only parasitic gate-drain capacitance. Y-parameters of the 2-port network can be written as follows:

$$Y_{12} = -j\omega \Big( C_{gd} - C_{neu} \Big), \tag{3}$$

$$Y_{21} = g_m - j\omega \left( C_{gd} - C_{neu} \right) \tag{4}$$



Figure 4. Small signal equivalent circuit with capacitive neutralization.

Equations (3) and (4) from Figure 4 show that capacitive neutralization can improve reverse isolation and gain [17]. Theoretically, the perfect isolation can be implemented as  $C_{neu}$  is equal to the  $C_{gd}$ .

To verify effect of neutralization, we configured a one-stage amplifier and conducted a simulation as changing the value of  $C_{neu}$ . Figure 5 shows the simulated maximum gain and isolation performance with respect to  $C_{nue}$  at 70 GHz. As can be seen, with the optimum  $C_{nue}$ , overall gain and the isolation can be greatly improved. When  $C_{neu}$  equals  $C_{gd}$ ,  $S_{12}$  is -39.5 dB, which is 22.1-dB lower than that with no neutralization. The gain begins to increase thanks to the effect of neutralization. According to equation (5), stability factor k is inversely proportional to  $S_{12}$ . Thus, as  $S_{12}$  becomes lower, k becomes greater than 1. Then, the gain starts to decrease, and turns to increase as  $S_{12}$  rises again. When k reduces under 1, however, the gain decreases again.

$$k = \frac{1 - |S_{11}|^2 - |S_{22}|^2 - |\Delta|^2}{2|S_{12}S_{21}|}, \ \Delta = S_{11}S_{22} - S_{12}S_{21}$$
(5)



Figure 5. MSG/MAG, stability factor, and reverse isolation according to C<sub>neu</sub> at 70 GHz.

In addition, the neutralization technique makes the input and output impedances less sensitive to change of the bias voltage for gain control. Figure 6 shows the simulated input and output impedances at various gate bias voltages. As can be seen, the magnitudes of the input and output impedance variations are 24.5  $\Omega$  and 69.0  $\Omega$ , respectively, when gate bias voltage is changed from 0.55 V to 0.25 V without  $C_{neu}$  at 73 GHz. With the optimum  $C_{neu}$  for best isolation, however, the input and output impedance variations are reduced to 3.0  $\Omega$  and 14.9  $\Omega$  for input and output ports, respectively. These are about 87 % and 78 % reductions in the impedance variations for each port. Thus, the large impedance variation can be significantly reduced with the neutralization technique, which will be of great help



for the reliable operation of the VGA. From the full EM simulation, we selected 9-fF  $C_{neu}$  for the reverse isolation that is the highest priority.

**Figure 6.** (a) Magnitude of input and output impedances ( $Z_{in}$  and  $Z_{out}$ ) of a single-stage differential amplifier core without neutralization and (b) with neutralization.

Transformers (TFs) have been commonly used for impedance matching in differential CMOS radio frequency integrated circuits (RFICs) [20–24]. TFs provide compact layout compared to other techniques; however, they still occupy large area in general. Given transistors or impedance need to be matched to 50- $\Omega$ ; the required inductances of the TFs are determined from the simple circuit theory and therefore there is no freedom for compact layout. In this work, we introduce a small shunt capacitor at the gate nodes, which led small TFs required for the given matching points. Figure 7a shows a schematic of the impedance matching circuit with a transformer and a shunt capacitor, and Figure 7b shows the equivalent circuit for the impedance matching. The input impedance ( $Z_{in}$ ) and the input source impedance ( $Z_s$ ) seen from the gate node are derived as follows:

$$Z_{in} = \frac{1}{Y_{in} + j(2\omega C_{shunt})},\tag{6}$$

$$Z_{S} = \left[ \left\{ 50 + j\omega \left( \frac{L_{1}}{2} - M \right) \right\} / / j\omega M \right] + j\omega \left( \frac{L_{2}}{2} - M \right), \tag{7}$$

where  $Y_{in}$  is the input admittance of the amplifier core and M is mutual inductance of the transformer. Assuming conjugate impedance matching,  $Z_{in}' = Z_s^*$  should be satisfied at the desired frequency. In order to verify the effectiveness of the shunt capacitor, we conducted simple calculation with the device parameters used in this work. The length and width of the MOSFET for the calculation was selected to 0.04 µm and 34.5 µm, respectively, which has the conductance (*G*) and susceptance (*B*) of 0.005  $\mho$  and 0.015  $\mho$ , respectively.  $L_1$  was assumed to equal  $L_2$ . Figure 7c shows the calculated secondary inductance of the impedance matching TF as a function of the shunt capacitance. This function is obtained by calculating  $Z_{in}' = Z_s^*$  with Equations (6) and (7). As shown in the figure, the shunt capacitor helps to match the given impedance with a small TF, leading compact matching circuit. It is assumed that this approach would improve conduction loss and quality factor of the TF

as well. In this work, an 8-fF capacitor is added in the core, and the layout is shown in Figure 8. Based on the results shown in Figure 7c, the occupied area of the matching TF was reduced by approximately 30 %. In the proposed amplifier, values of the coupling coefficient (*k*) of the transformers were selected to be  $k_1 = -0.63$ ,  $k_2 = -0.24$  and  $k_3 = -0.53$ . A low-*k* transformer that assisted wide bandwidth design was used in an inter-stage impedance matching network. Thick metal layer was used for signal lines to reduce signal losses. A lower metal layer at the gate paths was used to make input impedance of the amplifier core capacitive and thus easy to impedance-match. It should be noted here that large shunt capacitors may limit the gain and the noise performance of the amplifier because of the limited quality factor of the capacitor. In this work, 8-fF capacitance is selected based on the available space and the performance degradation. Quality factor of the shunt capacitor was around 20 at 73 GHz from the full EM simulation. As shown in Figure 3, the gain and the noise degradation due to the 8-fF capacitor were estimated to be around 0.6 dB and 0.3 dB, respectively.



**Figure 7.** (a) A transformer-based impedance matching network. (b) A simple equivalent circuit of the matching network is presented by a half circuit for easy analysis. (c) The calculated secondary inductance according to coupling coefficient against  $C_{shunt}$  at 73 GHz.

In addition, core transistors were weakly degenerated with the thick metal interconnections, of which inductance ( $L_{degen}$ ) was around 1.5 pH. This moved the conjugate input matching point to the middle of the noise circle, resulting in the return loss less than 13 dB even with the noise matching condition.



Figure 8. 3D view of the amplifier core.

#### 3. Measurement Results

The four-stage variable-gain VGA was fabricated in the 40-nm CMOS technology, and the microphotograph is shown in Figure 9. The active area of the proposed amplifier is 668  $\mu$ m  $\times$  159  $\mu$ m without DC and RF pads. The total drain current was 38.2 mA from 0.5-V supply at the peak gain condition. RF measurement was performed with an on-wafer probing system and a 110-GHz vector network analyzer. The effect of the RF pads was not de-embedded here. Figure 10 shows measured small signal S-parameters of the amplifier. The VGA achieved peak gain of 24.5 dB at 71.3 GHz with 3-dB bandwidth of around 10 GHz in 68 GHz–78 GHz span. Thanks to the inductive degeneration, good input return loss less than -10 dB was achieved in the operating frequency band even with the noise matching.



Figure 9. Photograph of the fabricated four-stage variable-gain amplifier (VGA).

In this paper, we control inter-stage gate bias voltages to tune the amplifier gain. In this measurement, to get a variable gain, we controlled the second gate bias voltage, and the measurement results are shown in Figure 11. The peak and minimum gains were achieved with the gate voltages of 0.55 V and 0.225 V, respectively. Meanwhile, DC power consumption of the amplifier was reduced from 19.1 mW to 15.5 mW accordingly. As can be seen,  $S_{21}$  could be tuned by approximately 21 dB in maximum while maintaining the 3-dB bandwidth of 10 GHz. Meanwhile, return losses at input and output ports were rarely changed and remained below 10 dB approximately in overall. At 73 GHz, input and output return loss variations were around 5.4 dB and 1.9 dB, respectively.



Figure 10. Measured S-parameters of the VGA.



**Figure 11.** Measured (a)  $S_{21}$ , (b)  $S_{11}$ , and (c) $S_{22}$  at various gate-bias voltages. The highest gain is when VG = 0.55 V, and the lowest gain is when VG = 0.225 V.

Table 1 summarizes the results of this work along with several prior works operating at similar frequencies. Even with low power consumption and compact layout, competitive performance in gain and tuning range was achieved. In particular, thanks to the compact matching circuit design with the optimum combination of the transformer and shunt capacitors, area reduction of 30% or more was achieved. In addition, the gain in dB per mW of around 1 was achieved by operating the amplifier with 0.5 V supply, which is superior to other prior works.

	[5]	[6]	[9]	[10]	[11]	[ <b>12</b> ]	[15]	[16]	This Work
Technology	55-nm BiCMOS	0.12-μm SiGe	65-nm CMOS	90-nm CMOS	40-nm CMOS	28-nm CMOS	28-nm CMOS	65nm CMOS	40-nm CMOS
Topology	1- attenuator + 1-CB	5-CE + 2- attenuator	2-current steering+ 1-splitting	2-cascode + 1-current steering + 1-CS	2-cascode (1-current steering)	3-CS	4-CS	3-CS	4-CS
Freq. (GHz)	73.5	81	60	78	57	79	82.3	58	73
Peak gain (dB)	4.8	24	21	23	6.7	23.8	29.6	25	24.5
Gain range (dB)	11.8 <sup>#</sup> (-7-4.8)	20	33 <sup>#</sup> (-12-21)	19.1 <sup>#</sup> (4.6–23.7)	5.7 (1.0–6.7)	4.5 (19.3– 23.8)	11.6 <sup>#</sup> (18.0–29.6)	17 (8–25)	21.3 <sup>#</sup> (3.2–24.5)
3-dB BW (GHz)	>5 (<71–>76)	>5 (<81–>86)	17 (52–69)	18.8 (68.8–87.6)	11 (51–62)	10	28.3 (68.1–96.4)	7.5 (53.5–61)	10.4 (67.8–78.2)
3-dB BW (%)	> 6.8	> 6.2	28.3	24.1	19.3	12.7	34.4	12.9	14.2
NF (dB)	-	4.5	7.9	5.3	5.1	4.9	6.4	4.8	4.8 (sim)
OP <sub>1dB</sub> (dBm)	-	-	-	-	-	-	1.5	-	-3.6 (sim)
OIP3 (dBm)	-	-	-	0.2	-	-	-	-	6.5 (sim)
PDC (mW)	18.4	67	11	55	12.1	30.6	31.3	47.5	19.1
VD (V)	1.6	1.6	1	1.2	1.1	0.9	0.9	1.3	0.5
Core area (mm <sup>2</sup> )	0.078	1.179	0.25 *	0.573 *	0.237 **	0.148 *	0.131 **	0.258 *	0.106

Table 1. Comparison with variable-gain amplifiers (VGAs) in literature.

#: Maintaining 3-dB BW, \*: chip size, including RF and DC pads, and \*\* estimated chip size without the pads.

## 4. Conclusions

This paper shows a variable-gain VGA fabricated in 40-nm CMOS technology in E-band. For the low DC power requirement, we reduced the VD down to 0.5 V, resulting in unity gain in dB per mW. The high-Q shunt capacitor enabled us to achieve approximately 30% TF area reduction, resulting in a very compact chip. One of the most serious drawbacks of the gate-bias control was migrated with the cross-coupled capacitor neutralization technique. Due to the high isolation of each gain stage, the propagation of impedance mismatch with the gate-bias control was avoided. Meanwhile, the comparative performance was achieved. The presented VGA achieved peak gain of 24.5 dB at 71.3 GHz and a 3-dB bandwidth of more than 10 GHz in 68 GHz–78 GHz range with approximately 4.8-mW power consumption per stage. The 21-dB variable-gain range was obtained by tuning the second gate voltage while maintaining 3-dB Bandwidth. The VGA performed promisingly, not only in gain tuning range and bandwidth but also in area and power dissipation for the beamforming transceivers for the unified V2X and radar applications.

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